CMOS IC – 3.5 – DIGIT A/D CONVERTER

1. DESCRIPTION

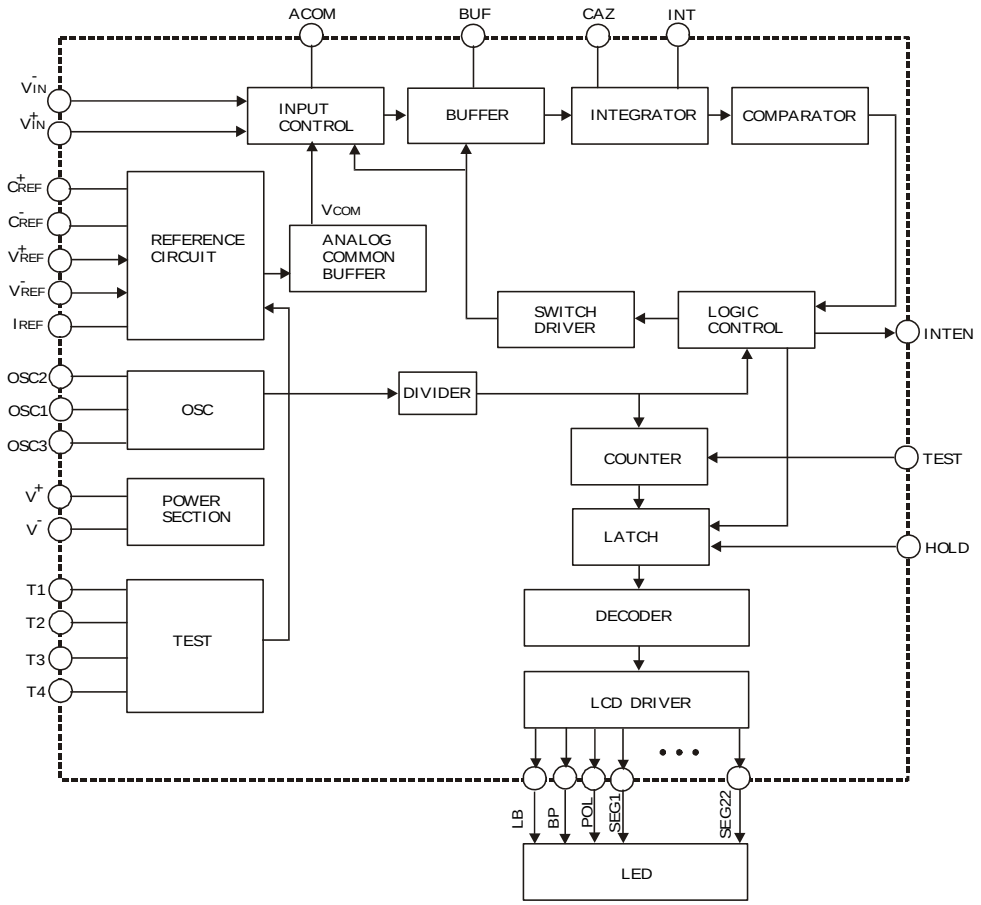
The HT7316A is high performance, low power 3 1/2 - digit A/D converter. All the necessary active devices are contained in a single CMOS IC, including seven-segment decoder, display driver, voltage reference and clock. HT7316A is designed to interface with a liquid crystal display (LCD). High accuracy 10μV for 200.0mV full-scale measurement, input bias current of 10pA max, and rollover of less than one count.

The HOLD pin makes hold or “freeze” a reading.

2. FUNCTIONS

- True polarity indication for precision null detection
- Low noise – Less than 15μ Vp-p
- Low power operation – 0.3 mW
- High Impedance CMOS differential inputs 10^{12} Ω
- True differential input and reference
- Low operating voltage: 2.5V ~ 5.2V
- Direct display drive for LCD
- No additional active components required
- Low linearity error: guaranteed less than 1 count
- Internal reference with low temperature drift
- Applications: digital panel meters, digital multimeters, thermometers, capacitance meters, PH meters, photometers etc.

3. BLOCK DIAGRAM



4. ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (V^+ to V^-)		6	V
Analog Input Voltage (either input)		V+ to V^-	V
Reference Input Voltage (either input)		V+ to V^-	V
Digital Inputs		V^- to V+	V
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage and Junction Temperature	T_{stg}	-55 ~ +150	°C

5. DC ELECTRICAL CHARACTERISTICS

V_{supply} (V^+ to V^-) = 3.0V, T_A = 25°C, f_{clock} = 48KHz, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V^+, V^-		2.5	3.0	5.2	V
Supply Current	I_{DD}	V_{IN} = 0		200		μA
Leakage Current Input	I_{LEAK}	V_{IN} = 0		1	10	pA
Segment and Back Plane Drive Voltage	V_{LCD}			3.0		V
Analog Common Voltage (With Respect to Negative Supply)	V_{ANACOM}			1.5		V
Noise (Pk-Pk Value Not exceeded 95% of Time)	V_N	V_{IN} = 0 Full Scale 200.0mV	-	15	-	μV
Zero Input Reading		V_{IN} = 0 Full Scale 200.0mV	-000.0	± 000.0	± 3	Digital Reading
Ratiometric Reading		V_{IN} = V_{REF} =100.0mV	999	999/1000	1000	Digital Reading
Linearity (Max. Deviation From Best Strait Line Fit)		Full Scale 200.0mV	-1	± 0.2	+1	Counts
Scale Factor Temp Coeff. (Advanced)		V_{IN} = 199.0mV 0 °C < T_A < 70 °C		± 5		ppm/ °C
Rollover Error		V^-_{IN}= V^+_{IN} =200.0mV	-1	± 0.2	+1	Counts
Reference Current	I_{REF}		18.6	19	19.4	μA
Reference Current Supply Voltage Ratio	$\Delta I_{REF}/\Delta V$	V = (V+ - V^-)		0.1		μA/V
Low Battery Detection Voltage	V_{LV}			2.5		V

6. FUNCTIONAL DESCRIPTION

An input signal to be measured is applied to the integrating capacitance for a fixed time as determined by a clock counter. The accumulated charge will be proportional to the input signal, for a fixed clock rate and constant current. The resulting integral is returned to zero by integrating a reference signal of polarity opposite that of the input signal. The length of time required for the integrator to return to zero, as measured with the clock counter to display at output, is proportional to the average magnitude of the input signal over the integration period

6.1. Analog Selection

Fig.1 shows the block diagram of the Analog Section for HT7316A. Each measurement cycle is divided into three parts.

They are:

(1) Signal integrated [INT]

(2) Deintegrated [DE]

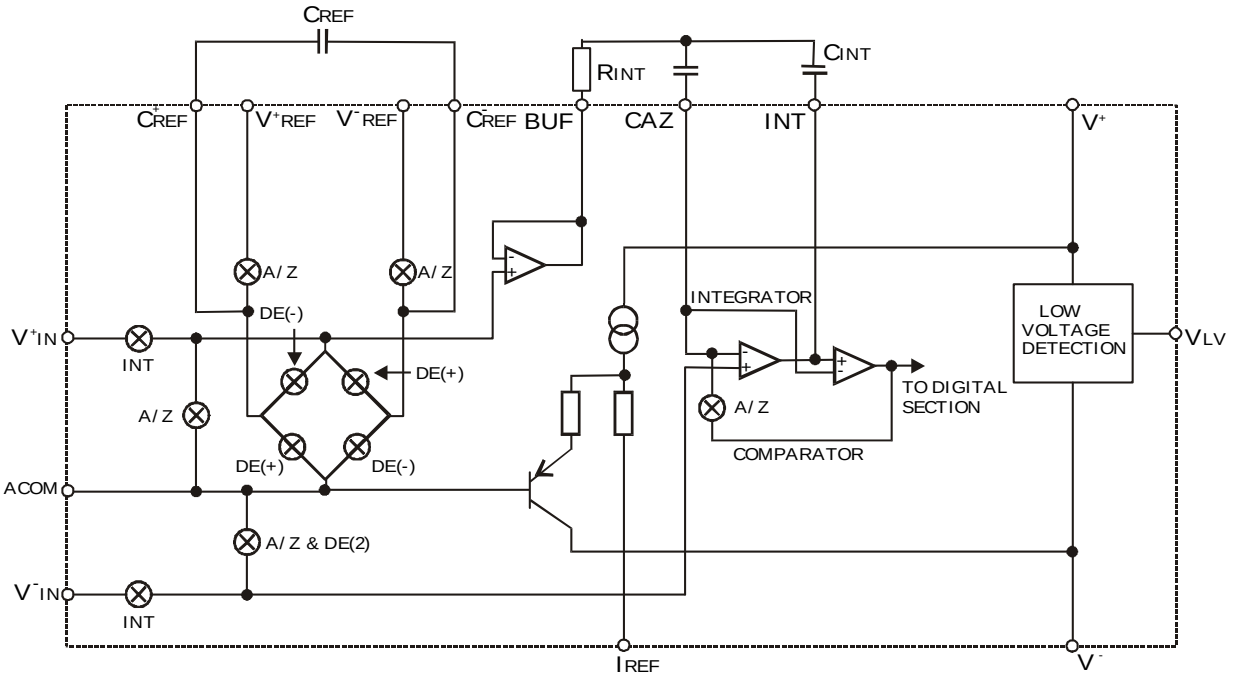


Fig.1 HT7316A Analog Section

a. Type Phase

During type phase, three things happen:

(1) Input high and low are disconnected from PIN and shorted to analog COMMON.

(2) The reference capacitor is charged to the reference voltage.

A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator and comparator.

b. Signal Integrate Phase

During signal integrate, the type phase loop is opened, the internal short is removed, and the internal inputs high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time (1000 counts). At the end of this phase, the polarity of the integrated signal is determined.

c. De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to Analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to type phase. The time required to return to type phase is proportional to the input signal. Specifically, the digital reading displayed is 1000

b. Digital Selection

Fig.2 show the digital section for the HT7316A. The internal digital ground is equal with V^- voltage. The BP frequency

is the clock frequency divided by 800. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible DC voltage exists across the segments.

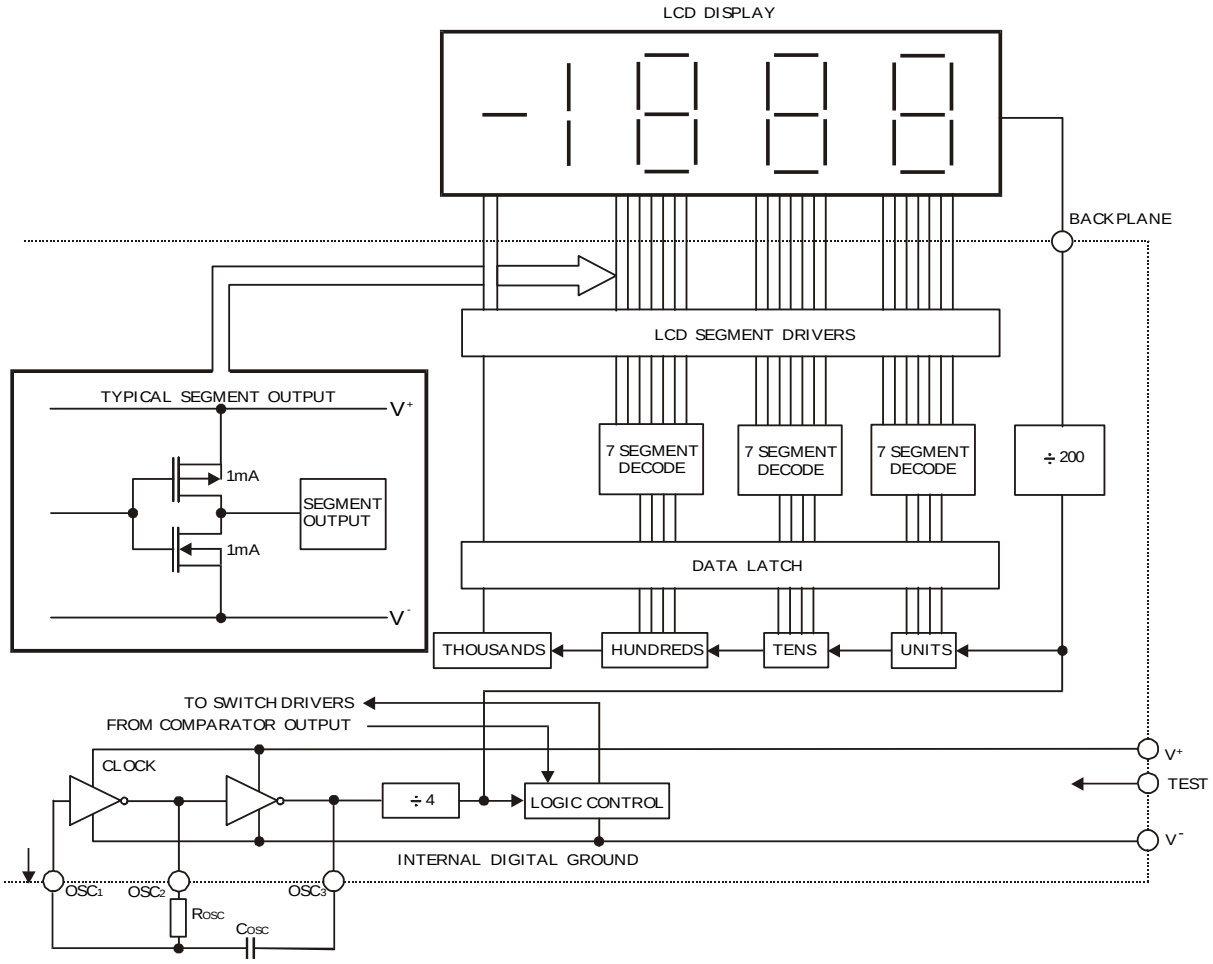
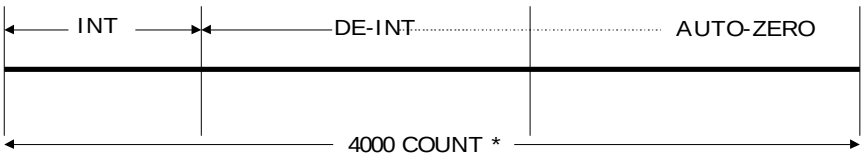


Fig.2 HT7316A Digital Section

6.2 System Timing

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phase. These are: signal integrated (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes complete measure cycles of 4000 (16000 clock pulses) independent of input voltage.



* as a matter of fact, the total measurement cycle is 4001 counts for measured values less than 2000 counts The measurement cycle becomes 4000 counts for overflow measurement

6.3 Clock Circuit:

HT7316A may use the following clocking methods:

1. An external oscillator connected to OSC_1.
2. An RC oscillator using OSC_1, OSC_2 and OSC_3.

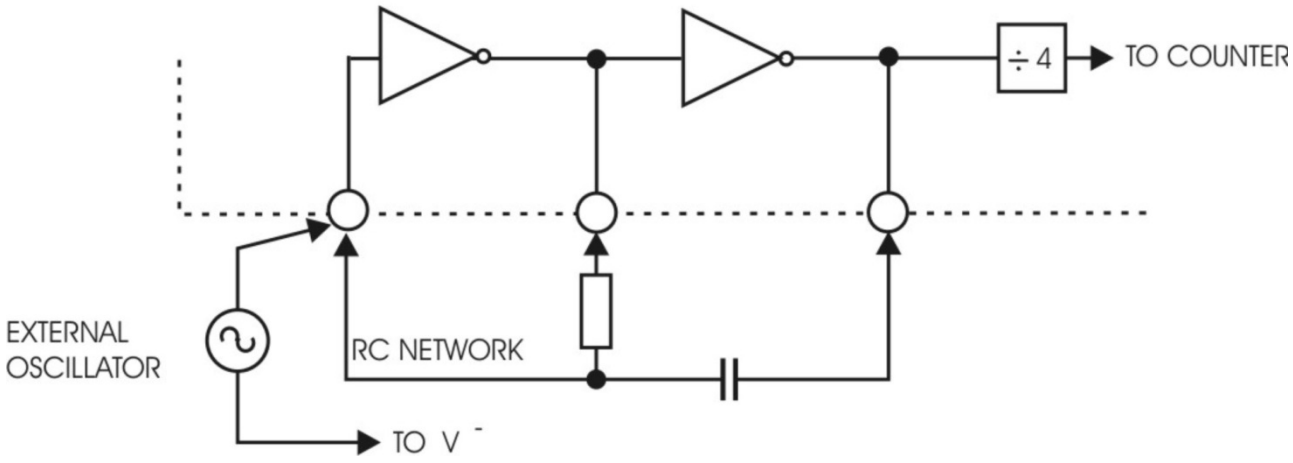


Fig.3 Clock Circuit

6.4 Integrating Resistor (R_{INT}) :

The buffer amplifier and integrator are designed with class A output stages with 10μA of quiescent current each. They can supply 10μA drive current with negligible linearity errors. R_{INT} should be large enough to remain in linear region but small enough to reduce the leakage current on the PC board. For 200mv full scale, R_{INT} is 200KΩ.

6.5 Oscillator Components (R_{OSC}, C_{OSC}) :

While using RC oscillator, the R_{OSC} (between OSC_1 and OSC_2) should be 100KΩ and C_{OSC} is selected from the following equation:

$$F_{osc} = \frac{0.45}{R_{osc} \bullet C_{osc}}$$

(R_{OSC} in MΩ, C_{OSC} in μF)

6.6 Integrating Capacitor (C_{INT}) :

C_{INT} should be chosen to give the maximum voltage swing without causing the saturation of integrator output swing. An additional requirement of C_{INT} is that C_{INT} must have low dielectric absorption to minimize rollover error. Polypropylene capacitors give undetectable errors at reasonable cost

6.7 Reference Voltage Selection:

The analog input required to generate full scale output (2000 counts) is $V_{IN} = V_{REF}$, thus:

V_{REF} = 100mV for full scale voltage 200mV.

V^-_{IN} and the transducer output is connected between V^+_{IN} and analog common.

6.8 Reference Voltage Capacitor (C_{REF}):

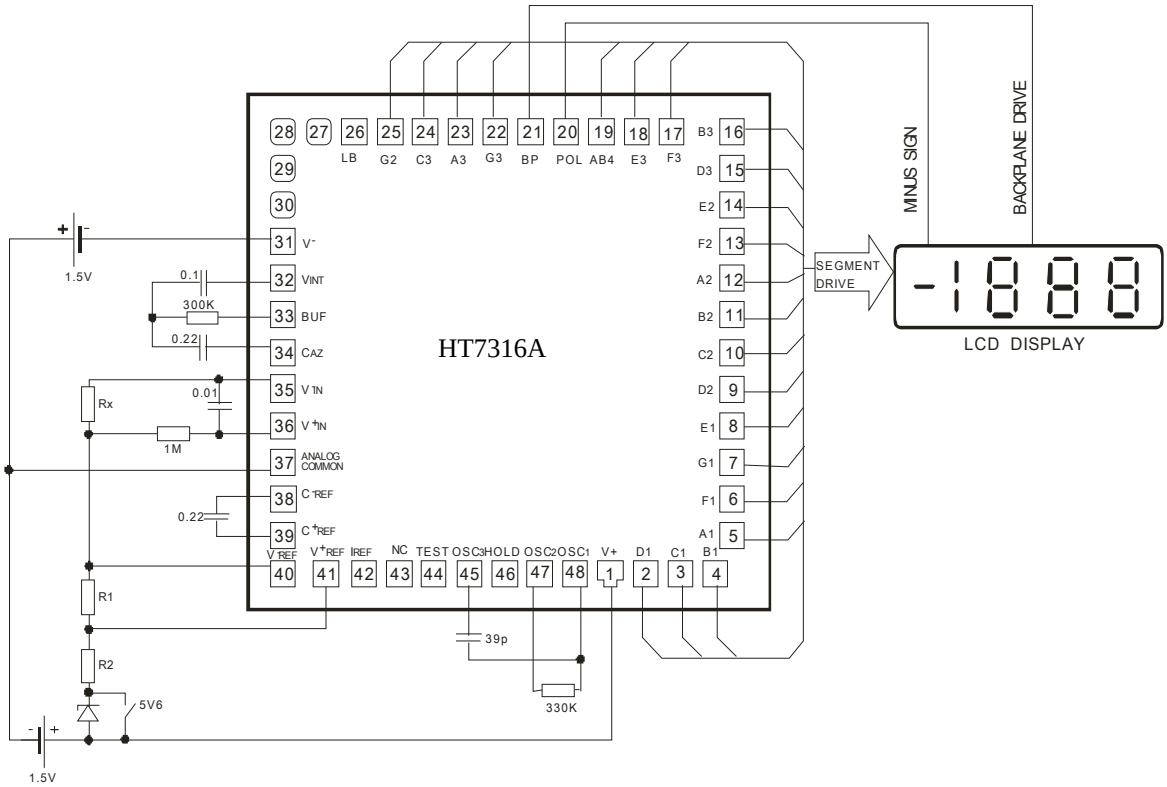
The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1μF capacitor gives good performance when V^-_{IN} is tied to analog common. If a large analog common voltage exists (V^-_{REF} unequal analog common) and a 200.0mV scale is used, a larger value is required to prevent rollover error. Generally 0.1μF will hold the rollover error to 0.5 count. In this case a mylar type dielectric capacitor is adequate

6.9 Reference Current (I_{REF}):

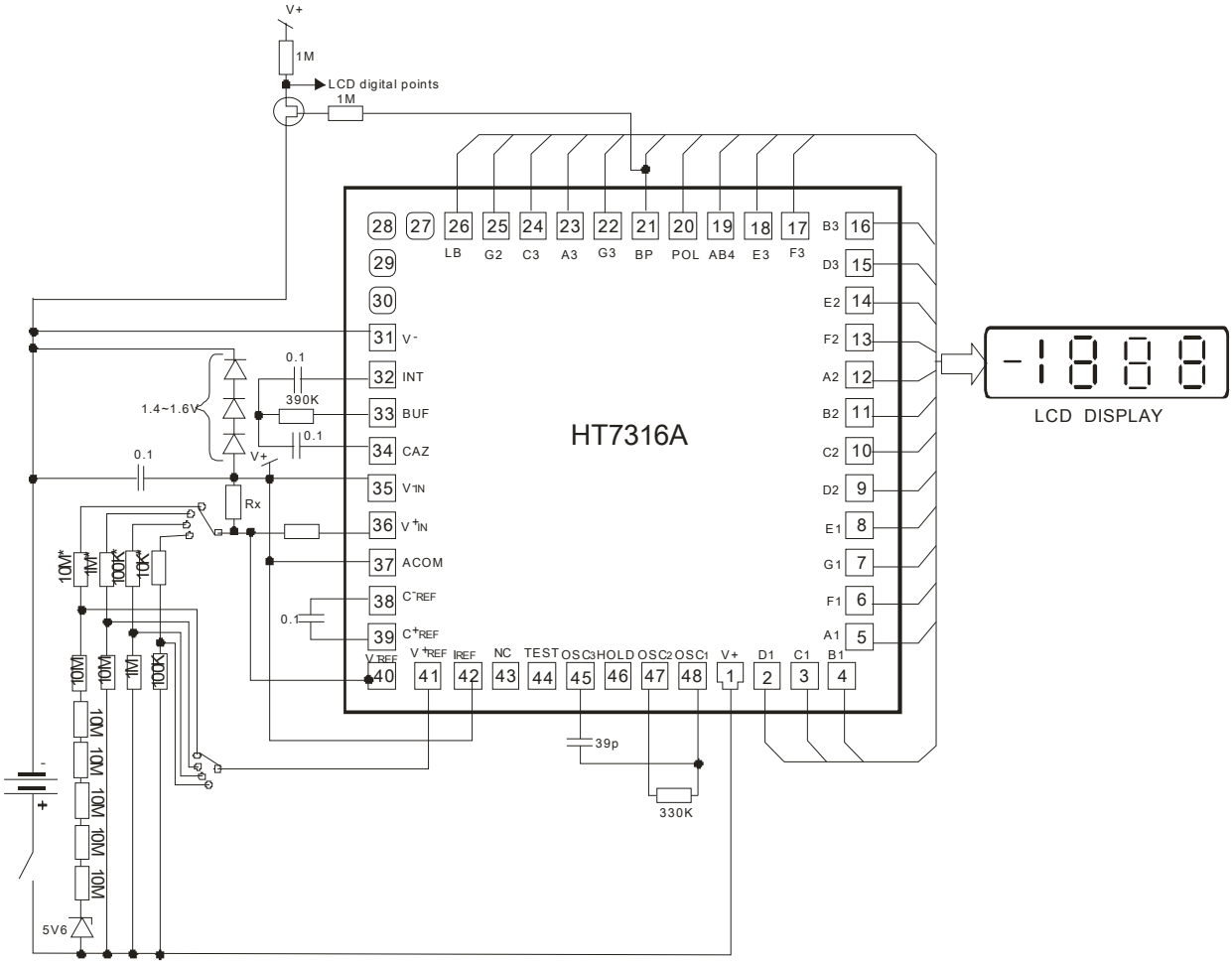
The 19μA reference current source is trimmed to 2.0% tolerance at T_A=25°C. It is intended to be used in conjunction with the external resistors to generate reference voltage

7. APPLICATION CIRCUITS

a. Resistance Meter (Two 1.5V batteries)



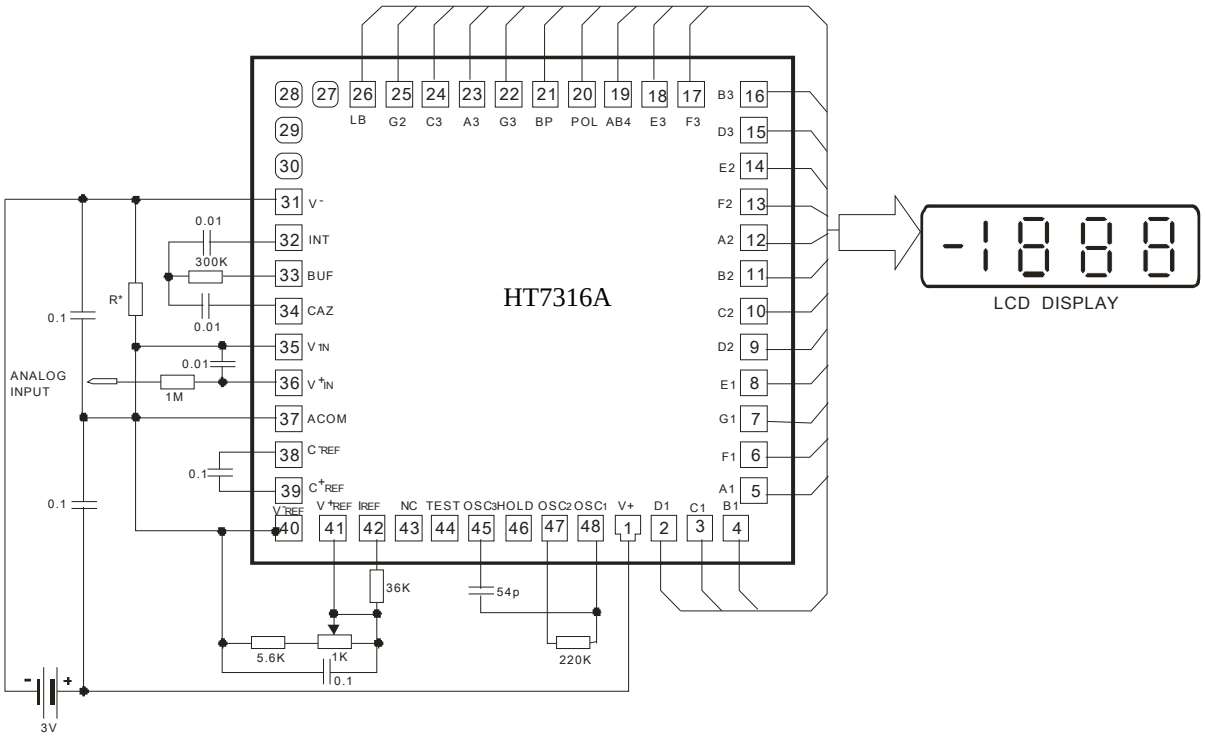
b. Resistance Meter (3V)



NOTE:

1. The chip substrate is electrically connected to V_{SS}.
2. R* - accuracy these resistors must be 1%.
3. $f_{OSC} \approx 32kHz$; $f_{LCD} = f_{OSC}/800$.

c. Voltmeter (3V battery)



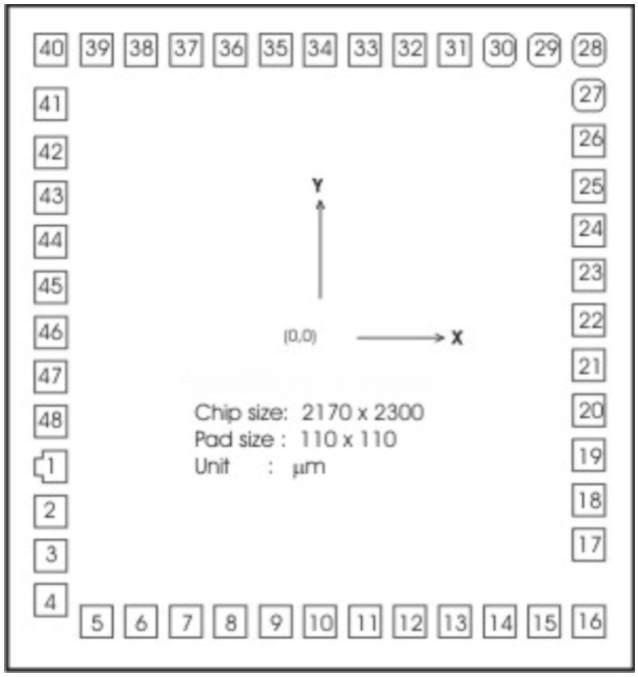
Notes: 1. The chip substrate is connected to Vss.

2. By R* = 75kΩ, the ACOM voltage is adjusted to min (V^+ - V^-)/2.

Resistor R* , which connects from V- to V-in, should be about 75kOhm, but correct value must be adjusted, - ACOM voltage is depended from this resistor and this resistor must be selected to adjust ACOM voltage (see Note 2).

(To simplify possible procedure we can recommend reserve two places for this resistor, as from sum of two resistors can be easy receive good result. Evidently maybe one resistor can be enough

8. PAD DIAGRAM



9. PAD DESCRIPTION

Pad No.	Pad Name	Description
1	V^+	Positive supply voltage.
2	D1	Activates the D section of the units display.
3	C1	Activates the C section of the units display.
4	B1	Activates the B section of the units display.
5	A1	Activates the A section of the units display.
6	F1	Activates the F section of the units display.
7	G1	Activates the G section of the units display.
8	E1	Activates the E section of the units display.
9	D2	Activates the D section of the tens display.
10	C2	Activates the C section of the tens display.
11	B2	Activates the B section of the tens display.
12	A2	Activates the A section of the tens display.
13	F2	Activates the F section of the tens display.
14	E2	Activates the E section of the tens display.
15	D3	Activates the D section of the hundreds display
16	B3	Activates the B section of the hundreds display
17	F3	Activates the F section of the hundreds display.
18	E3	Activates the E section of the hundreds display.
19	AB4	Activates both halves of the 1 in the thousands display.
20	POL	Activates the negative polarity display.
21	BP	LCD Backplane drive output.
22	G3	Activates the G section of the hundreds display.
23	A3	Activates the A section of the hundreds display.
24	C3	Activates the C section of the hundreds display.
25	G2	Activates the G section of the tens display.
26	LB	Low – Battery flag segment driver.
27	T1	Test pad.

28	T2	Test pad.
29	T3	Test pad.
30	T4	Test pad.
31	V^-	Negative power supply voltage.
32	INT	Integrator output. Connection point for integration capacitor.
33	BUF	Integration resistor connection.
34	CAZ	Auto-zero capacitor connection point.
35	V^-_{IN}	The analog LOW input is connected to this pin.
36	V^+_{IN}	The analog HIGH input is connected to this pin.
37	ACOM	Analog common point.
38	C^-_{REF}	Reference capacitor, negative terminal.
39	C^+_{REF}	Reference capacitor, positive terminal. A 0.1μF capacitor is used in most applications.
40	V^-_{REF}	Analog reference input, negative terminal.
41	V^+_{REF}	Analog reference input, positive terminal.
42	I_{REF}	Reference Current Output.
43	NC	
44	TEST	LCD test. When TEST pulled to V^+, LCD should read – 1888.
45	OSC_3	See OSC_1
46	HOLD	Hold input. Logic 1 hold display.
47	OSC_2	See OSC_2
48	OSC_1	Pins OSC_1, OSC_2 and OSC_3 make up the oscillator section.

10. PAD LOCATION

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	V^+	-930	-445	25	G2	930	525
2	D1	-930	-600	26	LB	930	680
3	C1	-930	-755	27	T1	930	840
4	B1	-930	-915	28	T2	930	995
5	A1	-775	-995	29	T3	775	995
6	F1	-620	-995	30	T4	620	995
7	G1	-465	-995	31	V^-	465	995
8	E1	-310	-995	32	INT	310	995
9	D2	-155	-995	33	BUF	155	995
10	C2	0	-995	34	CAZ	0	995
11	B2	155	-995	35	V^-_{IN}	-155	995
12	A2	310	-995	36	$V+_{IN}$	-310	995
13	F2	465	-995	37	ACOM	-465	995
14	E2	620	-995	38	C^-_{REF}	-620	995
15	D3	775	-995	39	$C+_{REF}$	-775	995
16	B3	930	-995	40	V^-_{REF}	-930	995
17	F3	930	-715	41	$V+_{REF}$	-930	810
18	E3	930	-560	42	I_{REF}	-930	640
19	AB4	930	-135	43	NC	-930	485
20	POL	930	-250	44	TEST	-930	330
21	BP	930	-95	45	OSC3	-930	175
22	G3	930	60	46	HOLD	-930	20
23	A3	930	215	47	OSC2	-930	-135
24	C3	930	370	48	OSC1	-930	-290