

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

BVDSS	RDSON	ID
100V	4.7mΩ	100A

PRPAK5X6 Pin Configuration

Description

AGM056N10A is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM056N10A	AGM056N10A	DFN5*6	325mm	16mm	3000

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V _{DS}	Drain-Source Voltage (V _{GS} =0V)	100	V
V _{GS}	Gate-Source Voltage (V _{DS} =0V)	±20	V
I _D	Drain Current-Continuous(T _c =25°C) (Note 1)	100	A
	Drain Current-Continuous(T _c =100°C)	75	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed (Note 2)	300	A
P _D	Maximum Power Dissipation(T _c =25°C)	123	W
	Maximum Power Dissipation(T _c =100°C)	63	W
EAS	Avalanche energy (Note 3)	120	mJ
T _J ,T _{STG}	Operating Junction and Storage Temperature Range	-55 To 150	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
R _{θJA}	Thermal Resistance Junction-ambient (Steady State) ¹	---	55	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.1	°C/W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.6	2.5	v
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		85		S
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =20A		4.7	6.5	mΩ
		V _{GS} =4.5V, I _D =15A		6.5	8.5	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =50V, V _{GS} =0V, F=1MHZ		3100		pF
C _{oss}	Output Capacitance			605		pF
C _{rss}	Reverse Transfer Capacitance			20		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1.0MHz		1.7		Ω
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{GS} =10V, V _{DS} =50V, I _D =14A, R _{GEN} =3.3Ω		10		nS
t _r	Turn-on Rise Time			6.5		nS
t _{d(off)}	Turn-Off Delay Time			45		nS
t _f	Turn-Off Fall Time			7.5		nS
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =12A		43		nC
Q _{gs}	Gate-Source Charge			18		nC
Q _{gd}	Gate-Drain Charge			9.5		nC
Source-Drain Diode Characteristics						
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			80	A
V _{SD}	Forward on Voltage	V _{GS} =0V, I _S =20A			1.0	V
t _{rr}	Reverse Recovery Time	I _F =15A, dI/dt=100A/μs, ·T _J =25°C			30	ns
Q _{rr}	Reverse Recovery Charge					148

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: T_J=25°C, V_{DD}=50V, V_G=10V, R_G=3.3Ω

Typical Characteristics

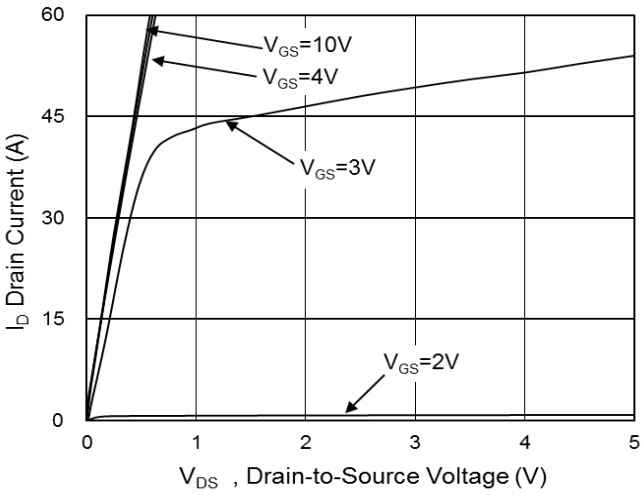


Fig.1 Typical Output Characteristics

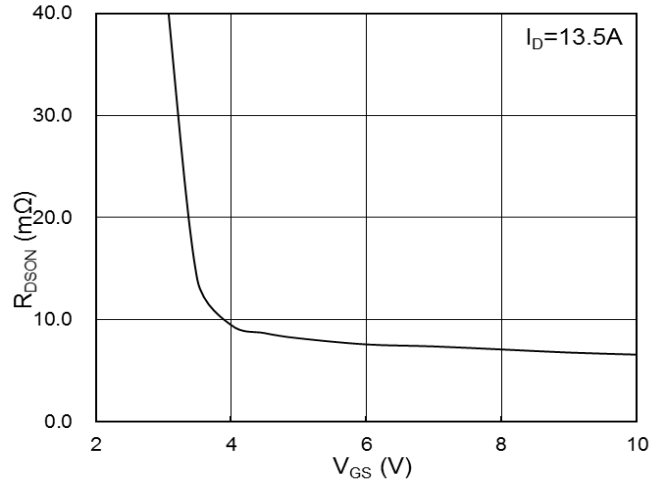


Fig.2 On-Resistance vs. G-S Voltage

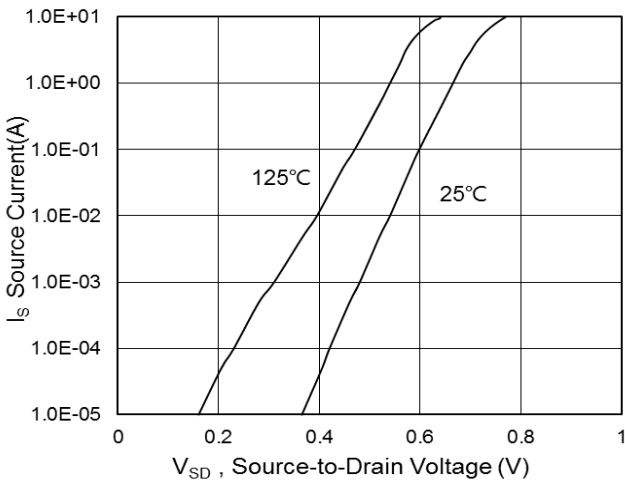


Fig.3 Source-Drain Forward Characteristics

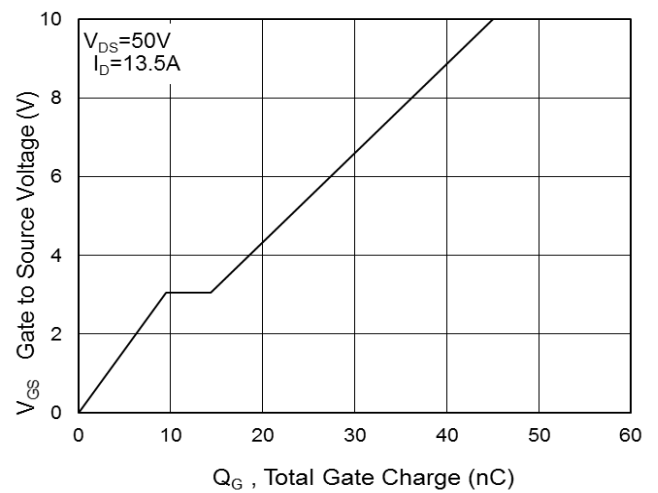


Fig.4 Gate-Charge Characteristics

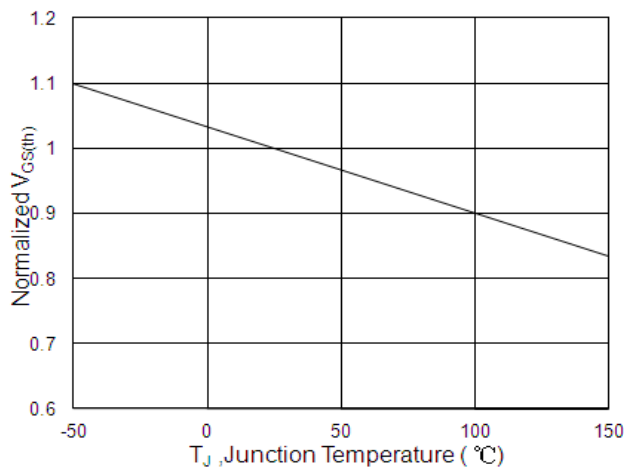


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

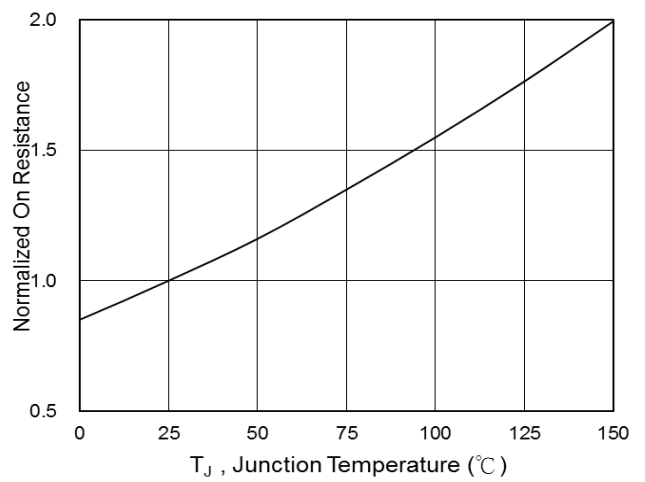


Fig.6 Normalized R_{DSON} vs. T_J

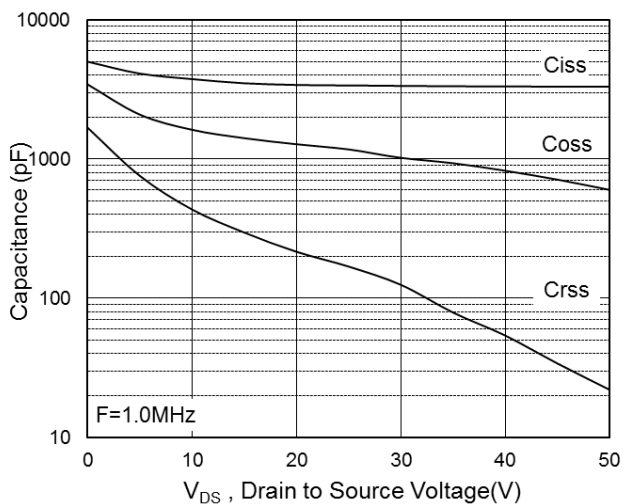


Fig.7 Capacitance

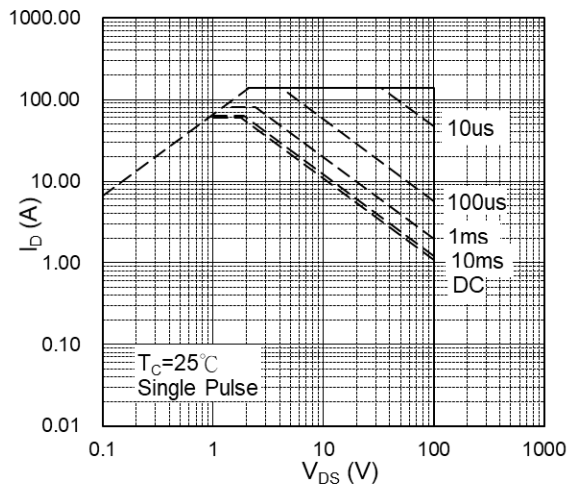


Fig.8 Safe Operating Area

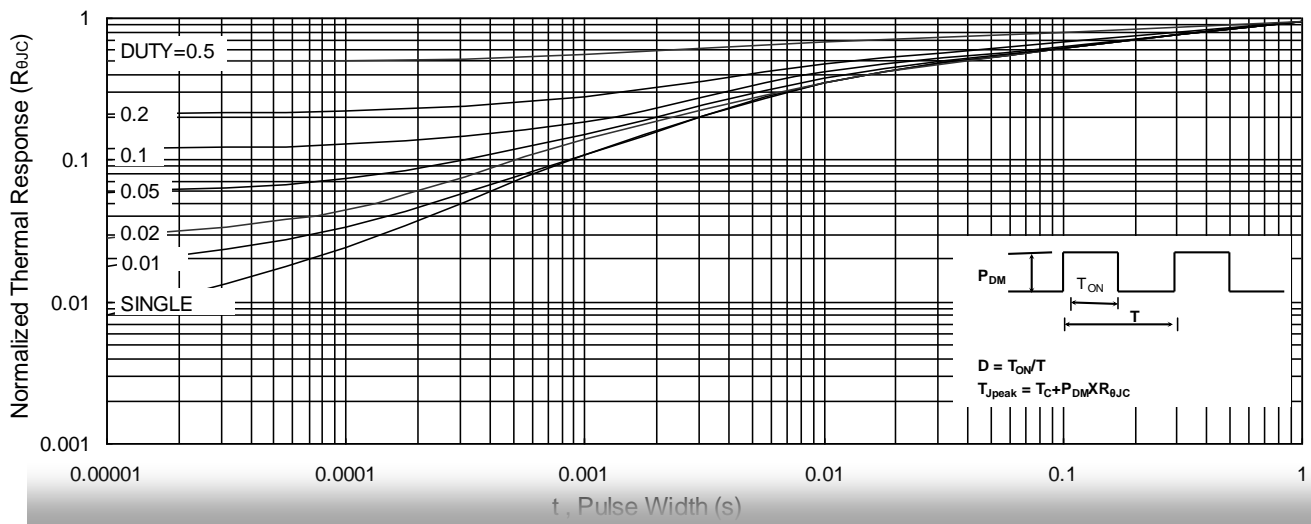


Fig.9 Normalized Maximum Transient Thermal Impedance

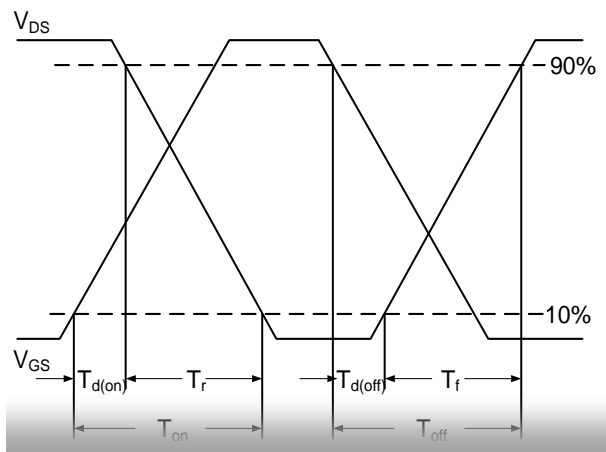


Fig.10 Switching Time Waveform

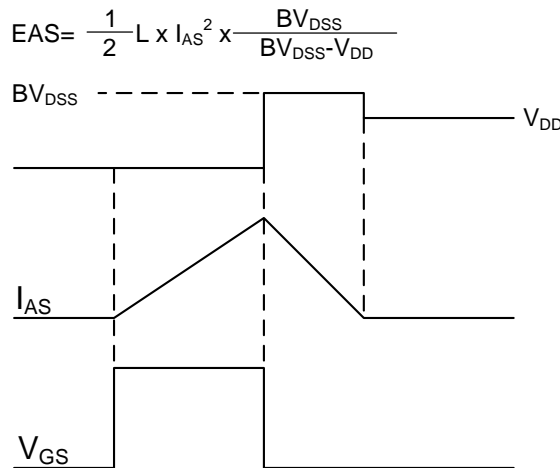
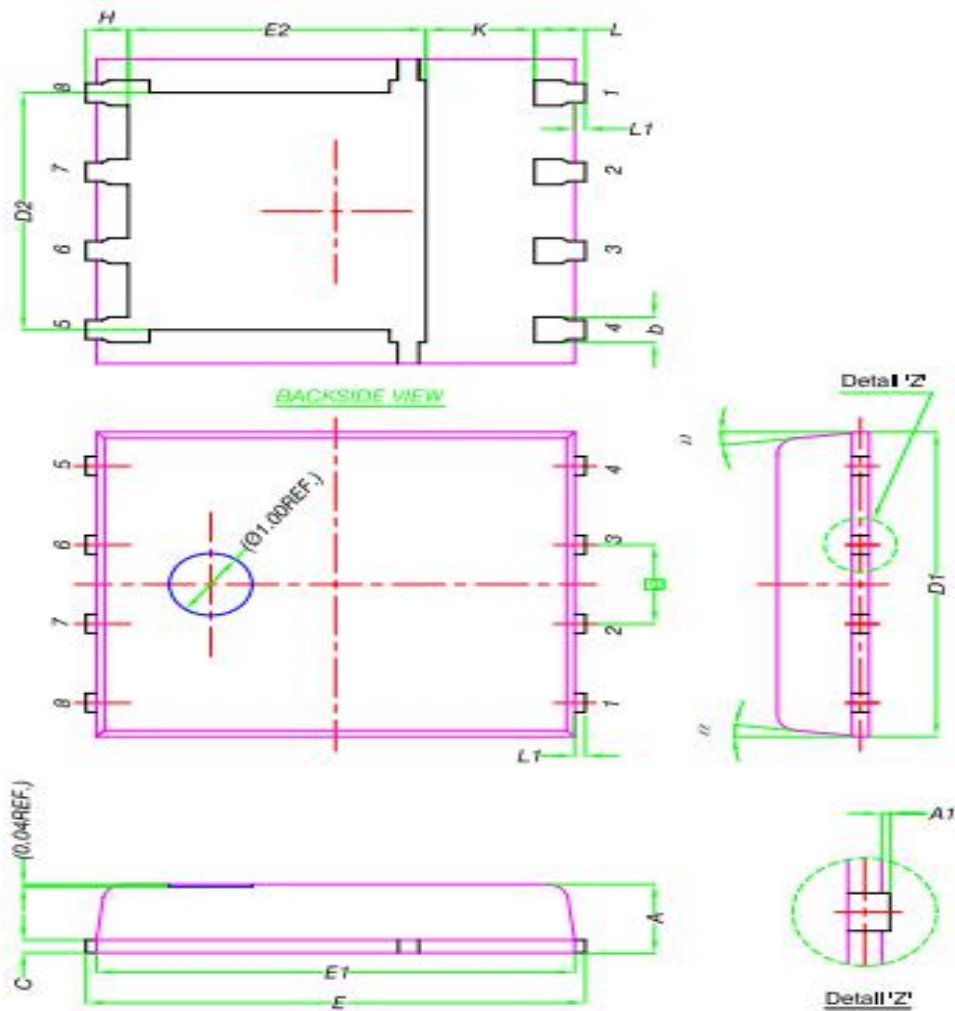


Fig.11 Unclamped Inductive Switching Waveform

●Dimensions (DFN5×6)


DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°


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