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# FDD306P

## P-Channel 1.8V Specified PowerTrench<sup>®</sup> MOSFET

### Features

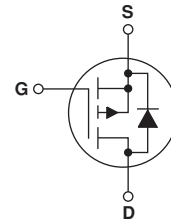
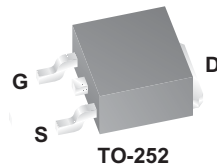
- -6.7 A, -12 V.  $R_{DS(ON)} = 28\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$   
 $R_{DS(ON)} = 41\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$   
 $R_{DS(ON)} = 90\text{ m}\Omega @ V_{GS} = -1.8\text{ V}$
- Fast switching speed
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability

### Applications

- DC/DC converter

### General Description

This P-Channel 1.8V Specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management.



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-12	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current – Continuous (Note 3)	-6.7	A
	– Pulsed (Note 1a)	-54	
$P_D$	Power Dissipation for Single Operation (Note 1)	52	W
		3.8 (Note 1a)	
		1.6 (Note 1b)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$
<b>Thermal Characteristics</b>			
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD306P	FDD306P	13"	16mm	2500 units

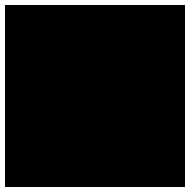
FDD306P P-Channel 1.8V Specified PowerTrench<sup>®</sup> MOSFET

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-0.6		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		2.2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -6.7\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -6.1\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -4.8\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -6.7\text{ A}, T_J = 125^\circ\text{C}$		21 29 42 25	28 41 90	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-45			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -6.7\text{ A}$		22		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		1290		pF
$C_{oss}$	Output Capacitance			590		pF
$C_{rss}$	Reverse Transfer Capacitance			430		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		4.2		$\Omega$
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -6\text{ V}, I_D = -1\text{ A}, V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		16	29	ns
$t_r$	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			34	54	ns
$t_f$	Turn–Off Fall Time			41	65	ns
$Q_g$	Total Gate Charge	$V_{DS} = -6\text{ V}, I_D = -6.7\text{ A}, V_{GS} = -4.5\text{ V}$		15	21	nC
$Q_{gs}$	Gate–Source Charge			2.0		nC
$Q_{gd}$	Gate–Drain Charge			4.4		nC
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-3.2	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -3.2\text{ A}$ (Note 2)		-0.8	-1.2	V
$T_{rr}$	Diode Reverse Recovery Time	$I_F = -6.7\text{ A}, diF/dt = 100\text{ A}/\mu\text{s}$ (Note 3)		37		ns
$I_{rm}$	Diode Reverse Recovery Current			0.9		A
$Q_{rr}$	Diode Reverse Recovery Charge			17		nC

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $R_{\theta JA} = 40^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $R_{\theta JA} = 96^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

3. Maximum current is calculated as:  $\sqrt{\frac{P_D}{R_{DS(on)}}}$  where  $P_D$  is maximum power dissipation at  $T_C = 25^\circ\text{C}$  and  $R_{DS(on)}$  is at  $T_J(\text{max})$  and  $V_{GS} = 10\text{ V}$ .

4. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = -4\text{ A}$ ,  $V_{GS} = -10\text{ V}$ ,  $V_{DD} = -12\text{ V}$ .

## Typical Characteristics

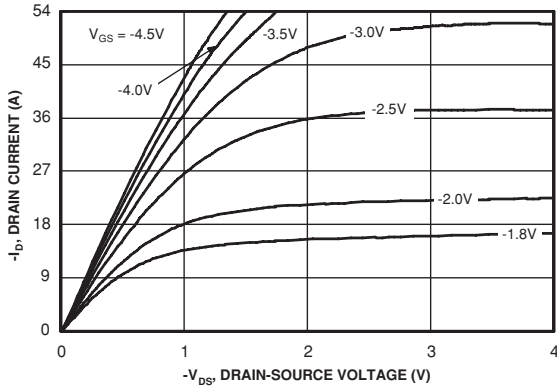


Figure 1. On-Region Characteristics.

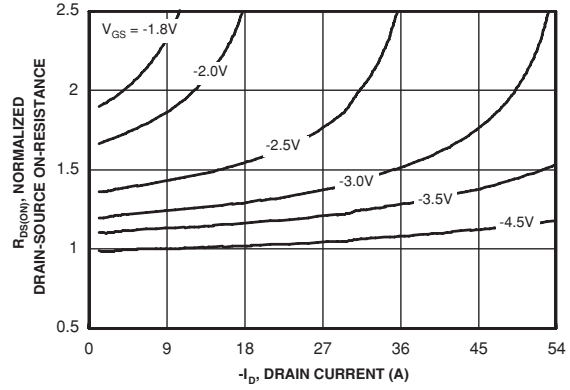


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

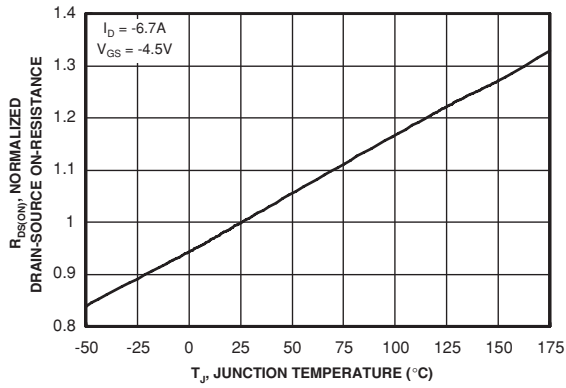


Figure 3. On-Resistance Variation with Temperature.

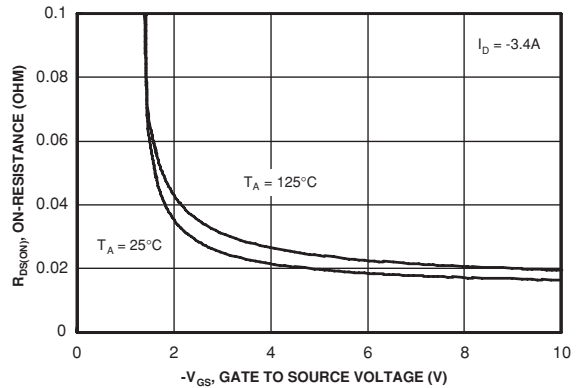


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

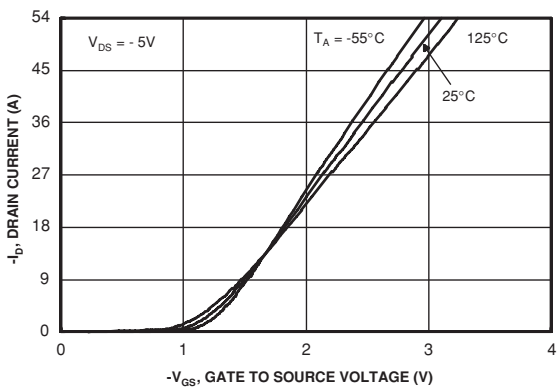


Figure 5. Transfer Characteristics.

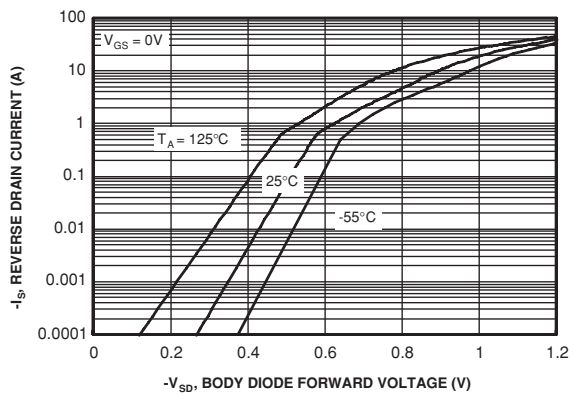
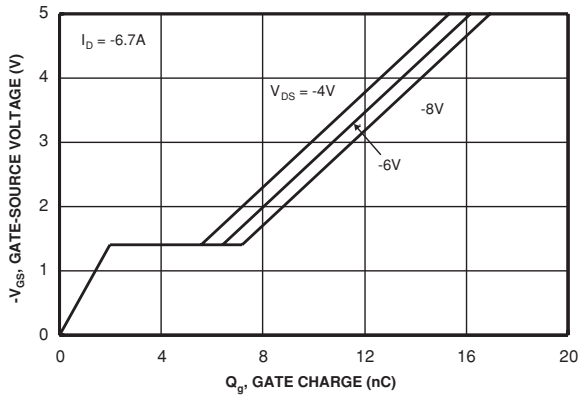
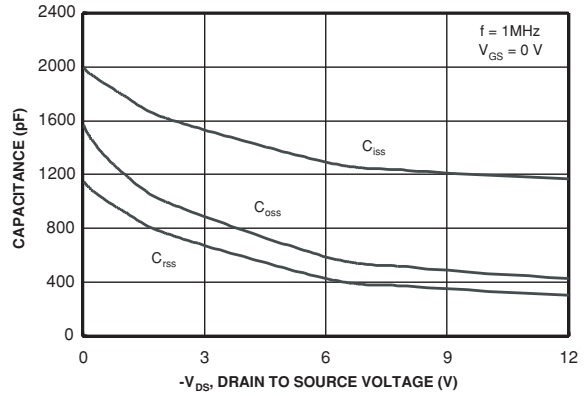


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

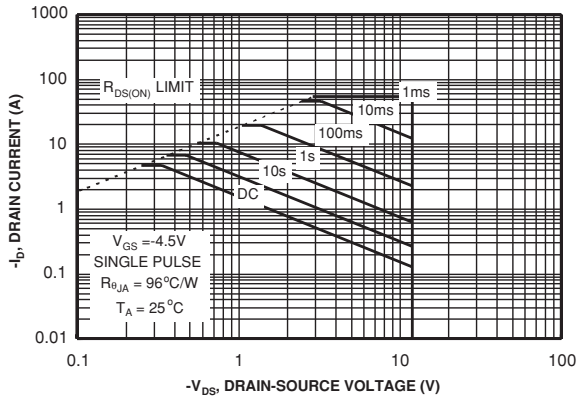
### Typical Characteristics



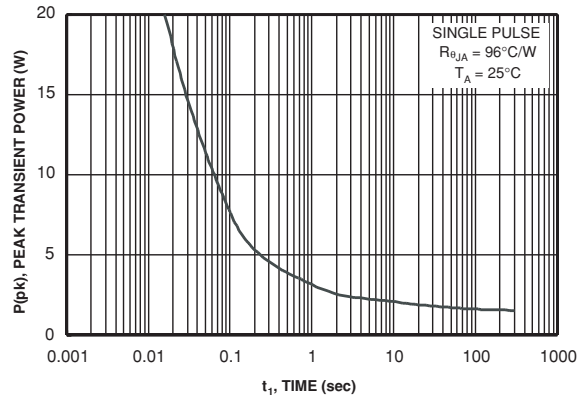
**Figure 7. Gate Charge Characteristics.**



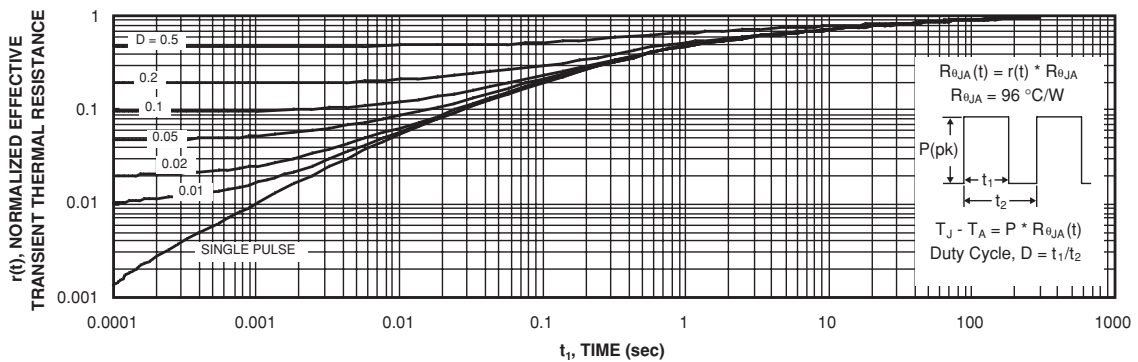
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



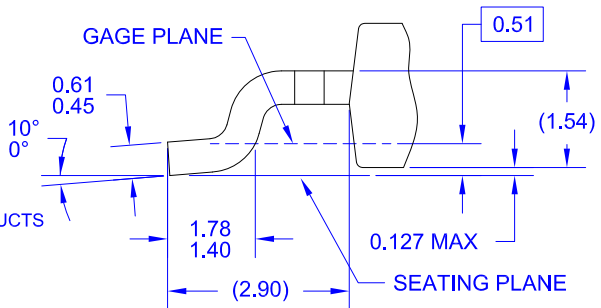
**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A  
(ROTATED -90°)  
SCALE: 12X



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