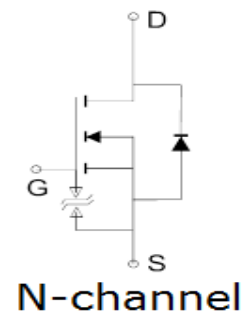
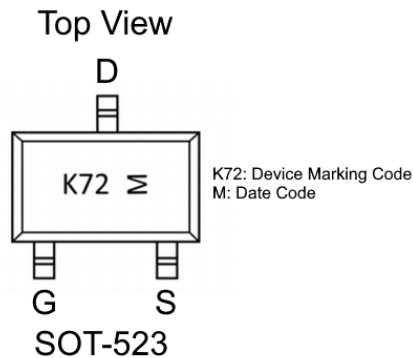


## General Description

The FX2N7002KMFH-06S1G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

## PIN Configuration



## Features

- $R_{DS(ON)} \leq 3\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 4\Omega @ V_{GS}=4.5V$
- ESD Protection HBM >2KV
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

## Applications

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

## Absolute Maximum Ratings(TA=25oC Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain	$T_A=25^\circ C$	$I_D$	A
	$T_A=70^\circ C$	$I_D$	
Pulsed Drain Current	$I_{DM}$	1.07	A
Maximum Power Dissipation	$T_A=25^\circ C$	$P_D$	W
	$T_A=70^\circ C$	$P_D$	
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	367	$^\circ C/W$

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

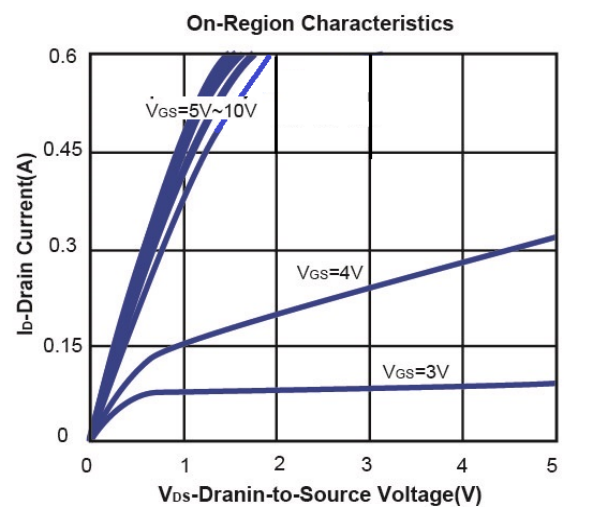
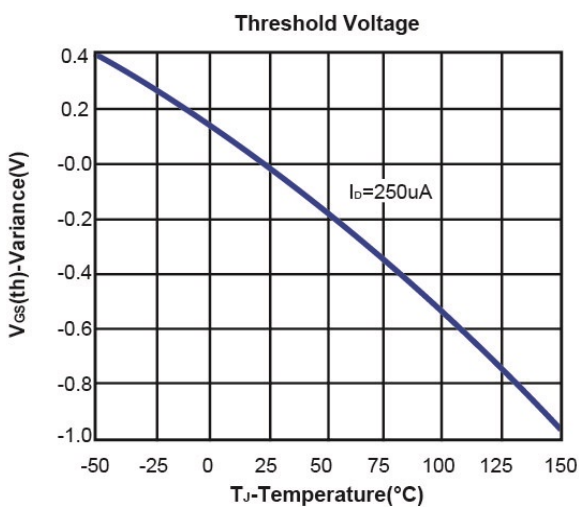
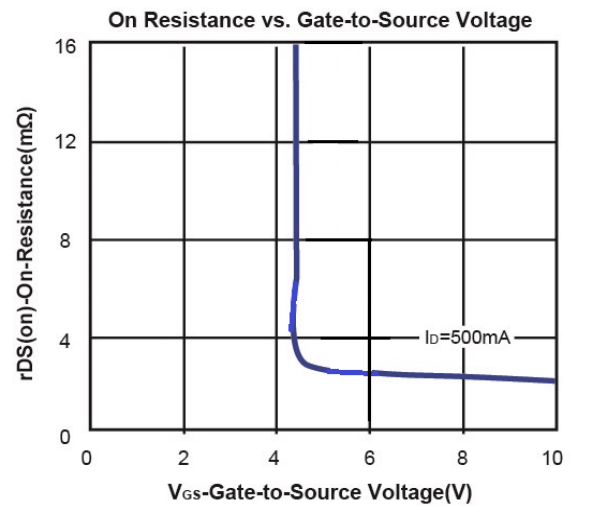
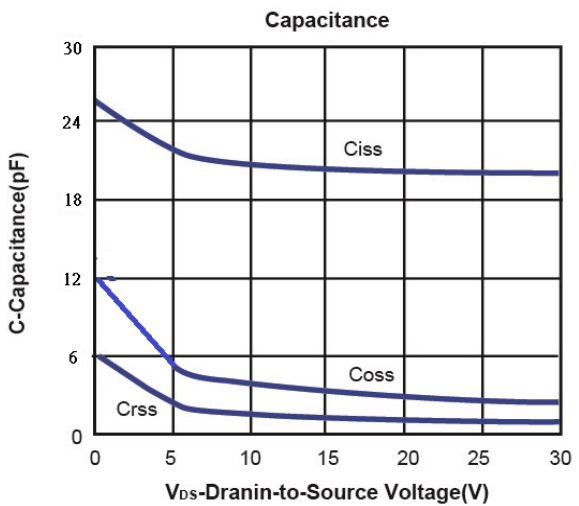
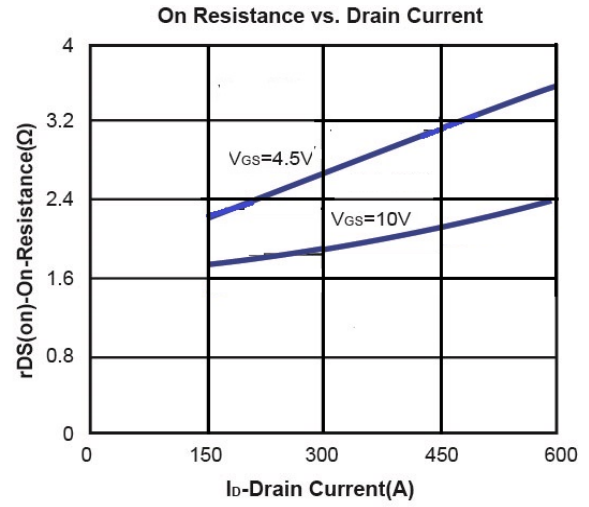
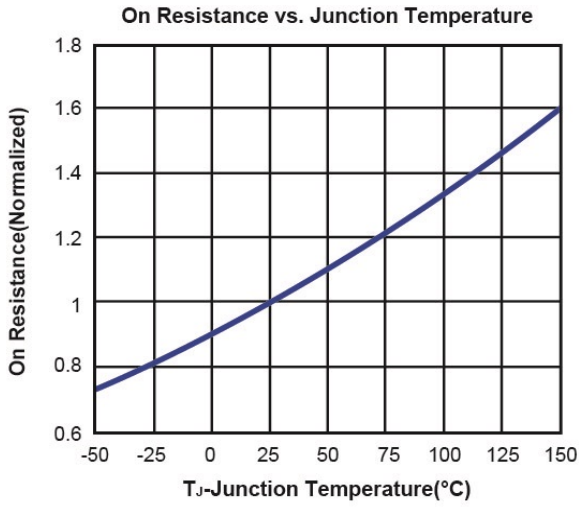
*Electrical Characteristics (TA =25 °C Unless Otherwise Specified)*

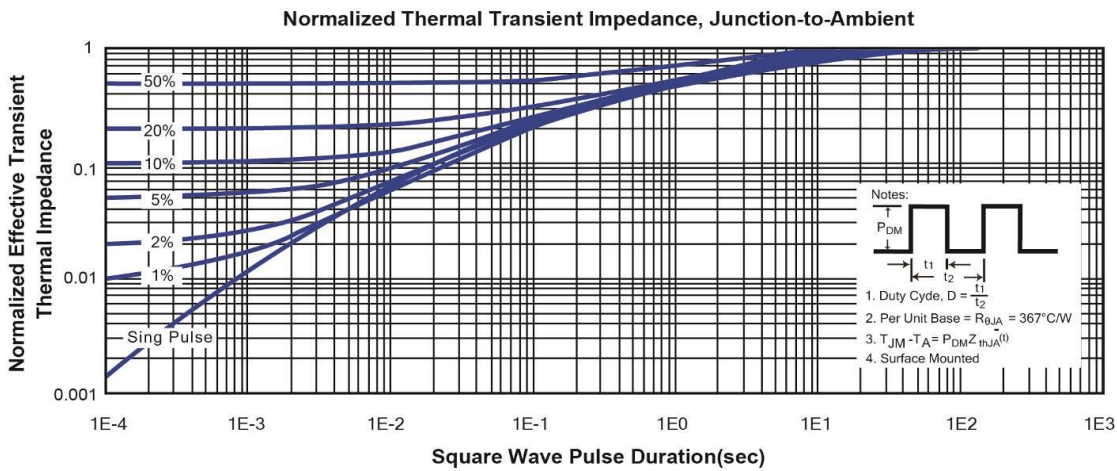
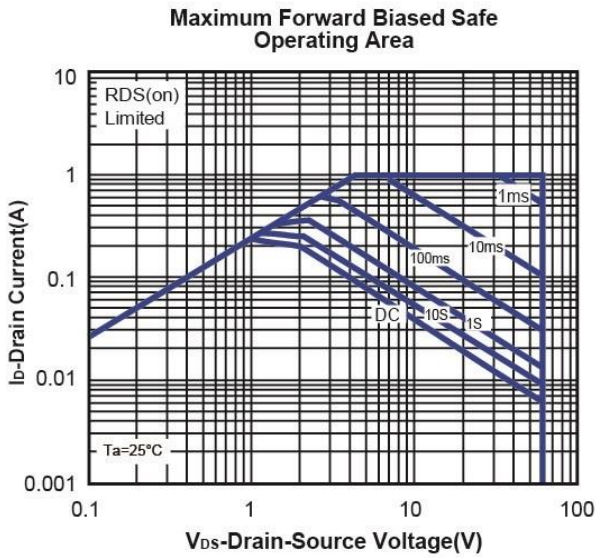
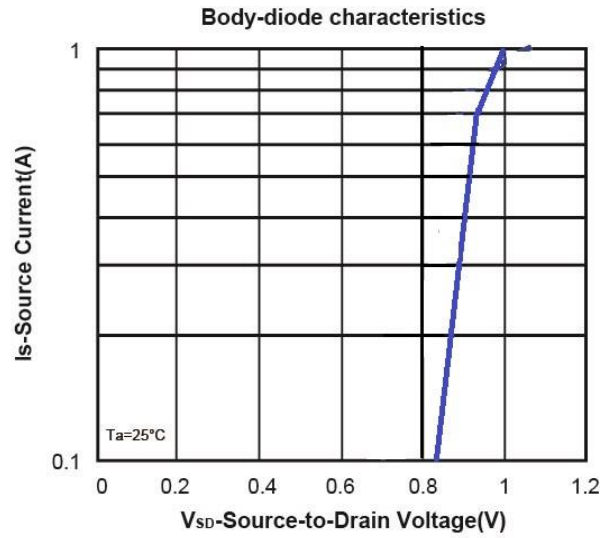
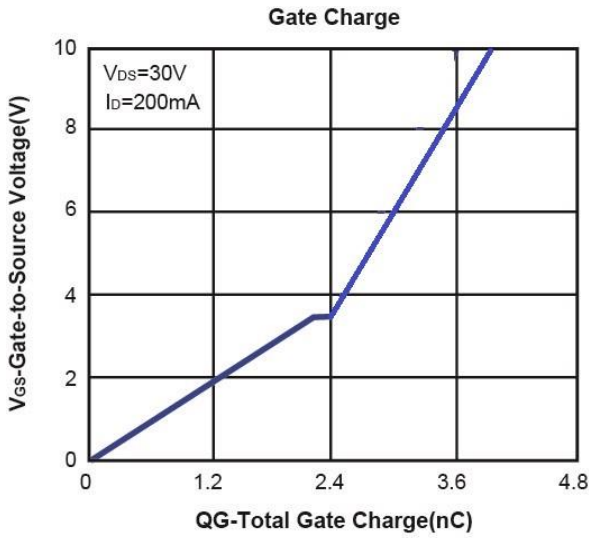
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0, I <sub>D</sub> =10uA	60			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.3		2.1	V
I <sub>GSS</sub>	Gate Body Leakage	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±10	uA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	uA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =500mA			3	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =200mA			4	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =200mA, V <sub>GS</sub> =0V			1.2	V
<b>Dynamic</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, V <sub>GS</sub> =10V, I <sub>D</sub> =200mA		3.7		nC
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =200mA		1.4		
Q <sub>gs</sub>	Gate-Source Charge			2.2		
Q <sub>gd</sub>	Gate-Drain Charge			0.2		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		21		pF
C <sub>oss</sub>	Output Capacitance			3		
C <sub>rss</sub>	Reverse Transfer Capacitance			1		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =30V, R <sub>L</sub> =150Ω V <sub>GS</sub> =10V, R <sub>GS</sub> =10Ω I <sub>D</sub> =200mA		3.5		Ns
t <sub>r</sub>	Turn-On Rise Time			20.3		
t <sub>d(off)</sub>	Turn-Off Delay Time			4.4		
t <sub>f</sub>	Turn-Off Fall Time			22.2		

Notes : a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

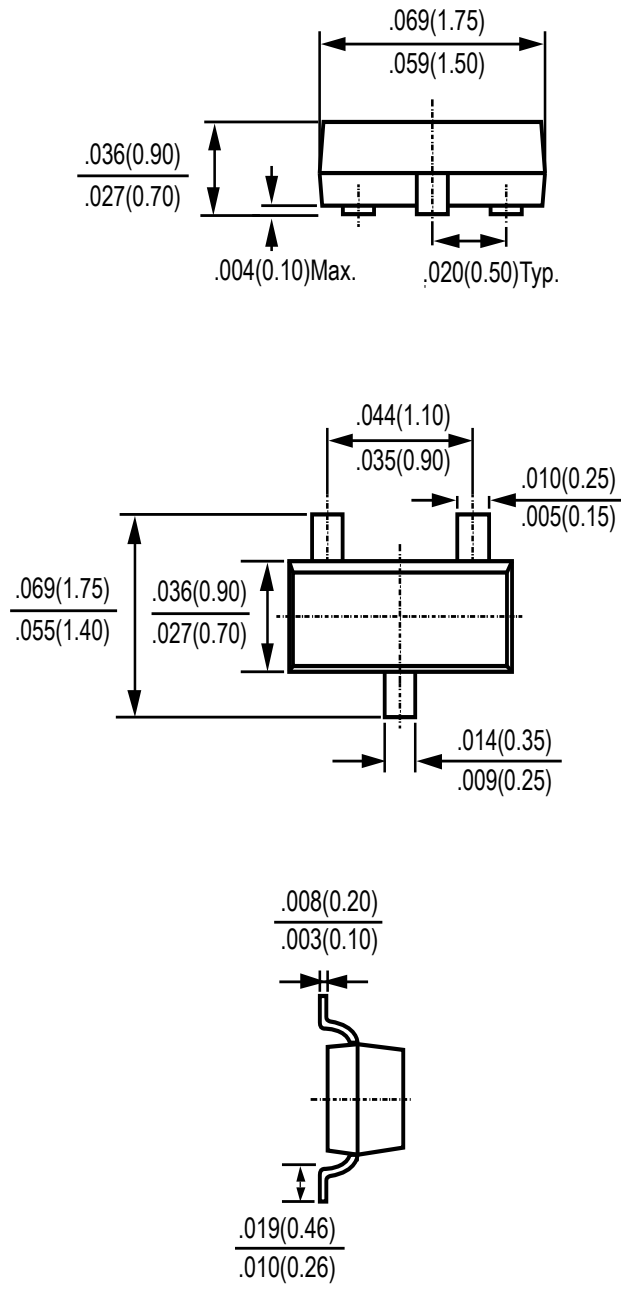
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics ( $T_J = 25^\circ\text{C}$  Noted)





*Package Outline Dimensions*



SOT-523

Dimensions in inches and (millimeters)

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