256Mb NAND FLASH

AFND5608U1 (/CE Don't Care mode)

Revision No.	History	Draft Date	Remark
Rev.00	Initial Draft	June. 2012	Preliminary
Rev. 01	- tCLS, tCS, tALS minimum values are added	Mar. 2013	
Rev.02	- Corrected TSOP Package Dimension	May. 2013	
Rev.03	- Add Industrial Temperature Option	Oct. 2013	
Rev.04	- Add 9mmx11mm 63ball BGA PKG option - Generate Industrial grade part no	Nov. 2013	

FEATURES SUMMARY

- **Power Supply**
  - -3.3V Device(AFND5608U1) 2.7V ~ 3.6V
- **Organization**
  - -Memory Cell Array : (32M + 1024K) x 8bits
  - -Data Register : (512 + 16) x 8bits
- **Automatic Program and Erase**
  - -Page Program : (512 + 16)Bytes
  - -Block Erase : (16K +512)Bytes
- **Page Read Operation**
  - -Page Size : (512 + 16)Bytes
  - -Random Access : 12us(Max.)
  - -Serial Page Access : 30ns(Min.)
- **Fast Write Cycle Time**
  - -Program time : 200us(Typ.)
  - -Block Erase time : 2ms(Typ.)
- **Copy-Back PROGRAM Operation**
  - -Fast Page copy without external buffering
- **Command Register Operation**
- **Security features**
  - -OTP area, 16Kbytes(32 pages)
- **Hardware Data Protection**
  - -Program / Erase locked during Power transitions
- **Data Integrity**
  - -Endurance : 100K Program / Erase Cycles (With 1bit/528byte ECC)
  - -Data Retention : 10 years
- **Package**
  - -AFND5608U1 : Pb-Free Package
  - 48-pin TSOP(12 x 20 / 0.5 mm pitch)
  - 48-Ball FBGA: 9.0 x 9.0 x 1.0mm
  - 63-Ball FBGA : 9.0 x 11.0 x 1.0mm
- **Operating Temperature**
  - Commercial : 0℃ ~70℃
  - Industrial : -40℃~ 85℃

Product Information

Part number	Voltage	Bus Width	Package
AFND5608U1-CKAK	2.7~3.6V	x8	12x20mm TSOP
AFND5608U1-CKCK			9x9mm FBGA
AFND5608U1-CKEK			9x11mm FBGA
AFND5608U1-CKAKI*			12x20mm TSOP
AFND5608U1-CKCKI			9x9mm FBGA
AFND5608U1-CKEKI			9x11mm FBGA

Note) I* : Industrial Grade

GENERAL DESCRIPTION

The AFND5608U1 is 256Mbit with spare 8Mbit capacity. The device is offered in 3.3V power supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market.

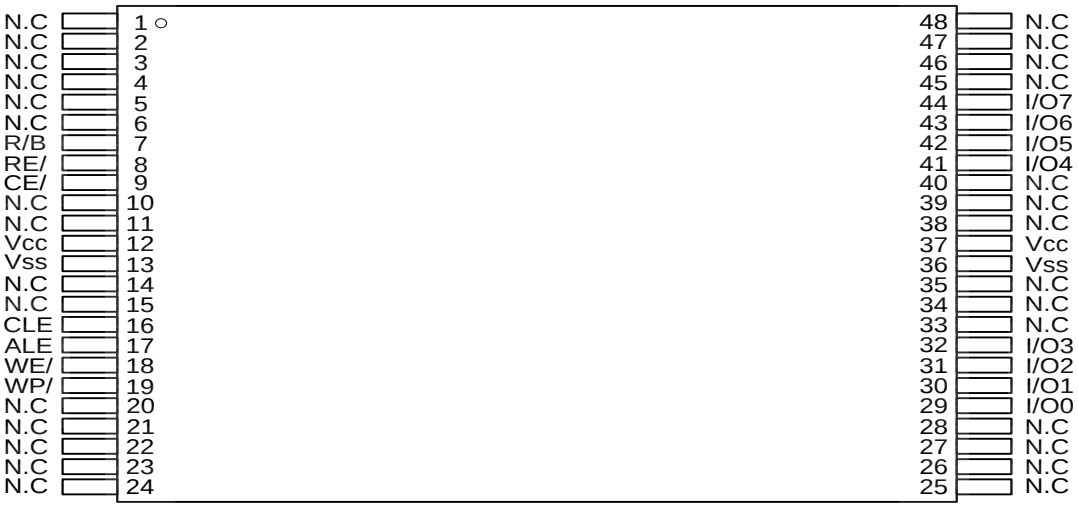
A program operation can be performed in typical 200us on the 528-bytes and an erase operation can be performed in typical 2ms on a 16K-bytes block. Data in the page can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. Command, data and address are synchronously introduced using /CE, /WE, ALE and CLE input pin. The output pin R/B(open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the AFND5608U1's extended reliability of 100K program / erase cycles by providing ECC(Error Correction Code) with real time mapping-out algorithm.

The chip could be offered with the /CE don't care function. This function allows the direct download of the code form the NAND flash memory device by a microcontroller, since the /CE transitions do not stop the read operation.

The copy back function allows the optimization of defective blocks management : when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Also, this device includes extra features like OTP area.

The AFND5608U1 is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

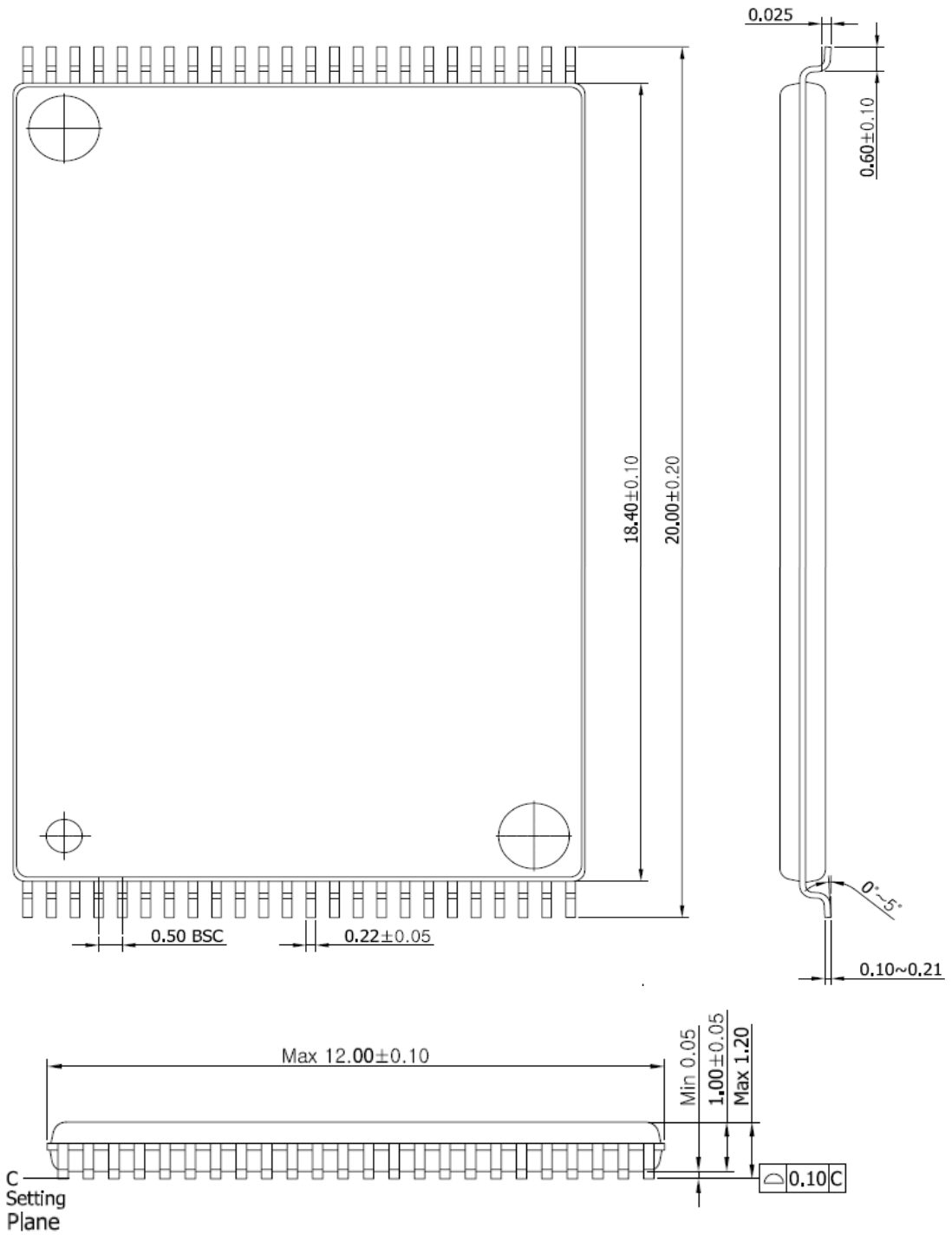
PIN CONFIGURATION (TSOP1)



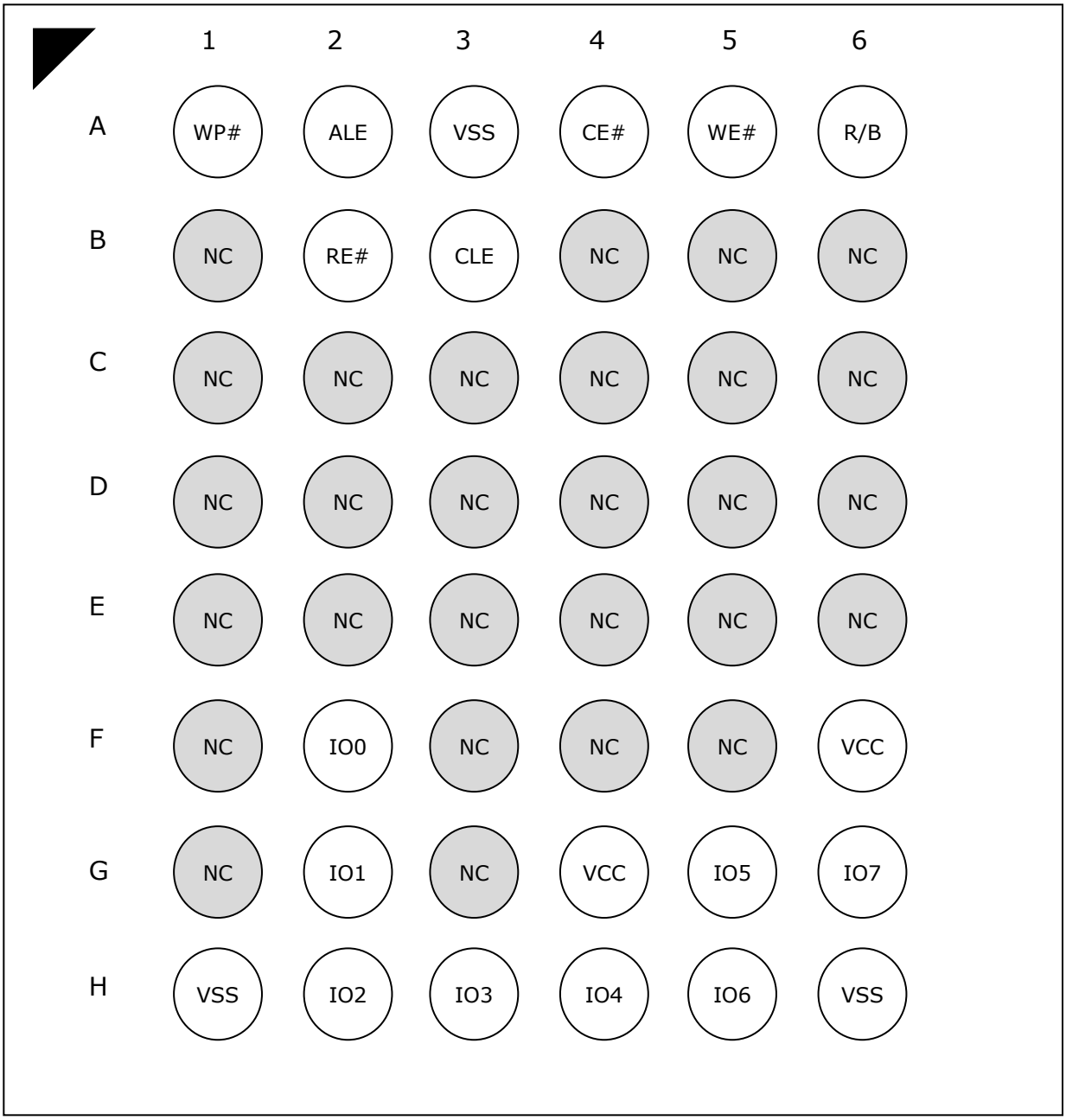
PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

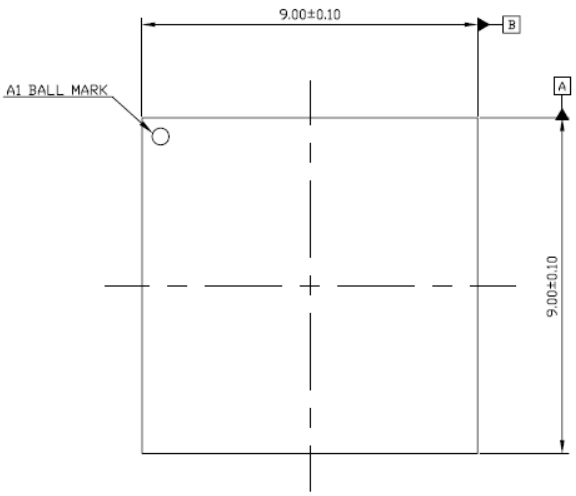
Dimensions in millimeters



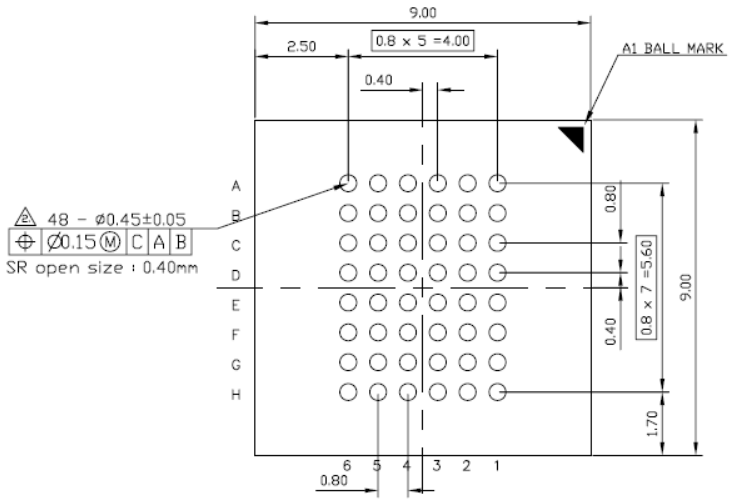
PIN CONFIGURATION (48ball-FBGA)



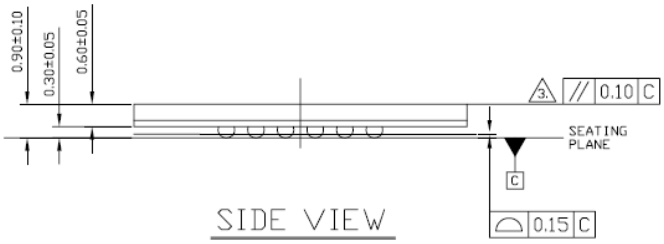
PACKAGE OUTLINE DRAWING (48ball-FBGA 9x9mm)



TOP VIEW



BOTTOM VIEW

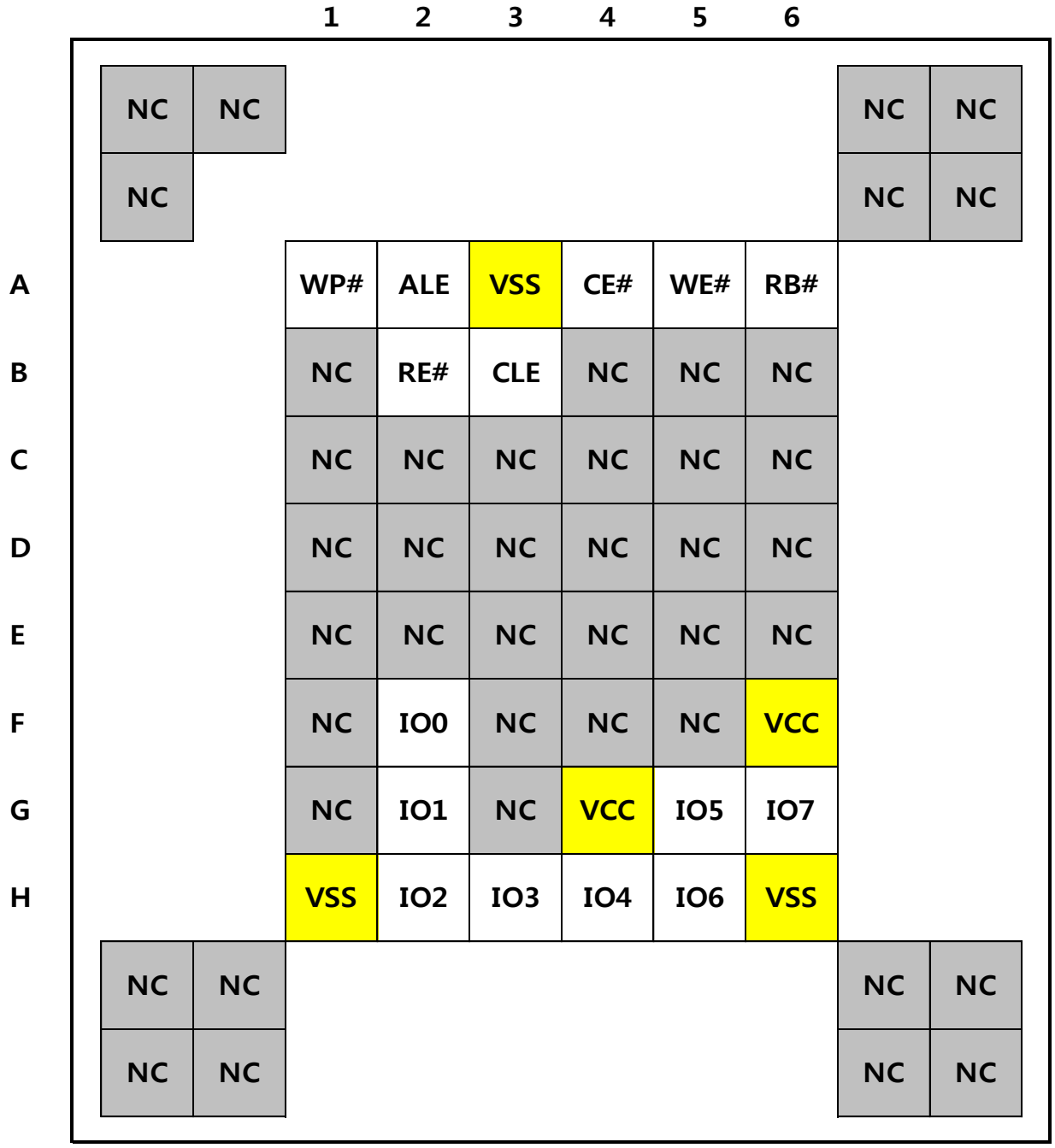


SIDE VIEW

Description
FBGA 48BALL
Dimension
9.0mm x 9.0mm x 0.90mm (Max. 1.0mm T)

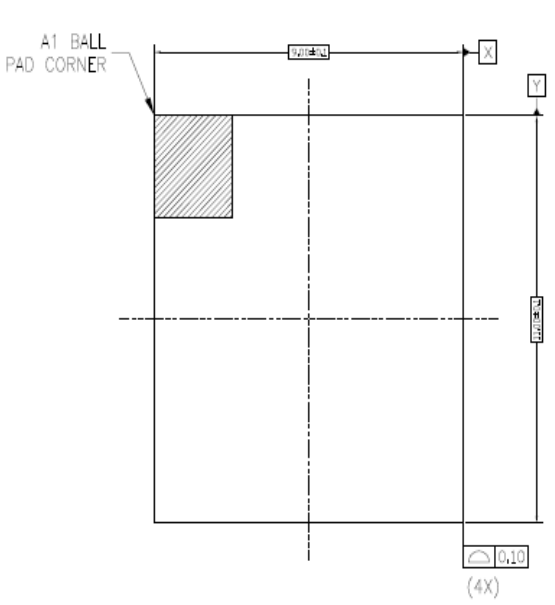
1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

PIN CONFIGURATION (63ball-FBGA)

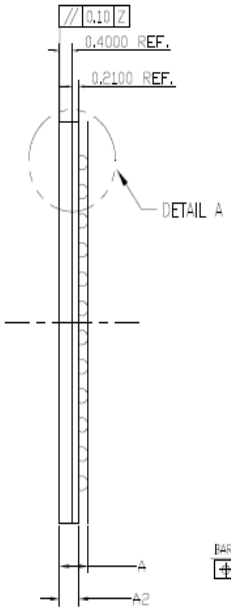


TOP VIEW

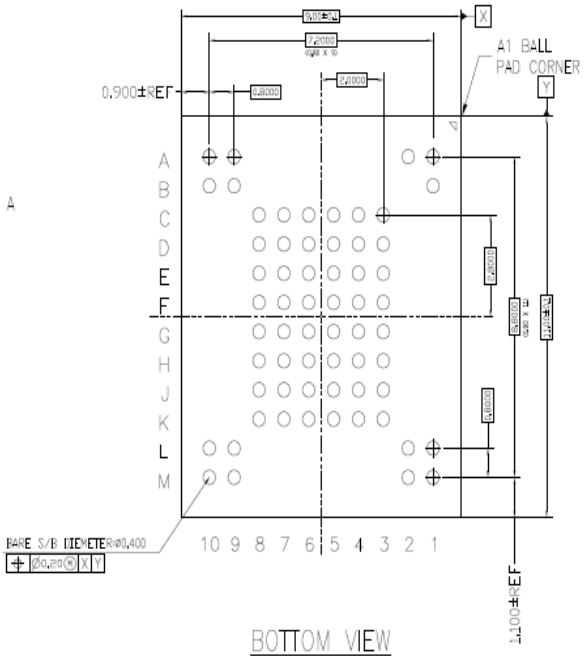
PACKAGE OUTLINE DRAWING (63ball-FBGA 9x11mm)



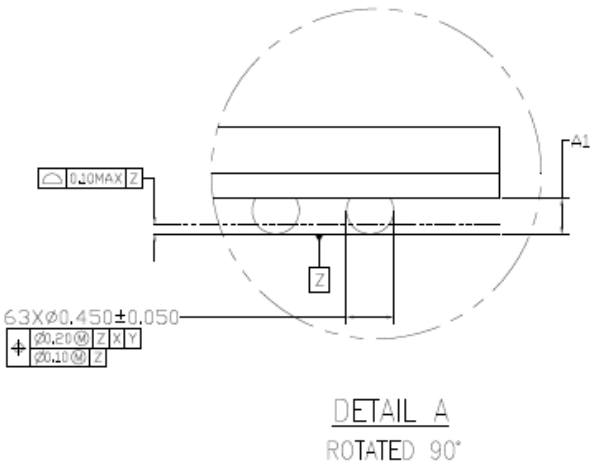
TOP VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL A
ROTATED 90°

Description
FBGA 63BALL
Dimension
9.0mm x 11.0mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the /WE signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of /WE with ALE high
/CE	**CHIP ENABLE** The /CE input is the device selection control. When the device is in the Busy state, /CE high is ignored, and the device does not return to standby mode in program or erase operation. Regarding /CE control during read operation, refer to 'Page Read' section of device operation.
/RE	**READ ENABLE** The /RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of /RE which also increments the internal column address counter by one.
/WE	**WRITE ENABLE** The /WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the /WE pulse.
/WP	**WRITE PROTECT** The /WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the /WP pin is active low.
R/B	**READY/BUSY OUTPUT** The R/B output indicates the status of the device operation. When low, it indicates that a program, erase of random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	**POWER** Vcc is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

Note : Connect all Vcc and Vss pins of each device to common power supply outputs
Do not leave Vcc or Vss disconnected.

Figure 1. AFND5608U1 FUNCTIONAL BLOCK DIAGRAM

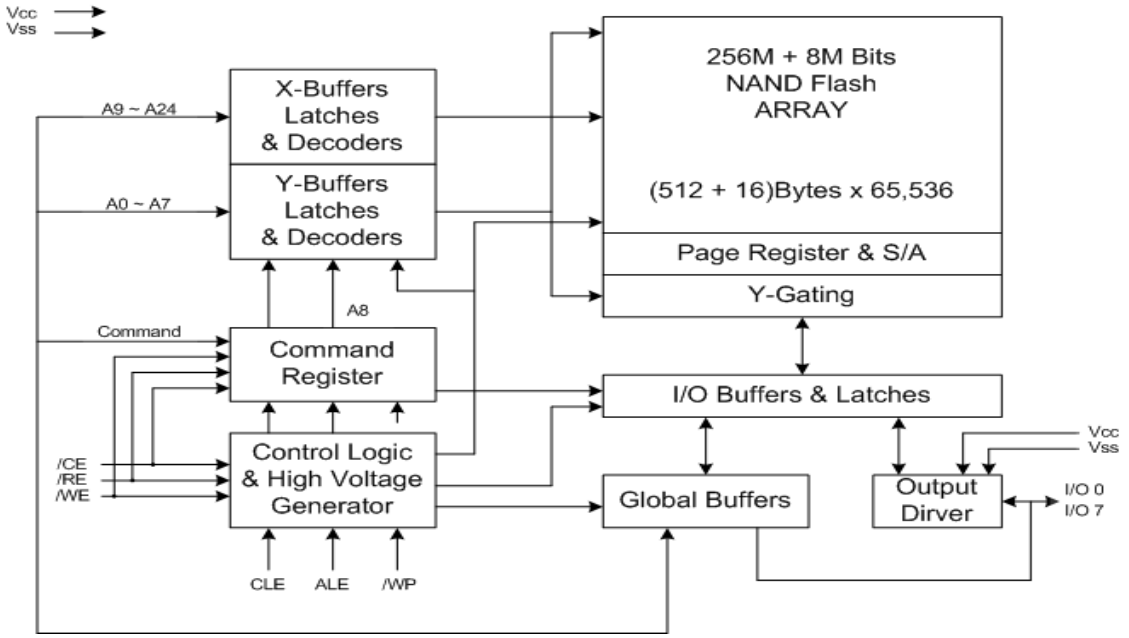
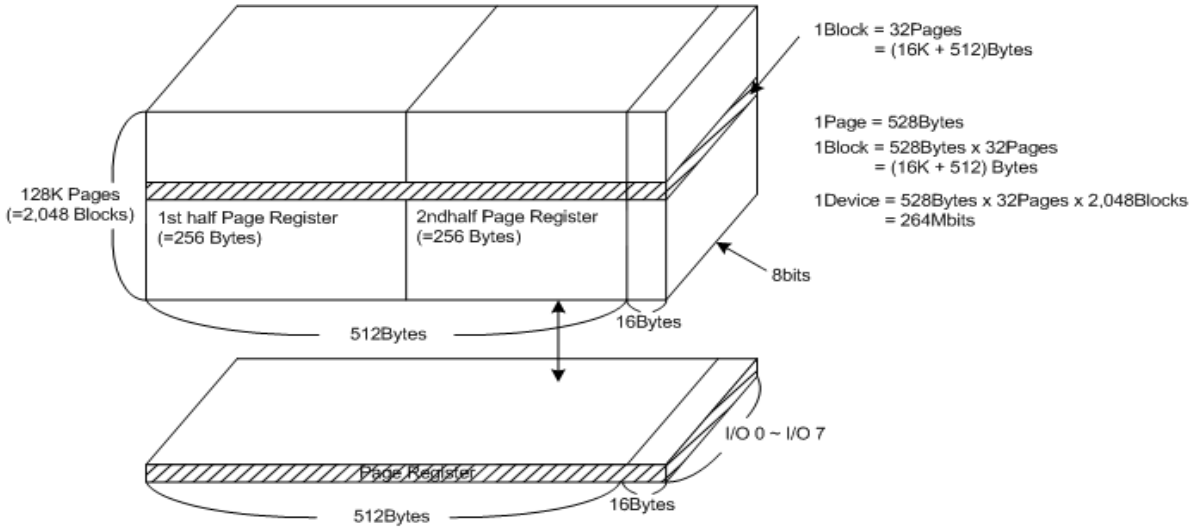


Figure 2. AFND5608U1 ARRAY ORGANIZATION



	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24

Column Address
Row Address
(Page Address)

NOTE : Column Address : Starting Address of the Register.
00h Command(Read) : Defines the starting address of the 1st half of the register.
01h Command(Read) : Defines the starting address of the 2nd half of the register.
* A8 is set to "Low" or "High" by the 00h or 01h Command.
* The device ignores any additional input of address cycles than required.

PRODUCT INTRODUCTION

The AFND5608U1 is a 264Mbits(276,824,064 bits) memory organized as 65,536 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-bytes data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists two NAND structures. A NAND structure consists of 16 cells. Total 135,168 NAND structures reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2,048 separately erasable 16K-bytes blocks. It indicates that the bit by bit erase operation is prohibited on the AFND5608U1.
The AFND5608U1 has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing /WE to low while /CE is low. Data is latched on the rising edge of /WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. The 32M byte physical space requires 24 addresses, thereby requiring three cycles for byte-level addressing : 1 cycle of column address, 2 cycles of row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however only the 2 cycles of row address are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the AFND5608U1.

Table 1. Command Sets

Function	1'st Cycle	2'nd Cycle	Acceptable Command During Busy
Read 1	00h/01h(1)	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	o
Page Program	80h	10h	
Copy Back Program	00h	8Ah	
Block Erase	60h	D0h	
Read Status	70h	-	o

NOTE : Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	Vcc	-0.6 to + 4.6	V
	VIN	-0.6 to + 4.6	
	VI/O	-0.6 to +4.6	
Temperature Under Bias	TBIAS	-50 to + 125	°C
Storage Temperature	TSTG	-65 to + 150	°C

NOTE :

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to –
   2.0V for periods<20ns.
   Maximum DC voltage on input/output pins is VCC+0.3V which, during transition, may overshoot to VCC+0.2V for periods < 20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded. Functional operation
   should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to
   absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, AFND5608U1-CX : T_A = 0 to 70℃, AFND5608U1-IX : T_A = -40 to 85℃)

Parameter	Symbol	3.3V			Unit
		Min	Typ	Max	
Supply Voltage	Vcc	2.7	3.3	3.6	V
	Vss	0	0	0	V

DC AND OPERATING CHARACTERISTICS

Parameter		Symbol	Test Conditions	3.3V			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	ICC1	tRC=30ns, /CE=VIL, Iout=0mA	-	10	20	mA
	Program	ICC2		-	10	20	
	Erase	ICC3		-	10	20	
Standby Current(TTL)		ISB1	/CE-VIH, /WP=0V/Vcc	-	-	1	
Standby Current(CMOS)		ISB2	/CE=Vcc-0.2, /WP=0V/Vcc	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc(max)	-	-	±10	
Output Leakage Current		ILO	Vout=0 to Vcc(max)	-	-	±10	
Input High Volgate		VIH	-	0.8*VCC	-	Vcc +0.3	V
Input Low Voltage, All inputs		VIL	-	-0.3	-	0.2*VCC	
Output High Voltage Level		VOH	AFND5608U1 : IOH = -400uA	2.4	-	-	
Output Low Voltage Level		VOL	AFND5608U1 : IOL = 2.1mA	-	-	0.4	
Output Low Current(R/B)		IOL (R/B)	VOL=0.4V	8	10	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	NVB	2,008	-	2,048	Blocks

Note :

1. The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528Byte ECC.
3. Minimum 1,004 valid blocks are guaranteed for each contiguous 128Mb memory space.

AC TEST CONDITION

(AFND5608U1-CX : T_A = 0 to 70℃, AFND5608U1-IX : T_A = -40 to 85℃)

Parameter	Value
	AFND5608U1(3.3V)
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL GATE and CL=100pF

CAPACITANCE (Temp=25℃, Vcc=3.3V, f=1.0Mhz)

Item	Symbol	Test Condition	Min	Typ	Max
Input/Output Capacitance	CI/O	VIL=0V	-	10	pF
Input Capacitance	CIN	VIN=0V	-	10	pF

NOTE: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	/CE	/WE	/RE	/WP	Mode	
H	L	L	↑edge	H	X	Read Mode	Command Input
L	H	L	↑edge	H	X		Address Input(3 clocks)
H	L	L	↑edge	H	H	Write Mode	Command Input
L	H	L	↑edge	H	H		Address Input(3 clocks)
L	L	L	↑edge	H	H	Data Input	
L	L	L	H	↓edge	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc(1)	Standby	

Note : 1. /WP should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		tPROG	-	200	500	us
Number of Partial Program Cycles in the same page	Main Array	Nop	-	-	2	Cycle
	Spare Array		-	-	3	Cycle
Block Erase Time		tVERS	-	2	3	ms

AC TIMING CAHARACTERISTICS FOR COMMAND / ADDRESS / DATA INPUT

Parameter	Symbol	Min	Max	Unit
CLE setup Time	tCLS	25	-	ns
CLE Hold Time	tCLH	10	-	ns
/CE setup Time	tCS	25	-	ns
/CE Hold Time	tCH	10	-	ns
/WE Pulse Width	tWP(1)	15	-	ns
ALE setup Time	tALS	25	-	ns
ALE Hold Time	tALH	10	-	ns
Data setup Time	tDS	10	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	30	-	ns
/WE High Hold Time	tWH	10	-	ns
Address to Data Loading Time	tADL	100	-	ns

Note : 1. If tCS is set less than 10ns, tWP must be minimum 25ns, otherwise, tWP may be minimum 15ns.

AC CAHARACTERISTICS FOR OPERATION

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	12	us
ALE to /RE Delay	tAR	10	-	ns
CLE to /RE Delay	tCLR	10	-	ns
Ready to /RE Low	tRR	20	-	ns
RE Pulse Width	tRP/ tRPB	15	-	ns
WE High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	30	-	ns
/RE Access Time	tREA/ tREAB	-	18	ns
/CE Access Time	tCEA	-	23	ns
/RE High to Output Hi-Z	tRHZ	-	30	ns
/CE High to Output Hi-Z	tCHZ	-	20	ns
/CE High to ALE or CLE Don't Care	tCSD	10	-	ns
/RE or /CE High to Output hold	tOH	15	-	ns
/RE High Hold Time	tREH	10	-	ns
Output Hi-Z to /RE Low	tIR	0	-	ns
/WE High to /RE Low	tWHR	50	-	ns
Device resetting time(Read/Program/Erase)	tRST	-	5/10/500(1)	us

Parameter	Symbol	Min	Max	Unit
Last /RE High to Busy(at sequential read)	tRB	-	100	ns
/CE High to Ready(in case of interception by /CE at read)	tCRY	-	50+tr(R/B)	ns
/CE High Hold Time(at the last serial read)(2)	tCEH	100	-	ns

Note : 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. The time to Ready depends on the value of the pull-up resistor tied R/B pin.

NAND FLASH TECHNICAL NOTES

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ATO. The information regarding the initial invalid block(s) is so called as the initial invalid block information.

Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528Byte ECC.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 6th byte in the spare area. ATO makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 517. Since the initial invalid block Information is also erasable in most cases, it is impossible to recover the information once it has been erased.

Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure3). Any intentional erasure of the Initial invalid block information is prohibited.

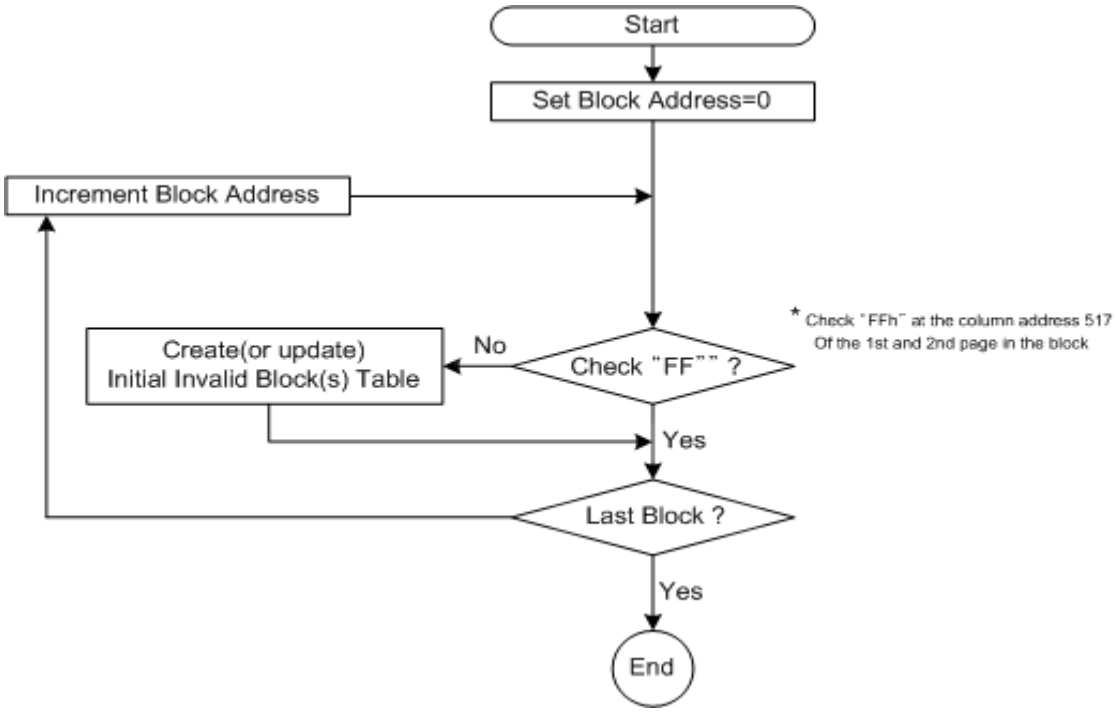


Figure 3. Flow chart to create initial invalid block table

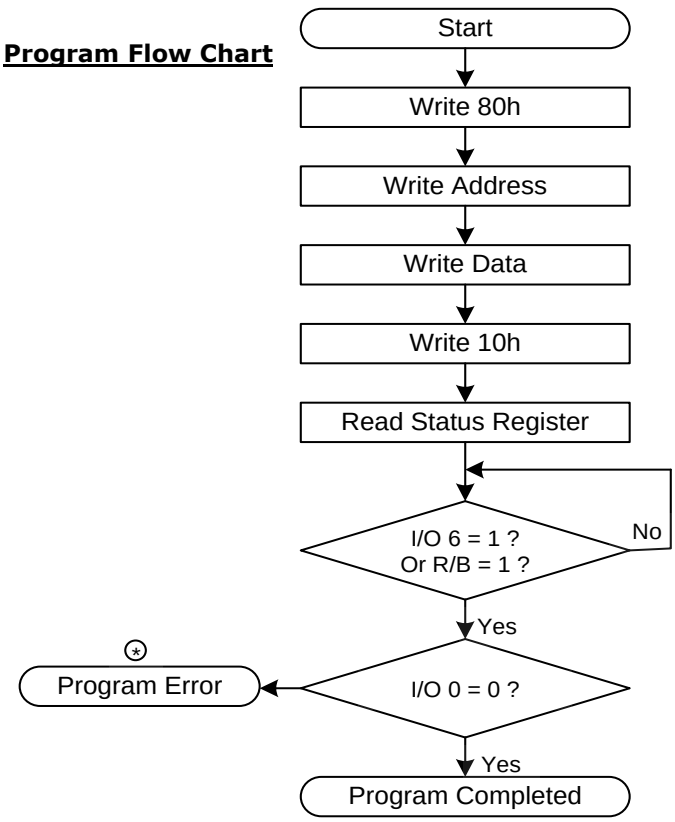
Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the block failure rate. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read failure due to single bit error should be reclaimed by ECC without any block replacement. The block failure rate in the qualification report does not include those reclaimed blocks

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase → Block Replacement
	Program Failure	Status Read after Program → Block Replacement
Read	Single Bit Failue	Verify ECC → ECC Correction

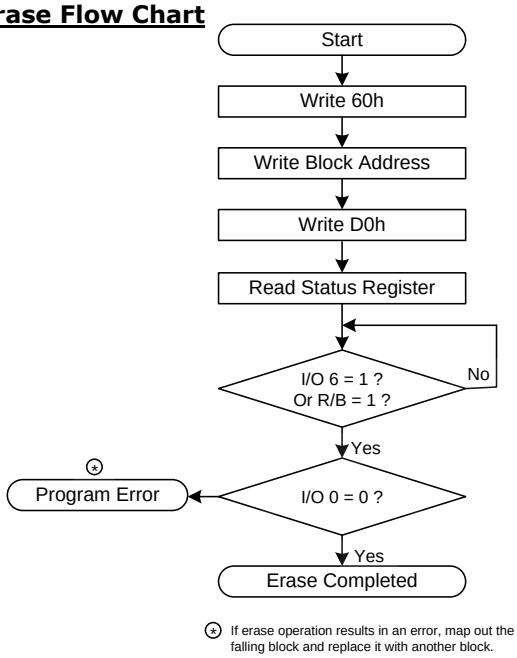
ECC : Error Correcting Code → Hamming Code etc. (Example : 1bit Correction & 2bits detection)

Program Flow Chart



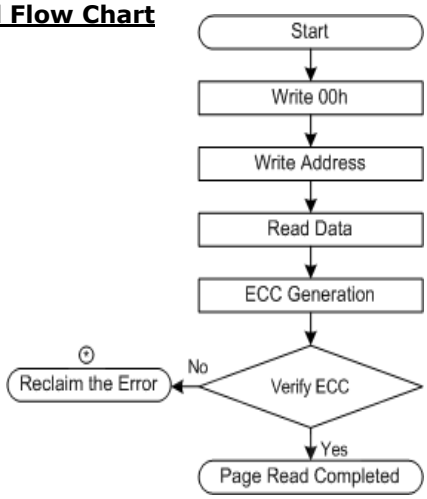
⊛ If program operation results in an errors, map out the Block including the page in error and copy the target Data to another block.

Erase Flow Chart

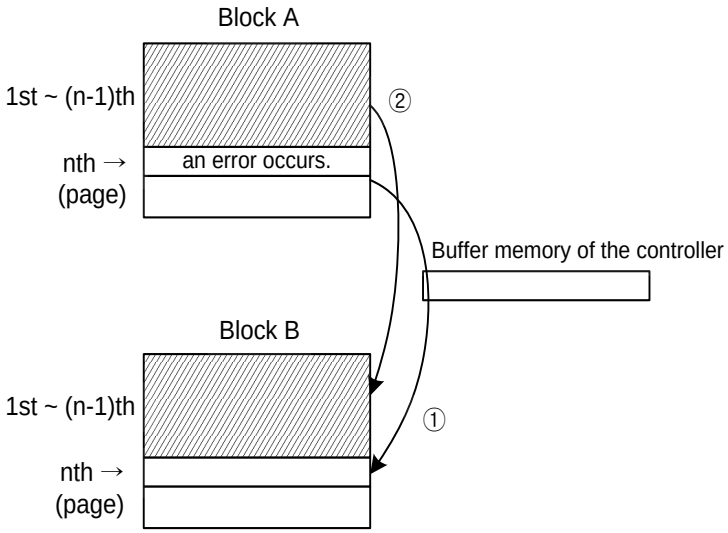


⊛ If erase operation results in an error, map out the falling block and replace it with another block.

Read Flow Chart



Block Replacement



* Step1. When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2. Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block (Block 'B)
* Step3. Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'
* Step4. Do not further erase Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

Pointer Operation of AFND5608U1

ATO NAND Flash has three address pointer commands as a substitute for the two most significant column address. '00h' Command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power-up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written

Table 2. Destination of the pointer

Command	Pointer Position	Area
00h	0~256byte	1st half array(A)
01h	256~511byte	2nd half array(B)
50h	512~527byte	Spare array(C)

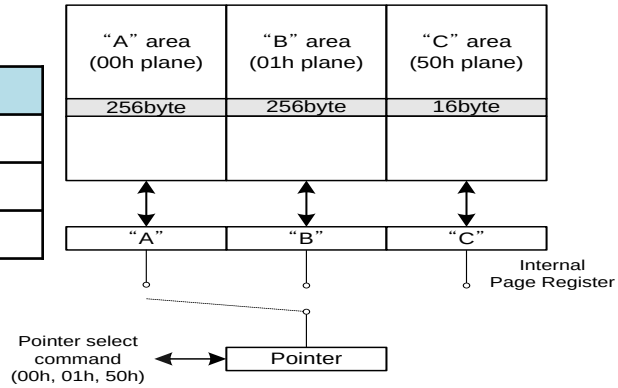
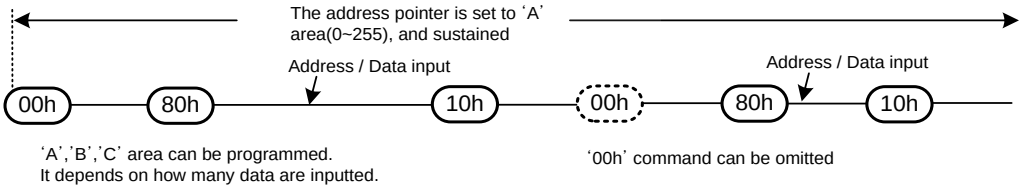
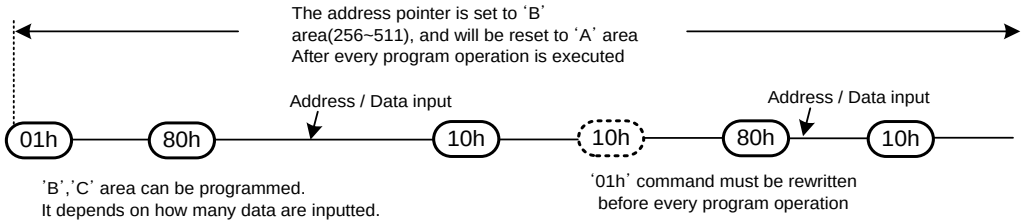


Figure 4. Block Diagram of Pointer Operation

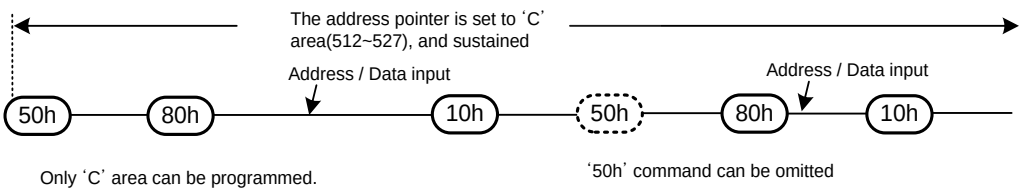
(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



(3) Command input sequence for programming 'C' area



System Interface Using /CE don't-care

For an easier system interface, /CE may be inactive during the data-loading or sequential data-reading as shown below. The internal 528bytes page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating /CE during the data-loading and reading would provide significant savings in power consumption.

Figure 5. Program Operation with /CE don't care

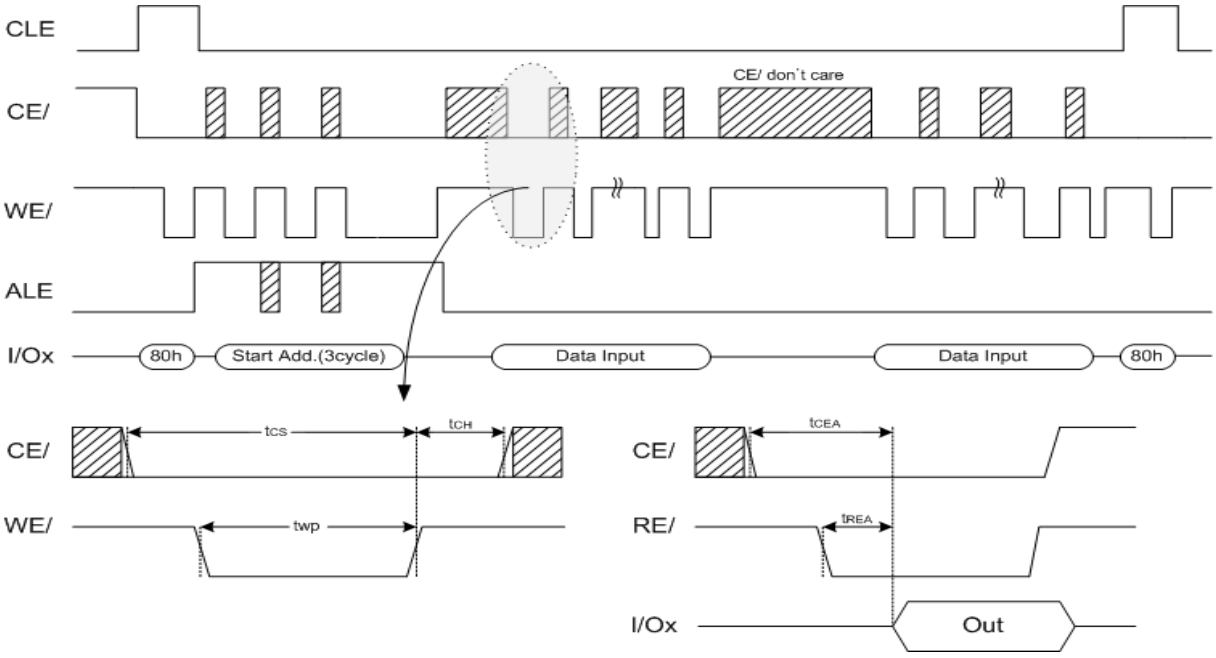
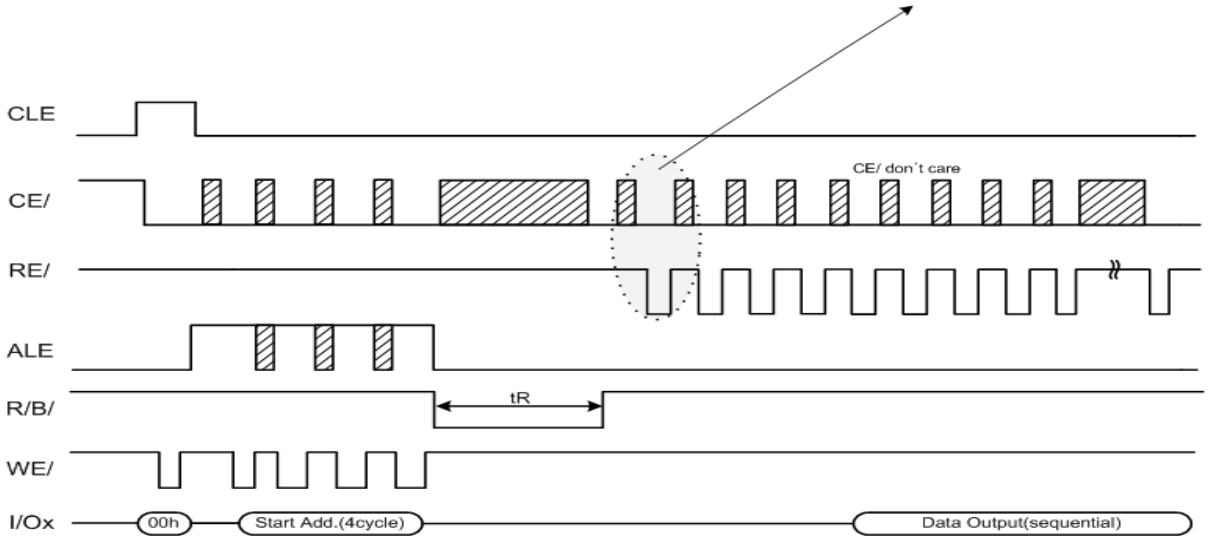
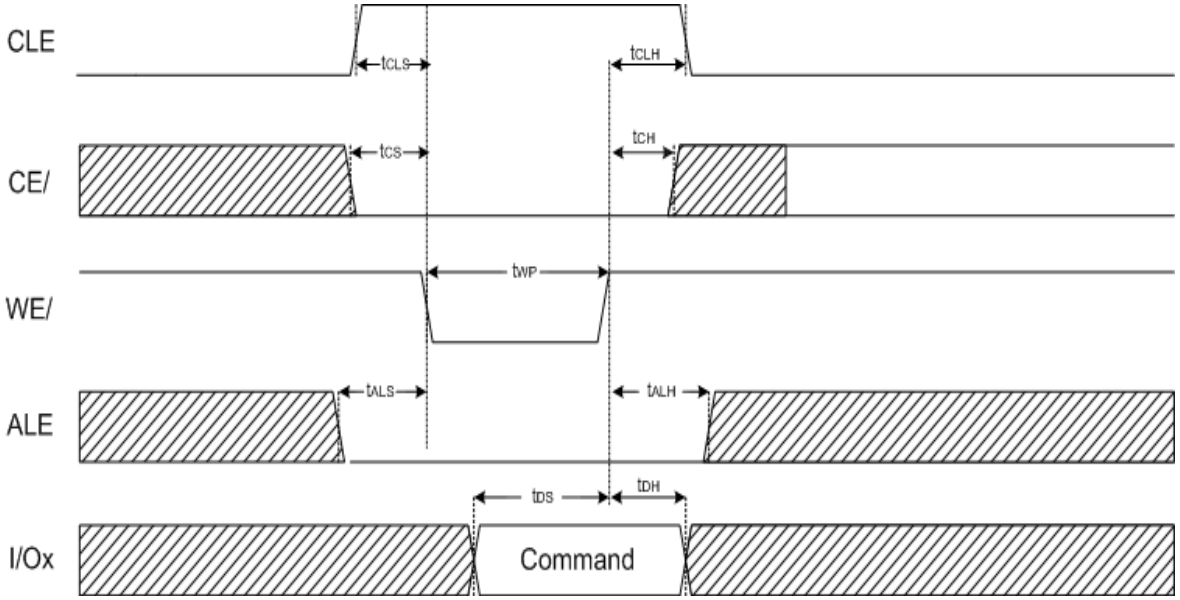


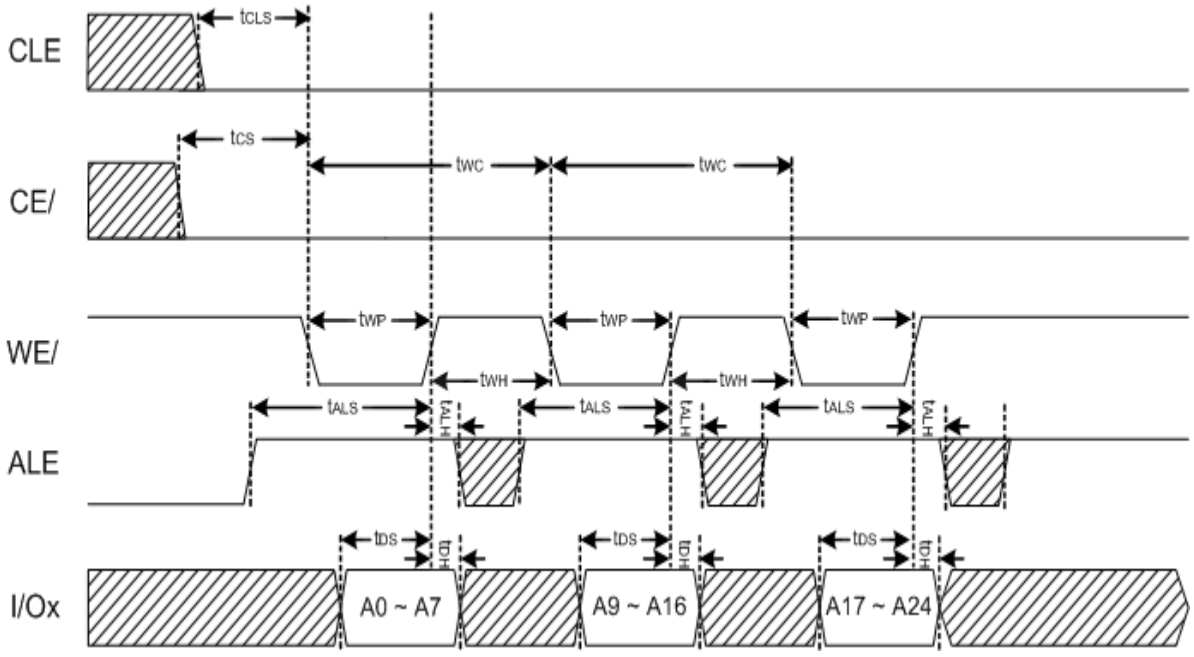
Figure 6. Read Operation with /CE don't-care



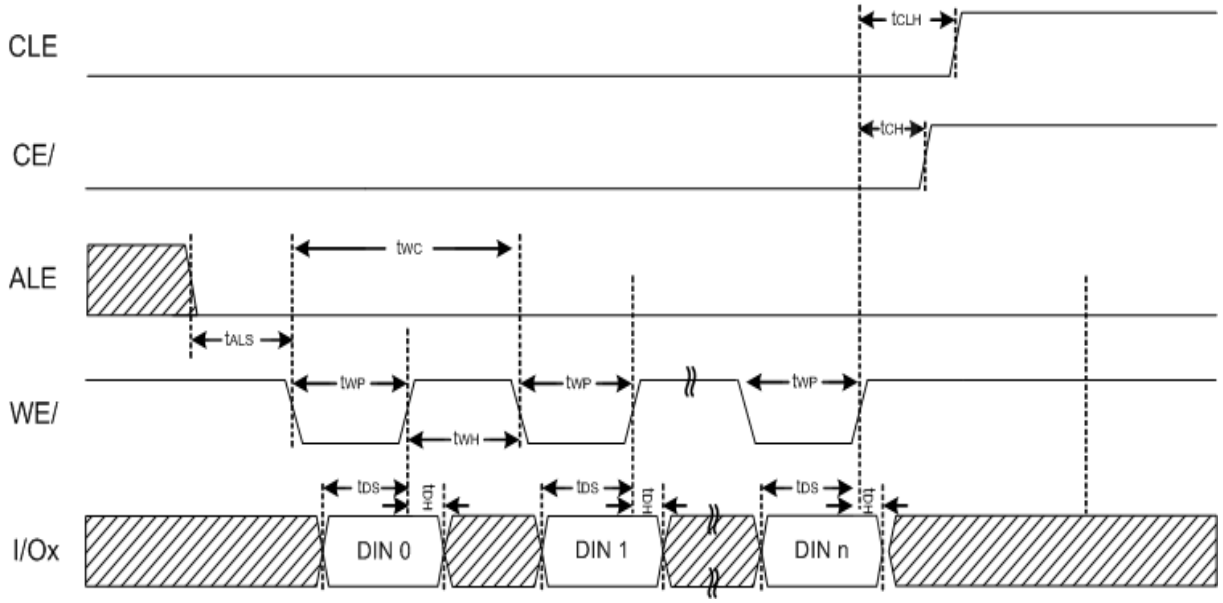
*** Command Latch Cycle**



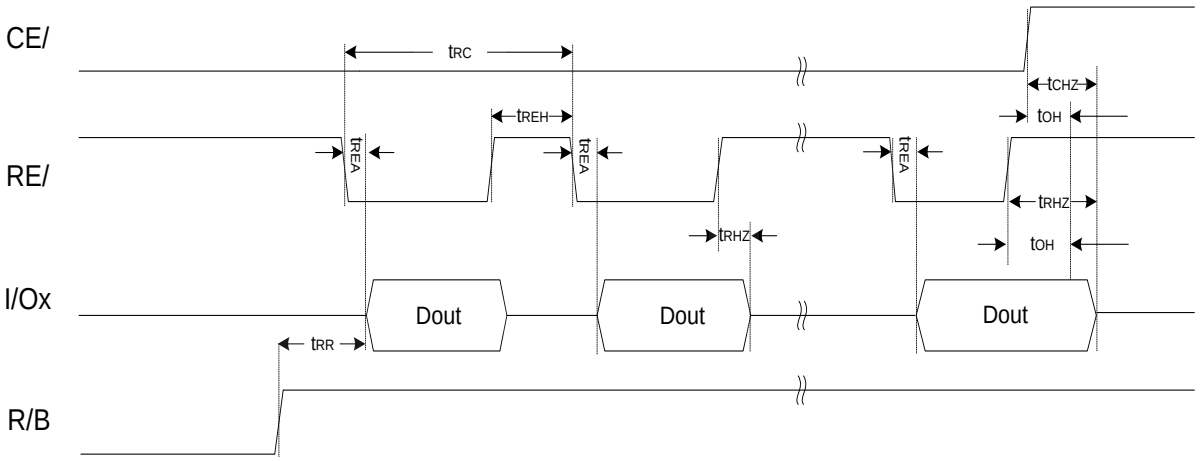
*** Address Latch Cycle**



*** Input Data Latch Cycle**

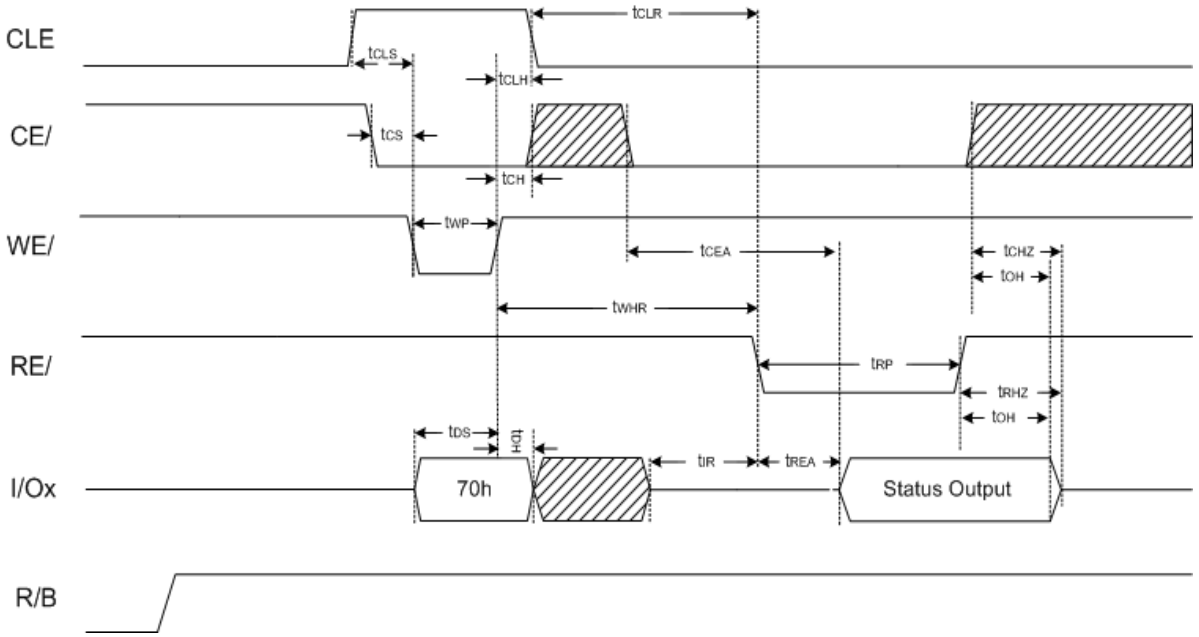


*** Sequential Out Cycle after Read(CLE=L, /WE=H, ALE=L)**

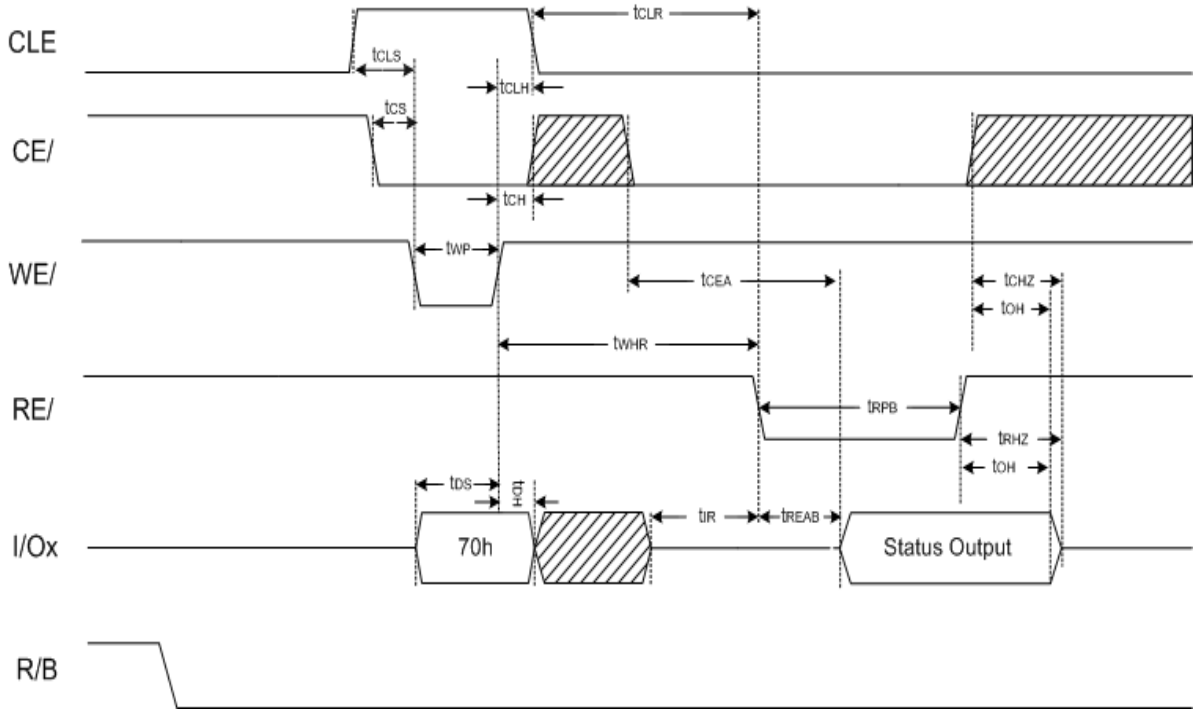


Note : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

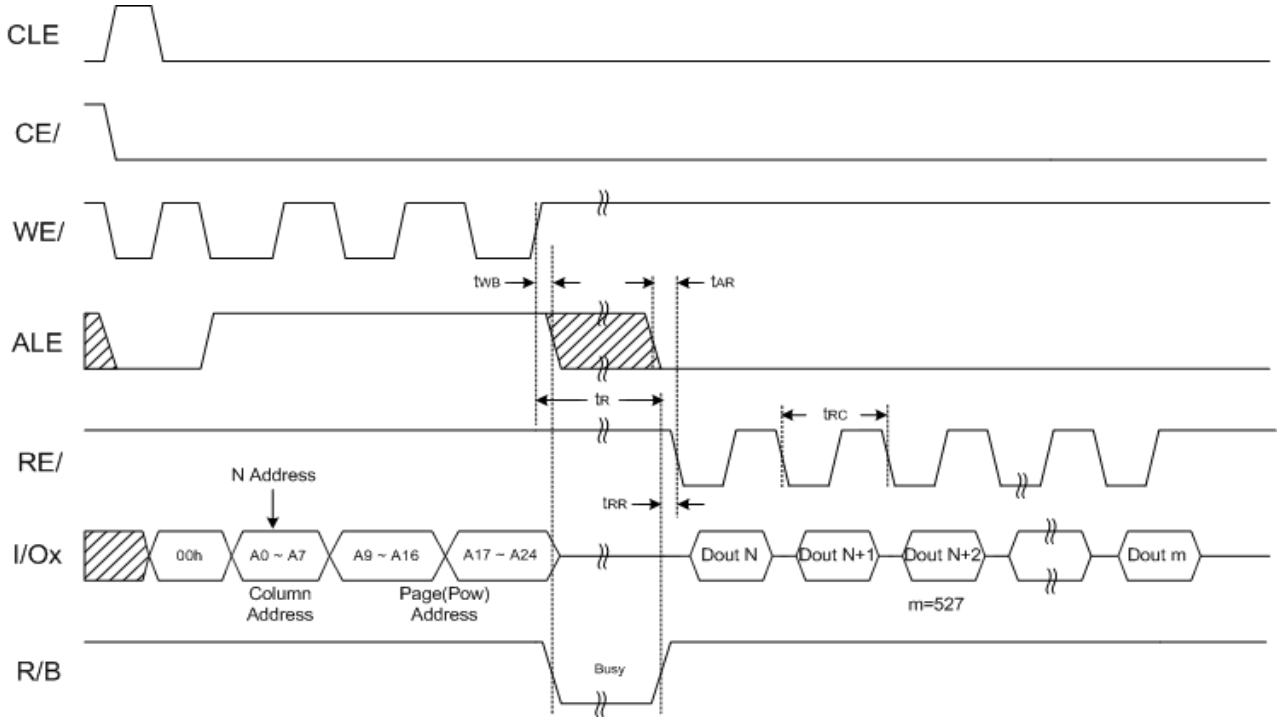
*** Status Read Cycle (During Ready State)**



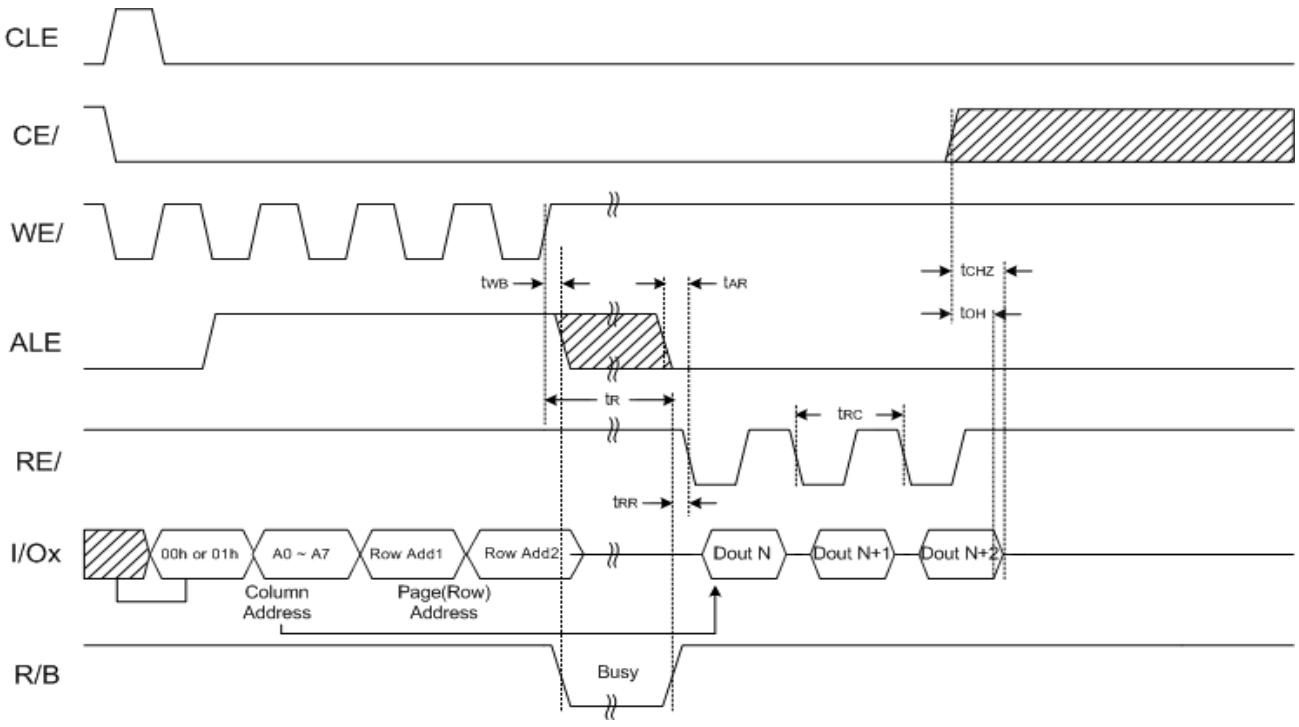
*** Status Read Cycle (During Busy State)**



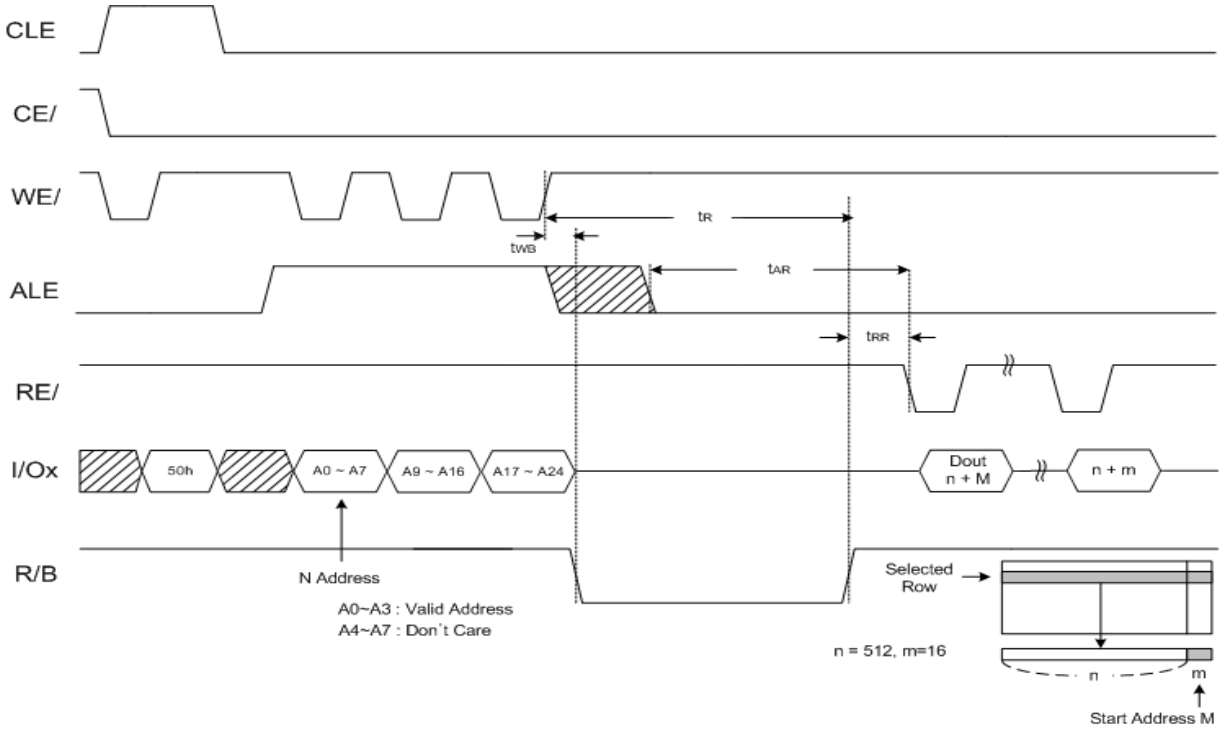
*** READ1 OPERATION (READ ONE PAGE)**



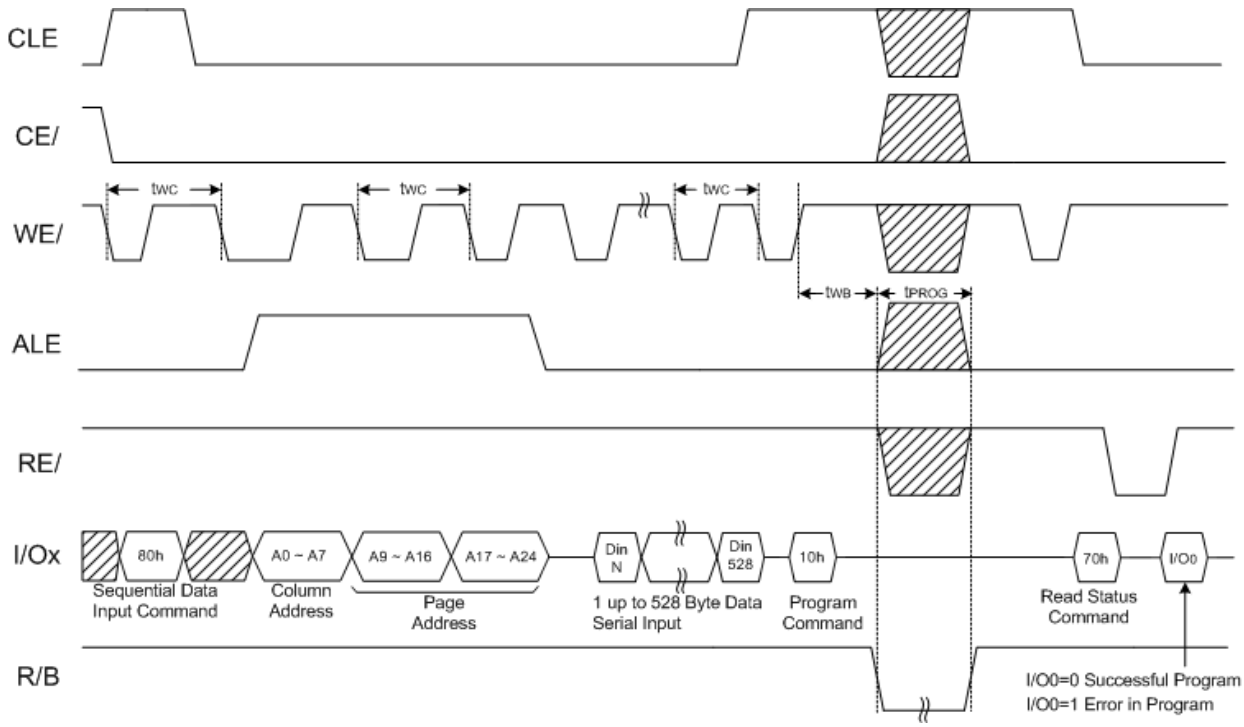
*** READ1 Operation (Intercepted by /CE)**



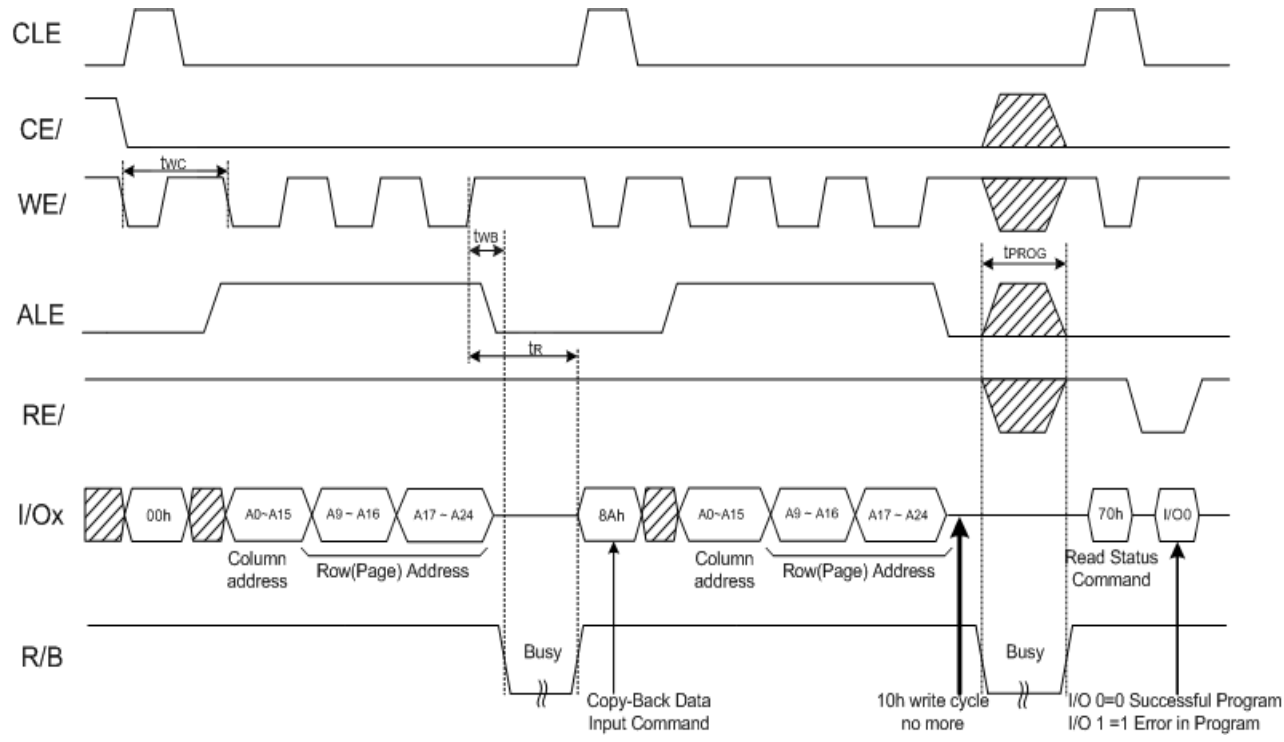
*** READ2 Operation (Read One Page)**



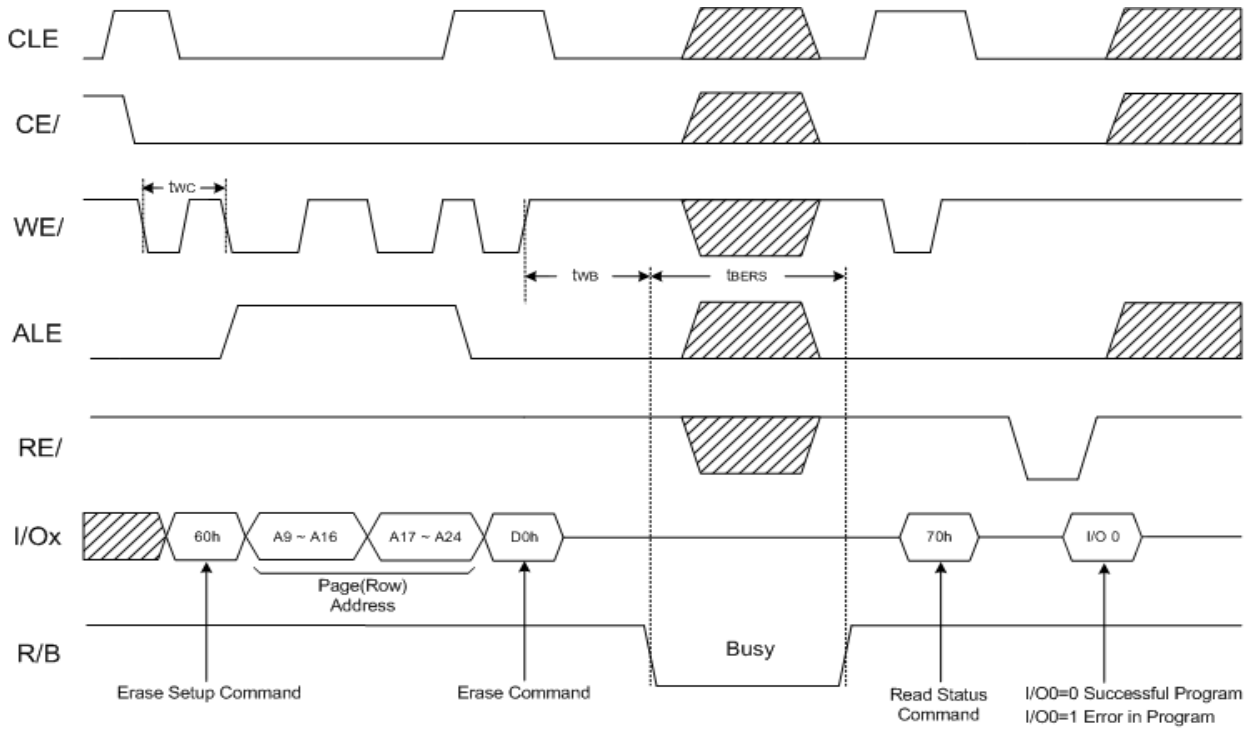
*** Page Program Operation**



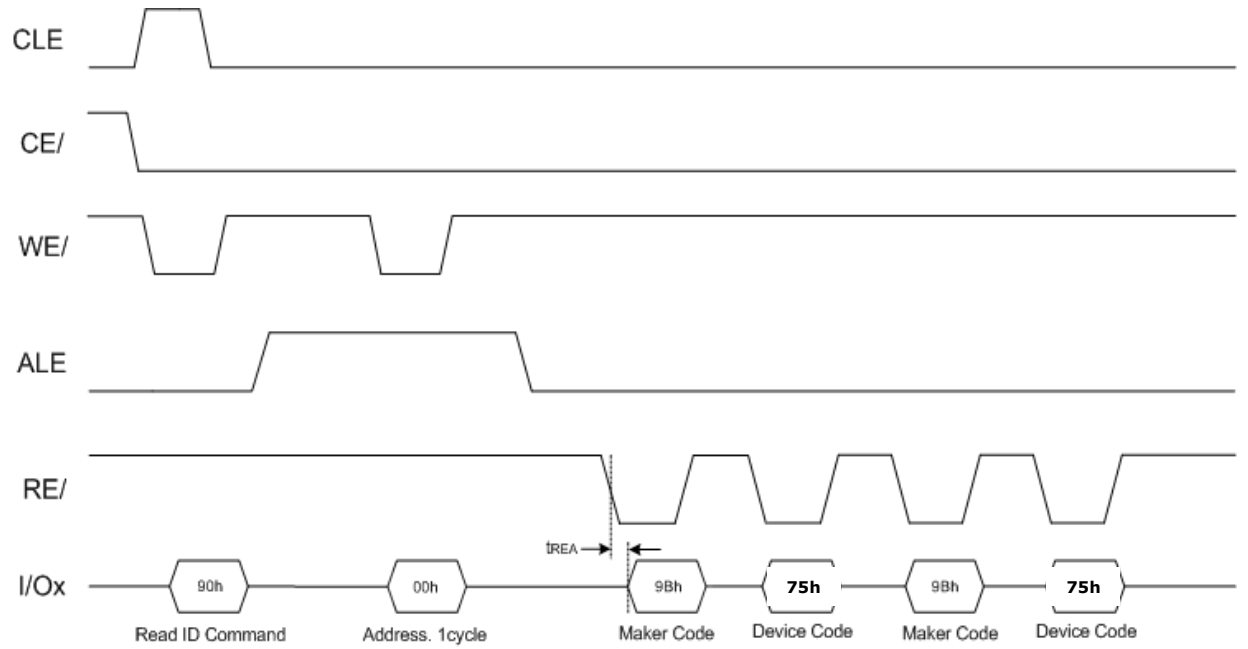
*** Copy-Back Program Operation**



*** Block Erase Operation (Erase One Block)**



*** Read ID Operation**



ID DEFINITION TABLE

90 ID : Access command =90h

	Value	Description
1st byte	9Bh	Maker Code
2nd byte	75h	Device Code

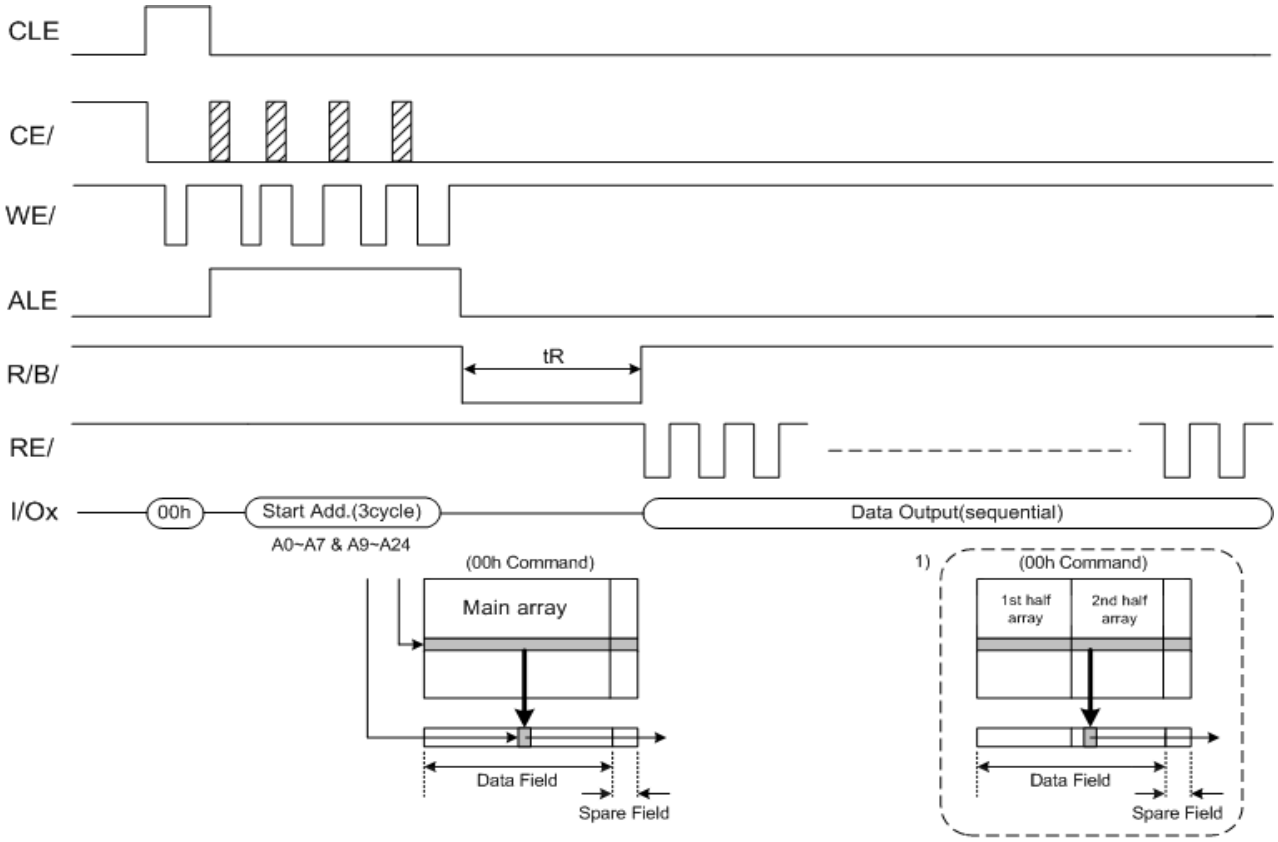
DEVICE OPERATION

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read. The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 12us(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. /CE must be held low while in busy for AFND5608U1, while /CE is don't care with AFND5608U1. If /CE goes high before the device returns to Ready, the random read operation is interrupted and Busy returns to Ready as the defined by tCRY. Since the operation was aborted, the serial page read does not output valid data. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing /RE, high to low transitions of the /RE clock output the data stating from the selected column address up to the last column address.

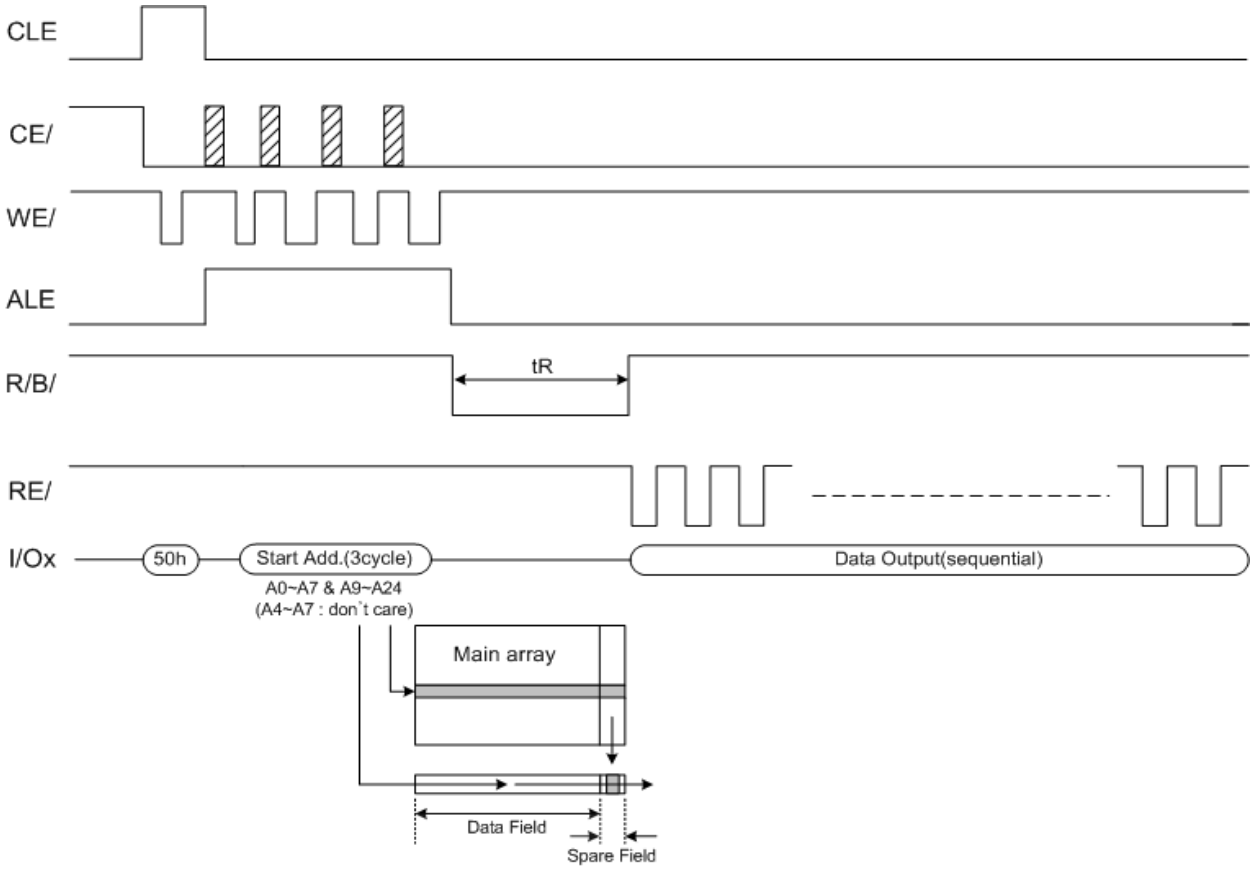
The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of 512 to 527 bytes may be selectively accessed by writing the Read2 command. Address A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figure 7 to 10 show typical sequence and timings for each read operation.

Figure 7. Read1 Operation



NOTE: 1) After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array(00h) at next cycle.

Figure 8. Read2 Operation

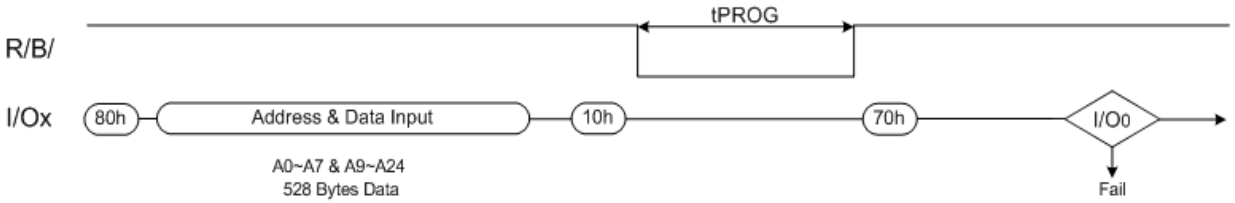


PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528 bytes, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with /RE and /CE low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Status Bit(I/O 0) may be checked(Figure 11). The internal program verify detects only errors for "1" s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 9. Program Operation

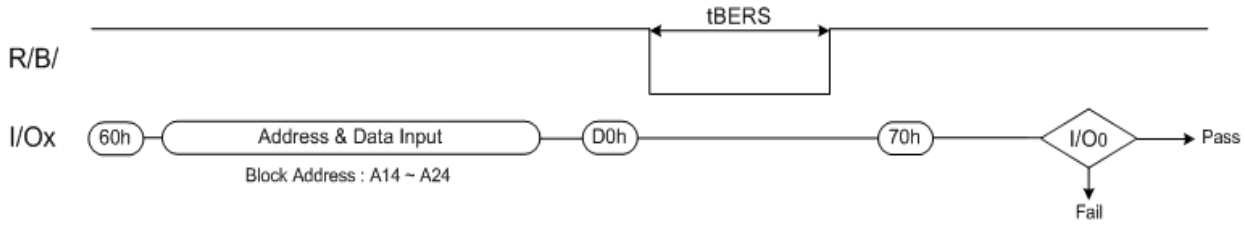


BLOCK ERASE

The Erase operation is done on block(16K Bytes) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A14 to A24 is valid while A9 to A13 ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of /WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Status Bit(I/O 0) may be checked.

Figure 12 details the sequence.

Figure 10. Block Erase Operation

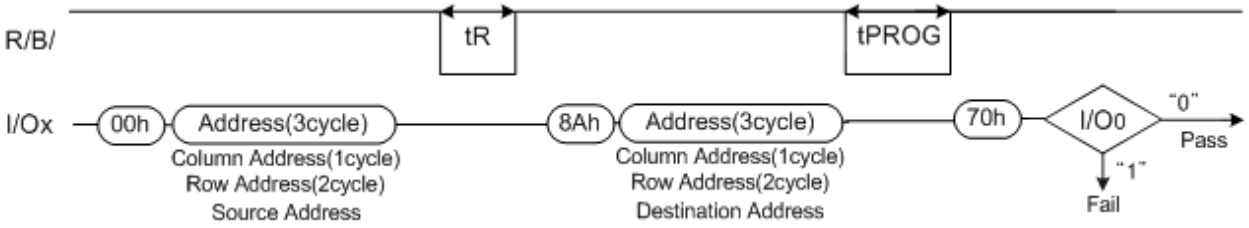


Copy-Back Program

The Copy-back program is provided to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without using an external memory. Since the time-consuming sequential-reading and its reloading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528bytes data into the internal buffer. As soon as the device returns to Ready state, Page-Copy data-input command(8Ah) with the address cycles of destination page followed may be written. The Program Confirm command(10h) is not needed to actually begin the programming operation. For backward-compatibility, issuing Program Confirm command during copy-back does not affect correct device operation.

Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Plane address must be the same between source and target page

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of /CE or /RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wried. /RE or /CE does not need to be toggled for updated status. Refer to table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

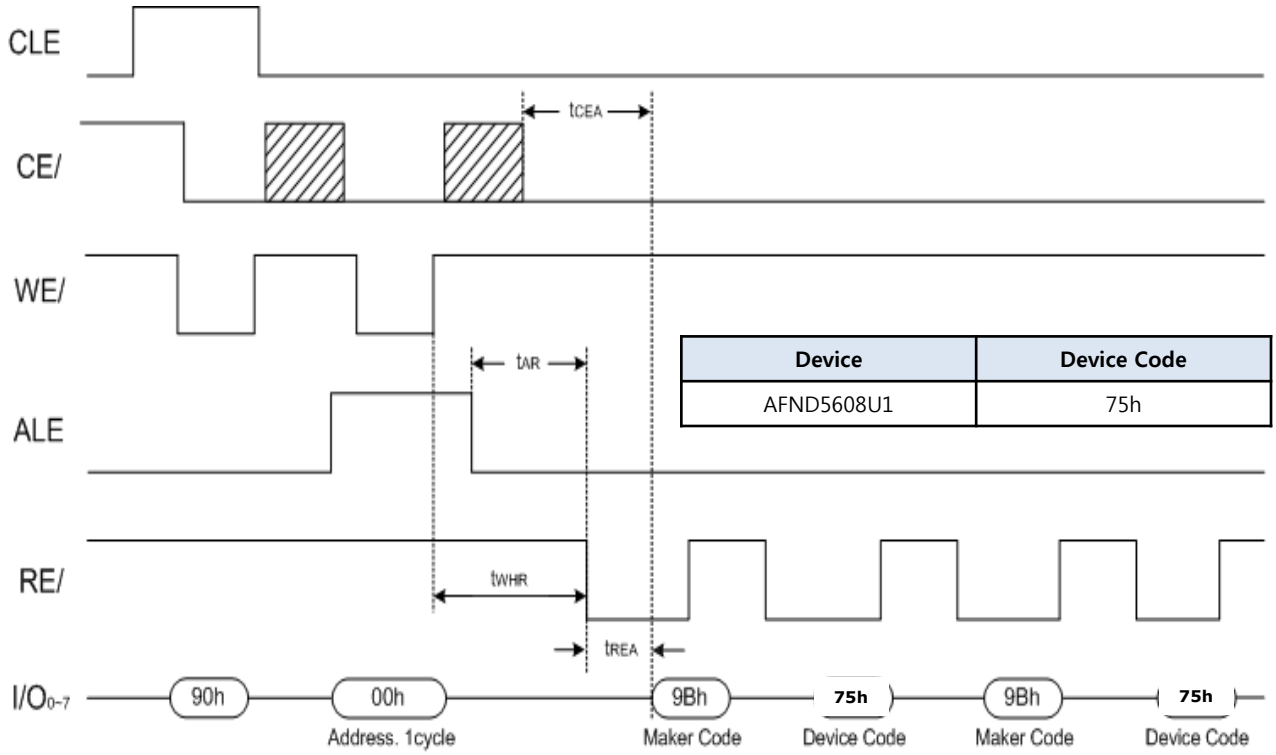
Table 3. Read Status Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase "1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	Busy : "0" Ready : "1"
I/O 7	Write Protect	Protected : "0" Not protect : "1"

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register followed by and address input of 00h. Two read cycles sequentially output the manufacturer code(9Bh), and the device code respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 13 shows the operation sequence.

Figure 11. READ ID Operation



Device	Device Code
AFND5608U1	75h

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when /WP is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written. Refer to Figure 14 bellow.

Figure 12. RESET Operation

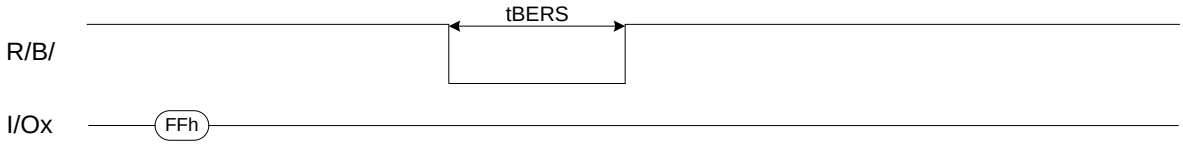


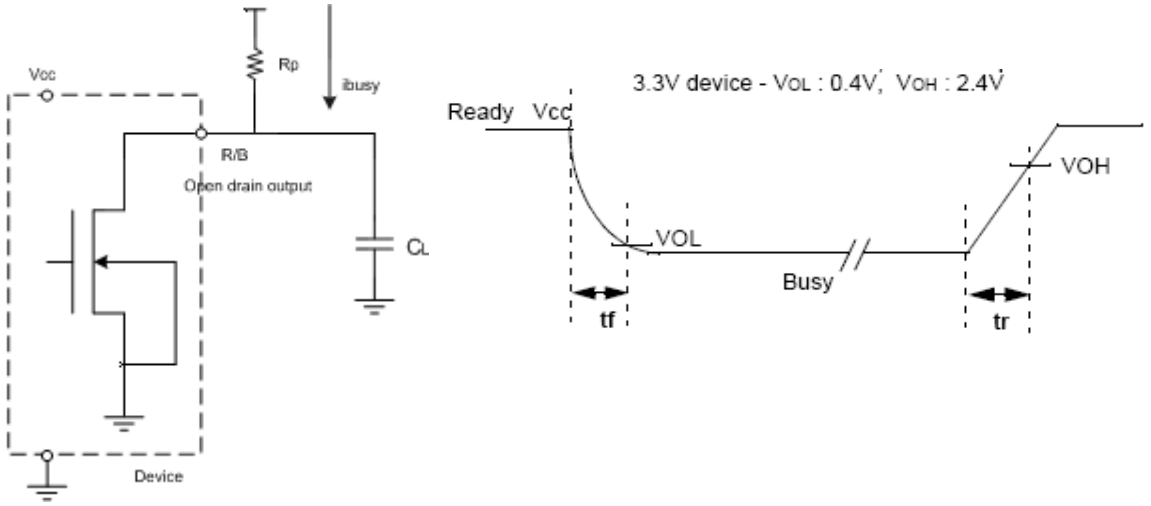
Table 4. Device Status

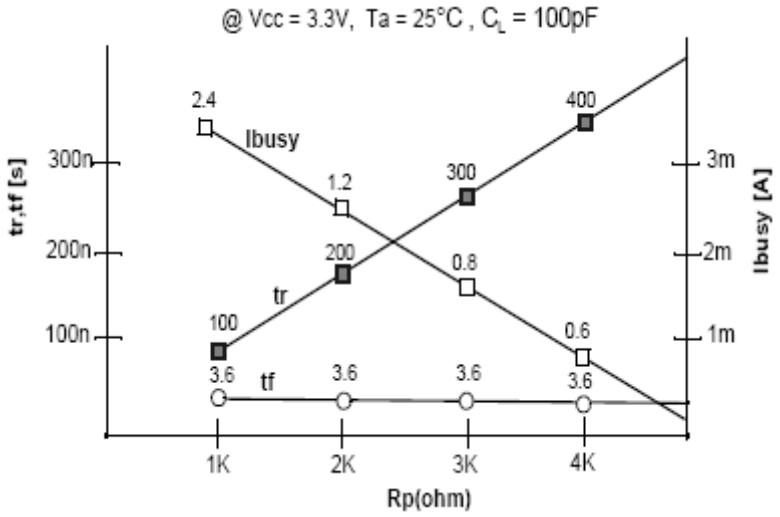
	After Power-up	After Reset
Operation mode	00h Command is latched	Waiting for next command

READY / BUSY

The device has a R/B output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B) and current drain during busy(ibusy), and appropriate value can be obtained with the following reference chart(Figure 15). Its value can be determined by the following guidance.

Figure 13. Rp vs tr , tf & Rp vs ibusy





Rp value guidance

$$Rp(min, 3.3V\ part) = \frac{Vcc(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

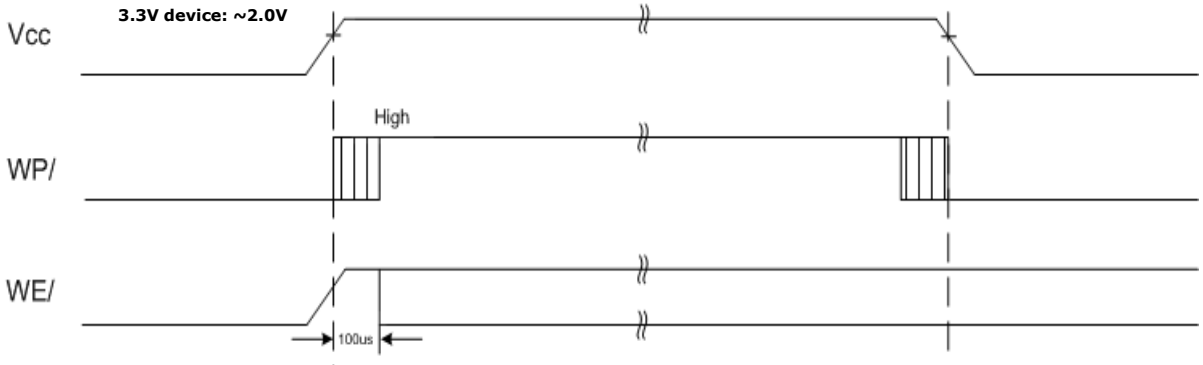
Data Protection & Power-up sequence

The device is designed to offer protection from any involuntary program / erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 2V.

/WP pin provides hardware protection and is recommended to be kept at VIL during power-down.

A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences as shown in Figure 16. The two command sequence for program / erase provides additional software protection.

Figure 14. AC Waveforms for Power Transition

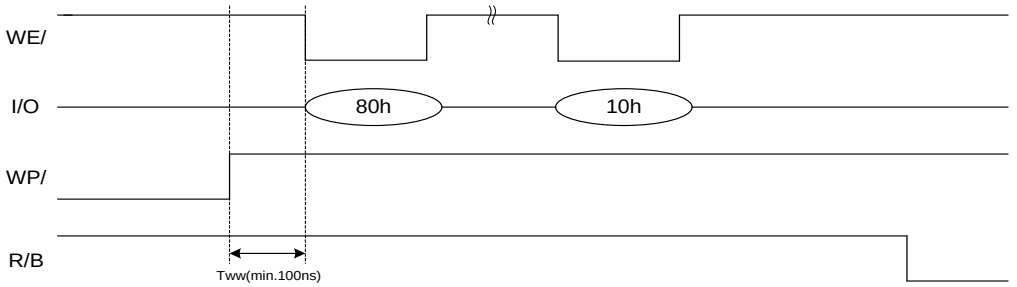


/WP AC Timing guide

Enabling /WP during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Figure A-1. Program Operation

1. Enable Mode



2. Disable Mode

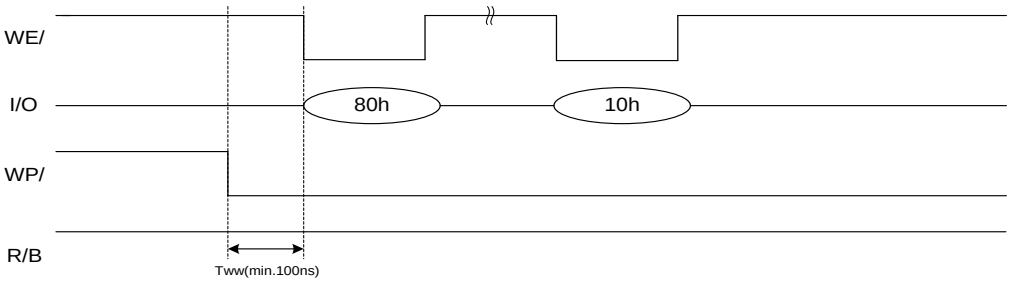
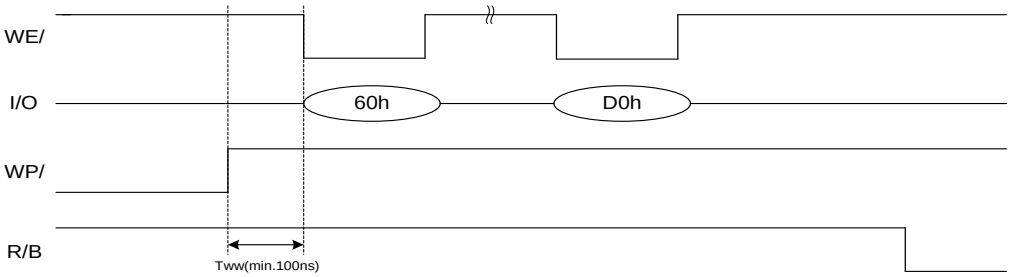


Figure A-2. Erase Operation

1. Enable Mode



2. Disable Mode