FH3400A

N-Channel Enhancement Mode MOSFET

Description

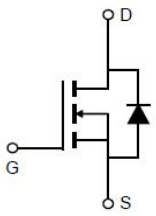
The FH3400A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and high density cell Design for ultra low on resistance. This device is suitable for use as a load switch or in PWM applications.

Application

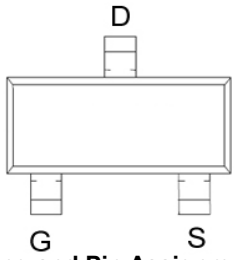
- PWM applications
- Load switch

General Features

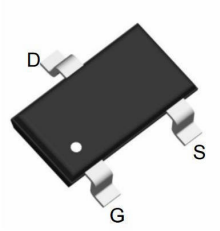
- V_{DS} =30V， I_D =6.5A
  $R_{DS(ON)}$ (Typ.)=17mΩ @V_{GS} = 10V
  $R_{DS(ON)}$ (Typ.)=18mΩ @V_{GS} =4.5V
  $R_{DS(ON)}$ (Typ.)=24mΩ @V_{GS} =2.5V
- High power and current handing capability
- Lead free product is acquired
- Surface mount package
- Fast Switching



Schematic diagram



Marking and Pin Assignment



SOT-23 top view

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	6.5	A
Pulsed Drain Current (Note 3)	I_{DM}	26	A
Drain-source Diode forward current (Note 1)	Is	2.5	A
Maximum power dissipation	P_D	1.25	W
Operating junction Temperature range	Tj	-55 – 150	℃

Thermal Characteristics

Thermal Resistance junction-to ambient (Note 3)	Rth JA	100	℃/W

■ Electrical Characteristics (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	30	35		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.65		1.2	V
Gate-Body Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	μA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 6.0A		17	21	mΩ
		V_{GS} = 4.5V, I_D = 5.0A		18	22	
		V_{GS} = 2.5V, I_D = 4.0A		24	29	
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D = 5.0A		11		S
Diode Forward Voltage **(Note 2)**	V_{SD}	V_{GS} = 0V, I_S = 2.5A			1.2	V
Diode Forward Current **(Note 1)**	I_S				2.5	A
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 15V, V_{GS} = 10V, I_D = 3A		7.0		nC
Gate-Source Charge	Q_{gs}			1.3		
Gate-Drain Charge	Q_{gd}			18		
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		760		pF
Output Capacitance	C_{oss}			88		
Reverse Transfer Capacitance	C_{rss}			67		
Switching						
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = 15V, R_L = 15Ω, V_{GS} = 10V, R_{GEN} = 6Ω, I_D = 1A		9		nS
Rise Time	t_r			3.3		
Turn-Off Delay Time	$t_{d(off)}$			29.3		
Fall-Time	t_f			3.4		

Note: 1. Mounted on FR4 board, t ≤ 10sec.

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

3. Repetitive Rating: Pulse width limited by maximum junction temperature.

Typical Performance Characteristics

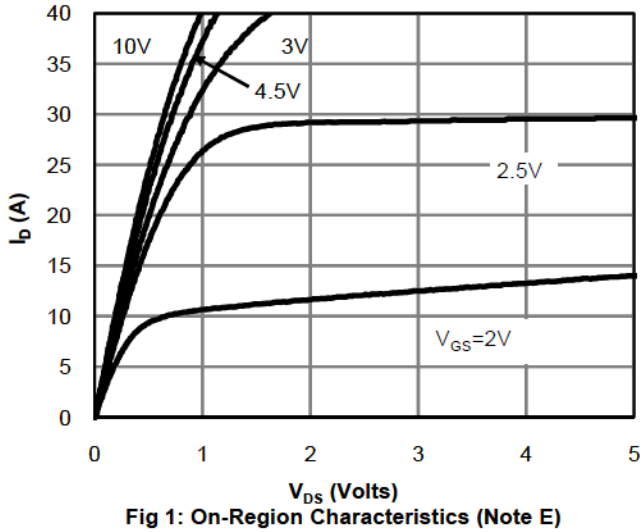


Fig 1: On-Region Characteristics (Note E)

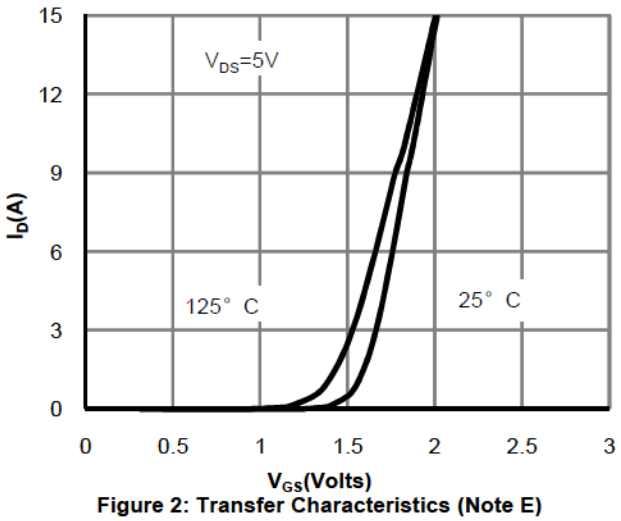


Figure 2: Transfer Characteristics (Note E)

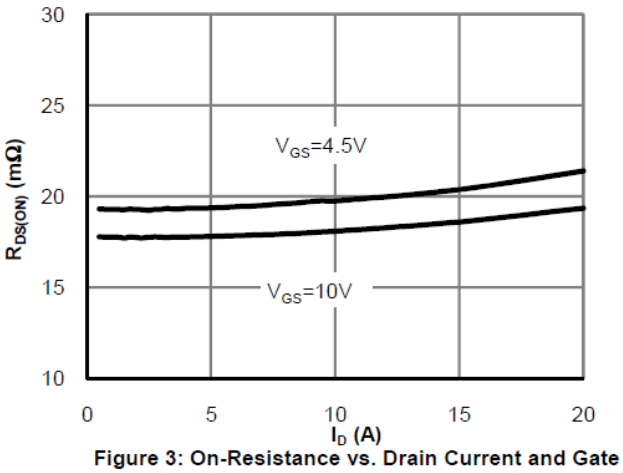


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

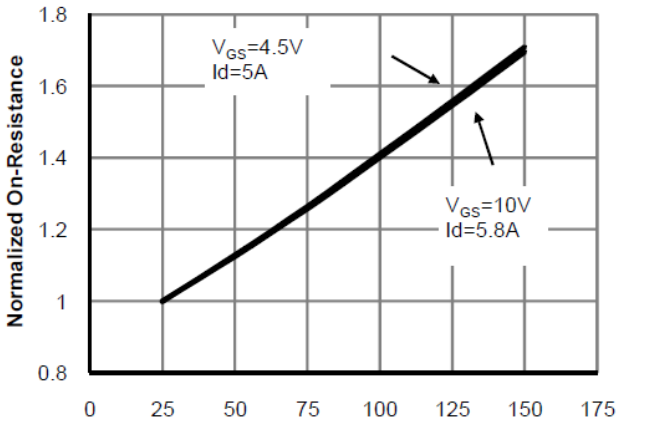


Figure 4: On-Resistance vs. Junction Temperature (Note E)

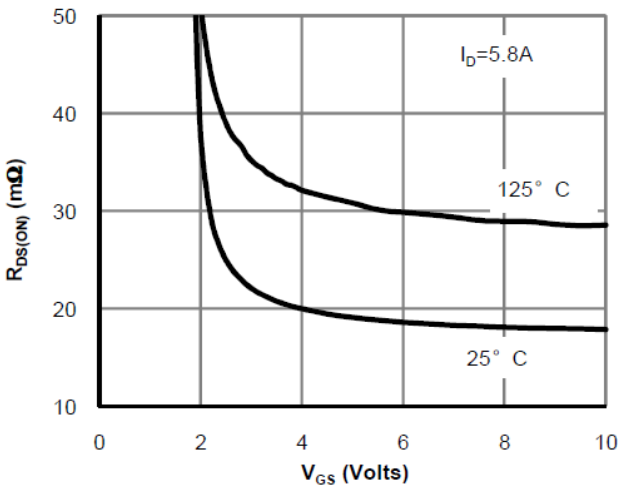


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

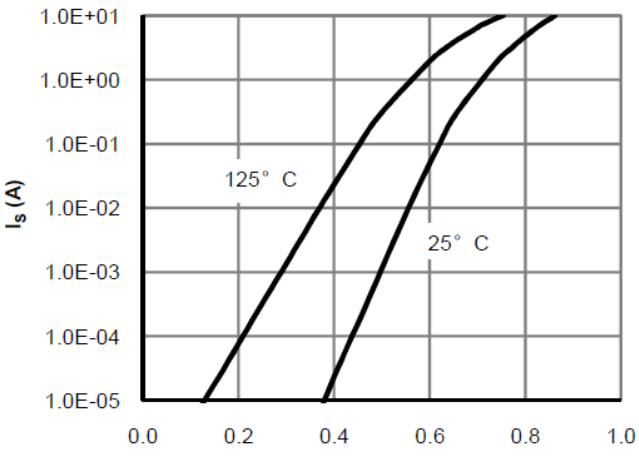


Figure 6: Body-Diode Characteristics (Note E)

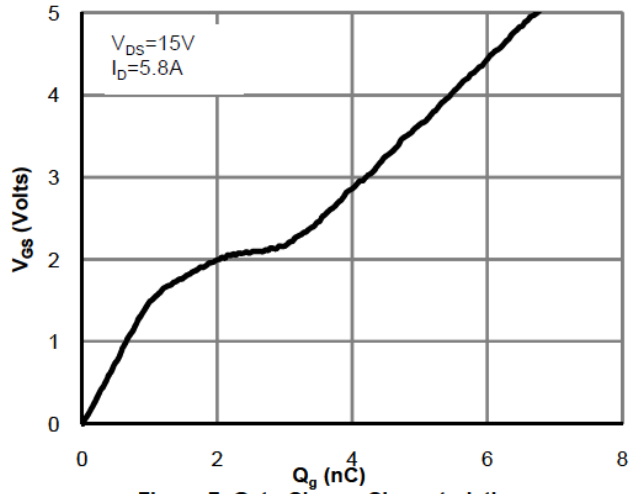


Figure 7: Gate-Charge Characteristics

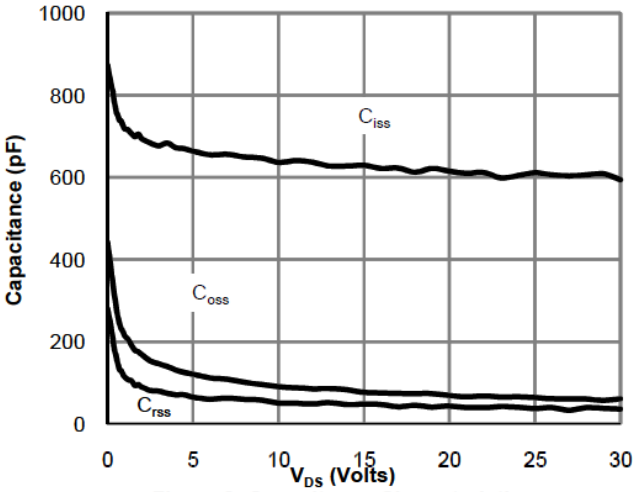


Figure 8: Capacitance Characteristics

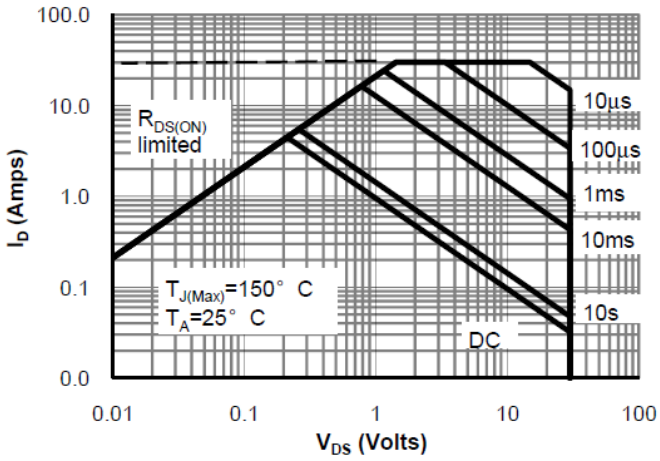


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

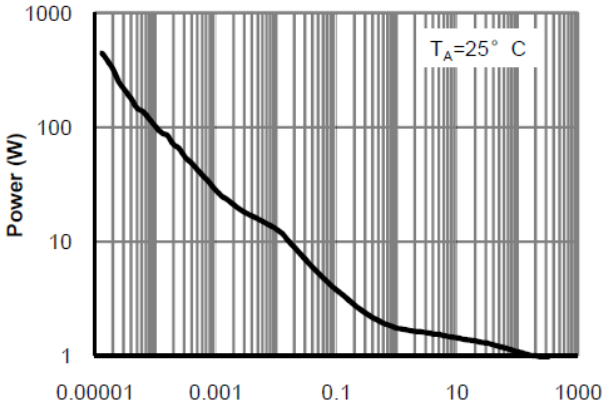


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

■ Typical Electrical and Thermal Characteristics

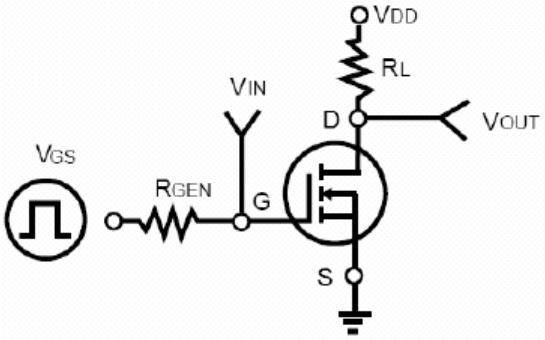


Figure 1: Switching Test Circuit

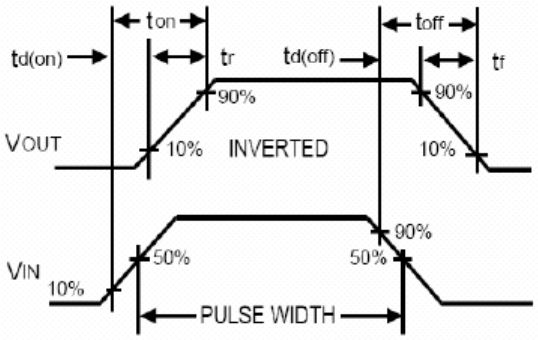


Figure 2: Switching Waveforms

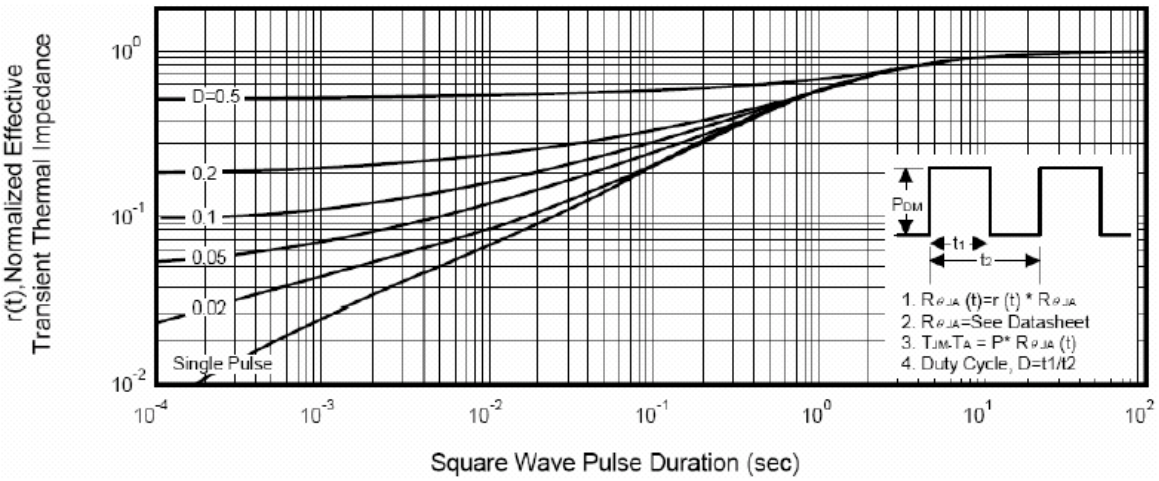
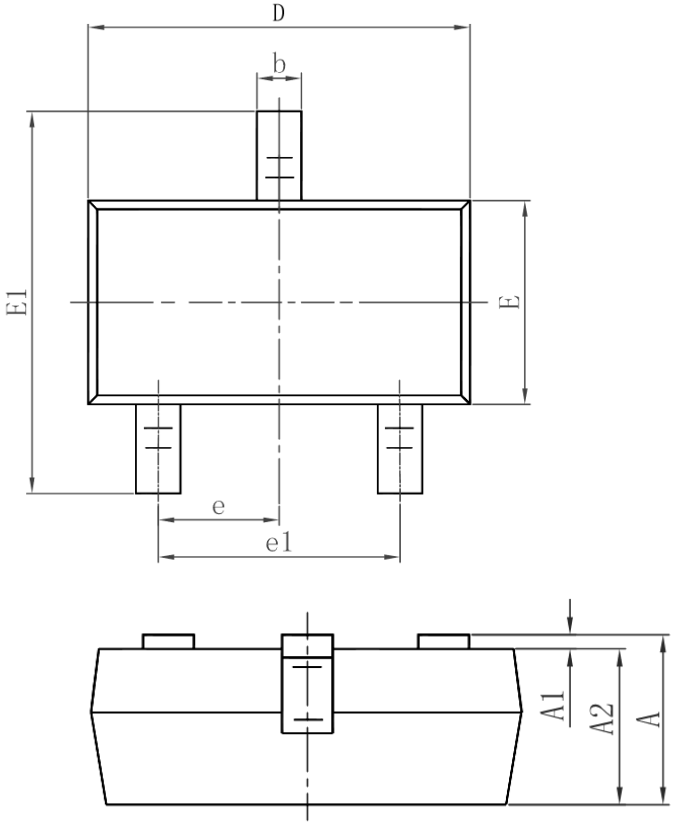


Figure 3: Normalized Maximum Transient Thermal Impedance

Package Information : SOT-23



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°