*适用于成本敏感型系统的*HT900x *低功耗*、RRIO、1MHz *运算放大器*

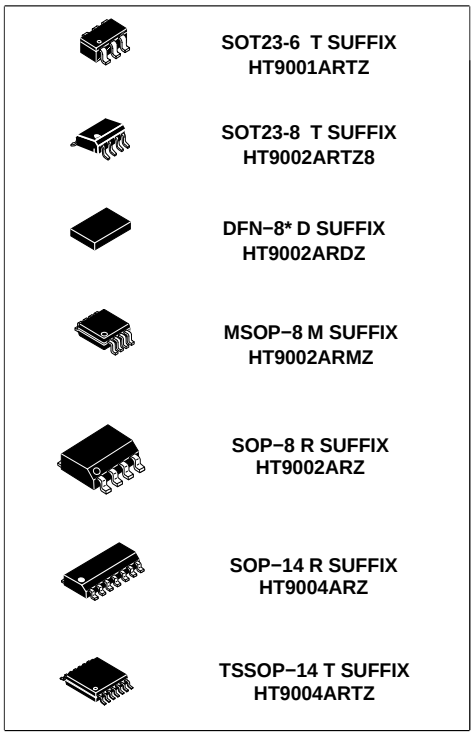
HT900x 系列包括单通道 (HT9001)、 双通道 (HT9002)、 和四通道 (HT9004) 低电压（1.8V 至 5.5V）运算放大器，具有轨至轨输入和输出摆幅能 力。这些运算放大器为空间受限、需要低压运行和高容性负载驱动的应用（例如烟雾探测器、可穿戴电子产品 和小型电器）提供了具有成本效益的解决方案。HT900x 系列的电容负载驱动器具有 500pF 的电容， 而电阻式开环输出阻抗使其能够在更高的电容负载下更 轻松地实现稳定。这些运算放大器专为低工作电压 (1.8V 至 5.5V)而设计，性能规格类似于 HT600x 器 件。

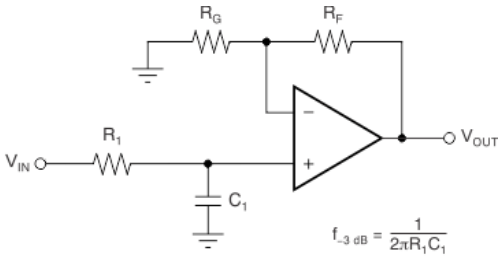
特性

- 可扩展 CMOS 放大器，适用于低成本应用
- 轨至轨输入和输出
- 低输入失调电压：±0.4mV
- 单位带宽增益积：1MHz
- 低宽带噪声：27nV/√Hz
- 低输入偏置电流：5pA
- 低静态电流：60μA/通道
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 可在电源电压低至 1.8V 的情况下运行
- 由于具有电阻式开环输出阻抗，因此可在更高的容性负载下更轻松地实现稳定
- 工作温度范围：－40°C 至 125°C

应用

- 传感器信号调节
- 电源模块
- 有源滤波器
- 低侧电流检测
- 烟雾探测器
- 运动检测器
- 可穿戴设备
- 大型和小型家用电器
- EPOS
- 条形码扫描仪
- 个人电子产品
- HVAC：暖通空调
- 电机控制：交流感应

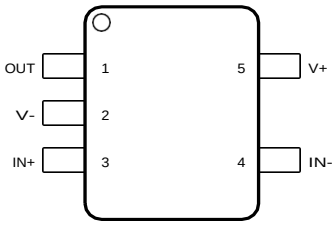




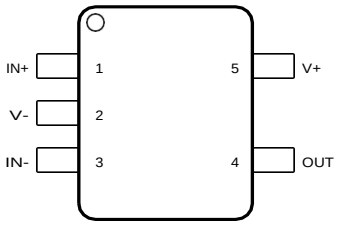
$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

单极低通滤波器

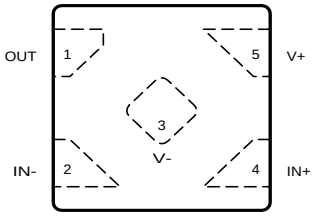
Pin Configuration and Functions



HT9001A



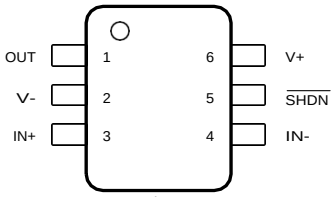
HT9001B



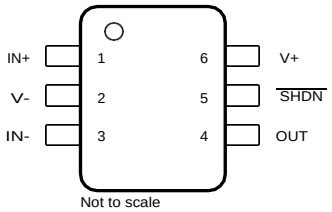
HT9001Q

表 6-1. Pin Functions: HT9001

PIN				I/O	DESCRIPTION
NAME	SOT-23,	SOT23	QFN		
IN −	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V −	2	2	3	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	I	Positive (high) supply



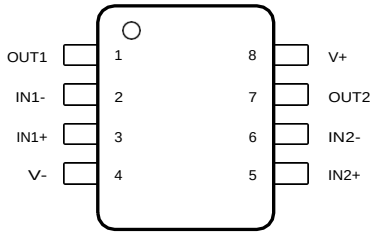
HT9001SA



HT9001SB

表 6-2. Pin Functions: HT9001S

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOT-23		
IN −	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
$\overline{SHDN}$	5	5	I	Shutdown: low = amp disabled, high = amp enabled. See 节 8.5 for more information.
V −	2	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply



HT9002R,HT9002M,HT9002S,HT9002T

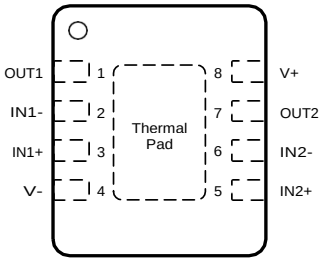


图 6-7. HT9002D

表 6-3. Pin Functions: HT9002

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 −	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 −	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V −	4	I or —	Negative (low) supply or ground (for single-supply operation)

Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage (V+) – (V–)				7	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		
Operating, T_A			–55	150	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

HT9002S PACKAGE			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
ALL OTHER PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

7.10 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.4	±1.6	mV
		V_S = 5 V, T_A = –40°C to 125°C			±2	
dV_{OS}/dT	V_{OS} vs temperature	T_A = –40°C to 125°C		±0.6		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 to 5.5 V, V_{CM} = (V–)	80	105		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		86		dB
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		95		
		V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to 125°C	63	77		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to 125°C		68		
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 5 V		±5		pA
I_{OS}	Input offset current			±2		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, V_S = 5 V		4.7		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, V_S = 5 V		30		nV/√Hz
		f = 10 kHz, V_S = 5 V		27		
i_n	Input current noise density	f = 1 kHz, V_S = 5 V		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	117		dB
		V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		100		
		V_S = 1.8 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 2 kΩ		115		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 5 V		1		MHz
Φ_m	Phase margin	V_S = 5.5 V, G = 1		78		°
SR	Slew rate	V_S = 5 V		2		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF		2.5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF		3		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.85		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, 80-kHz measurement BW		0.004%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ		10	20	mV
		V_S = 5.5 V, R_L = 2 kΩ		35	55	
I_{SC}	Short-circuit current	V_S = 5.5 V		±40		mA

7.10 Electrical Characteristics (continued)

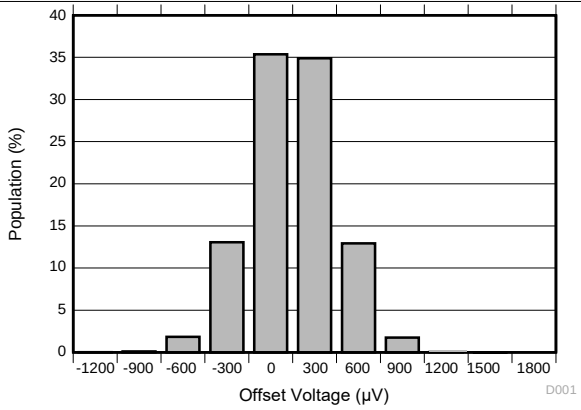
For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Specified voltage range			1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	HT9002, HT9002S HT9004, HT9004S	I_O = 0 mA, V_S = 5.5 V		60	75	µA
		HT9001, HT9001S	I_O = 0 mA, V_S = 5.5 V		60	77	
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to 125°C				85	
SHUTDOWN(1)							
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 V to 5.5 V, all amplifiers disabled, SHDN = V_S –			0.5	1.5	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 1.8 V to 5.5 V, amplifier disabled			10 || 2		GΩ || pF
	High level voltage shutdown threshold (amplifier enabled)	V_S = 1.8 V to 5.5 V			(V–) + 0.9	(V–) + 1.1	V
	Low level voltage shutdown threshold (amplifier disabled)	V_S = 1.8 V to 5.5 V		(V–) + 0.2 V	(V–) + 0.7 V		V
t_{ON}	Amplifier enable time (full shutdown)	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–			70		µs
	Amplifier enable time (partial shutdown)	V_S = 1.8 V to 5.5 V, partial shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–			50		
t_{OFF}	Amplifier disable time	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S / 2, R_L connected to V–			4		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ SHDN ≥ (V+) – 0.8 V			40		nA
		V_S = 1.8 V to 5.5 V, V– ≤ SHDN ≤ V– + 0.8 V			150		

(1) Specified by design and characterization; not production tested.

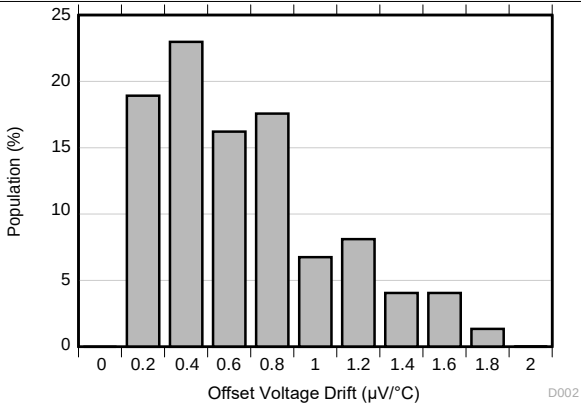
7.11 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V－ = －2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5 V

图 7-1. Offset Voltage Distribution Histogram



V_S = 5 V, T_A = －40°C to 125°C

图 7-2. Offset Voltage Drift Distribution Histogram

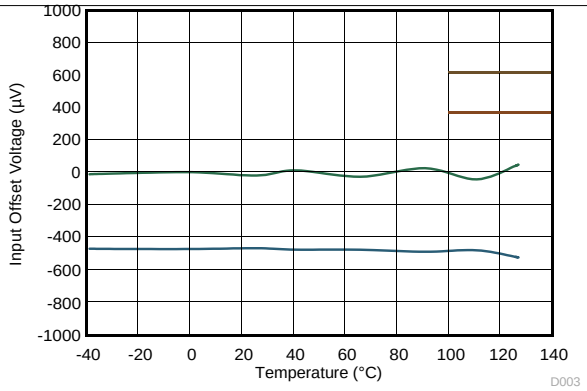


图 7-3. Input Offset Voltage vs Temperature

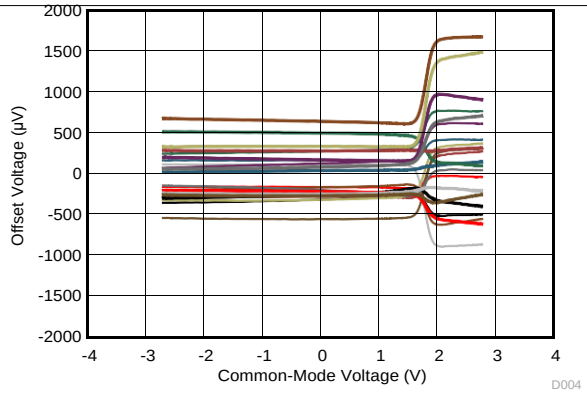


图 7-4. Offset Voltage vs Common-Mode

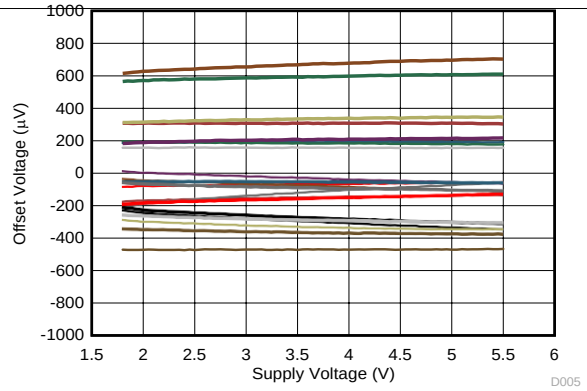


图 7-5. Offset Voltage vs Supply Voltage

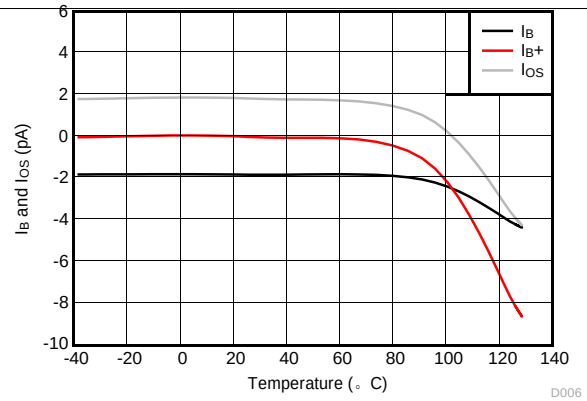


图 7-6. I_B and I_{OS} vs Temperature

7.11 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V – = – 2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

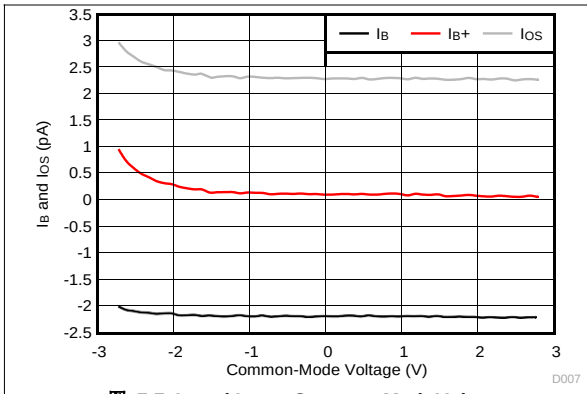


图 7-7. I_B and I_{OS} vs Common-Mode Voltage

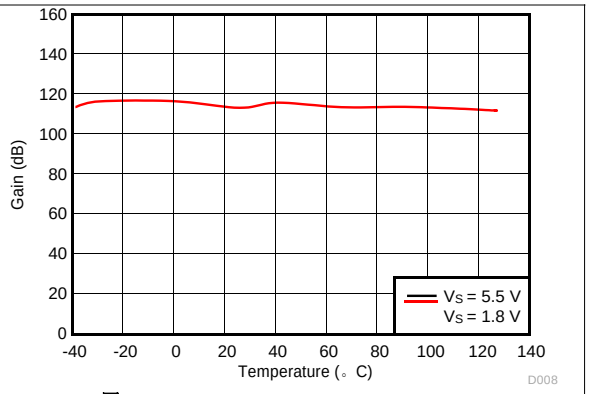
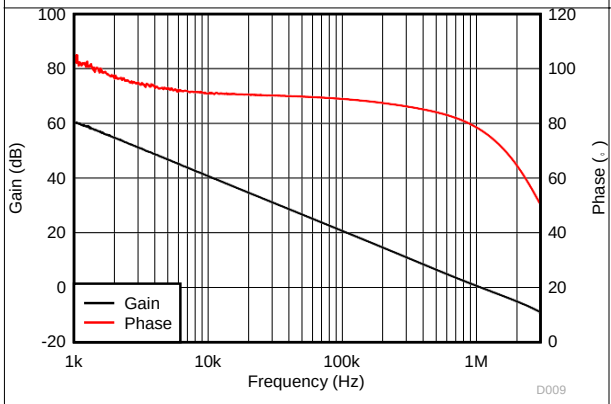


图 7-8. Open-Loop Gain vs Temperature



C_L = 10 pF

图 7-9. Open-Loop Gain and Phase vs Frequency

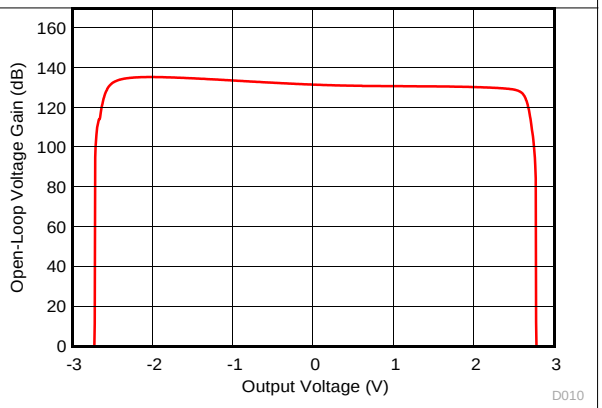
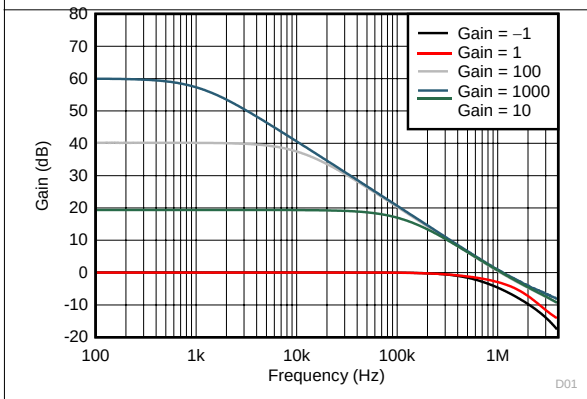


图 7-10. Open-Loop Gain vs Output Voltage



C_L = 10 pF

图 7-11. Closed-Loop Gain vs Frequency

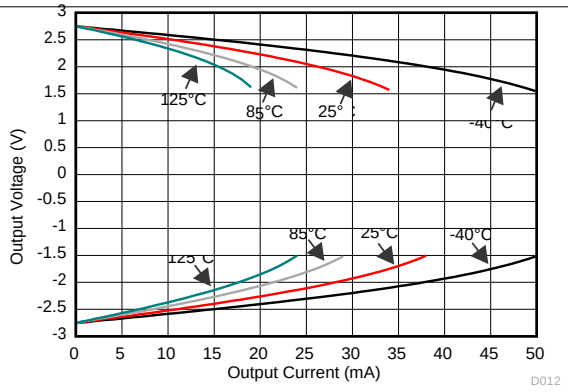


图 7-12. Output Voltage vs Output Current (Claw)

7.11 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V－ = －2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

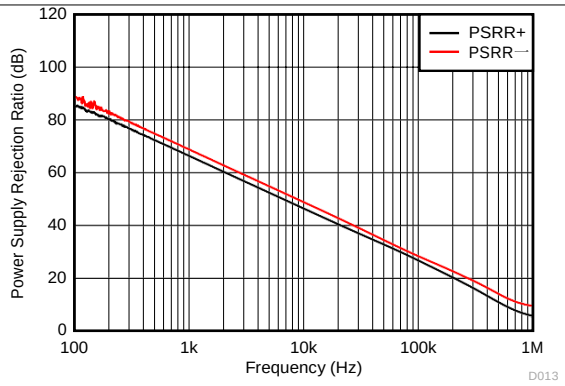
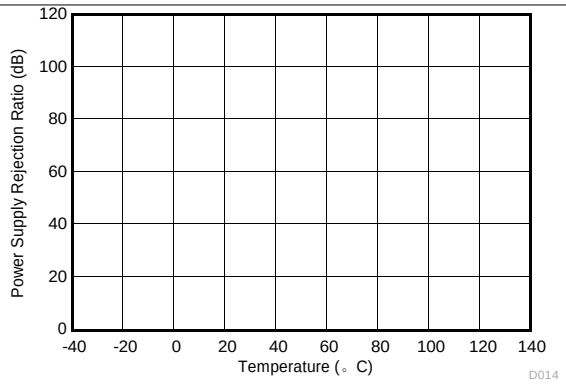


图 7-13. PSRR vs Frequency



V_S = 1.8 V to 5.5 V

图 7-14. DC PSRR vs Temperature

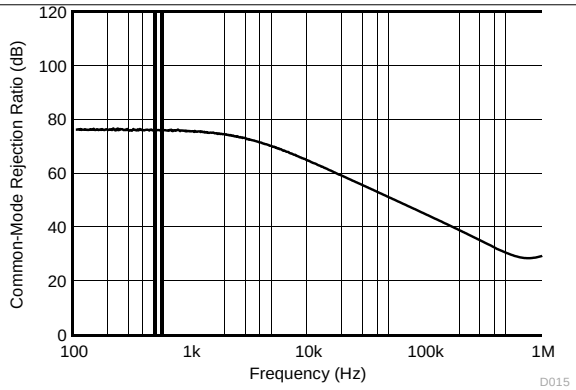
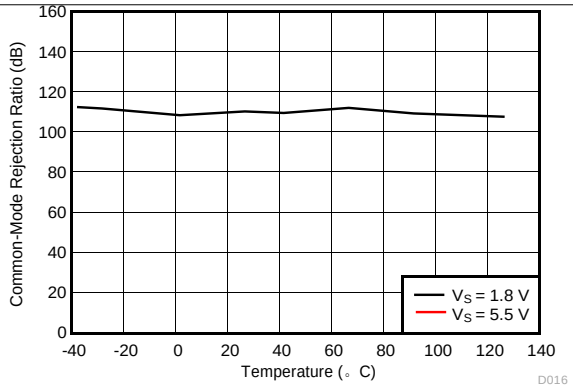


图 7-15. CMRR vs Frequency



V_{CM} = (V－) － 0.1 V to (V+) － 1.4 V

图 7-16. DC CMRR vs Temperature

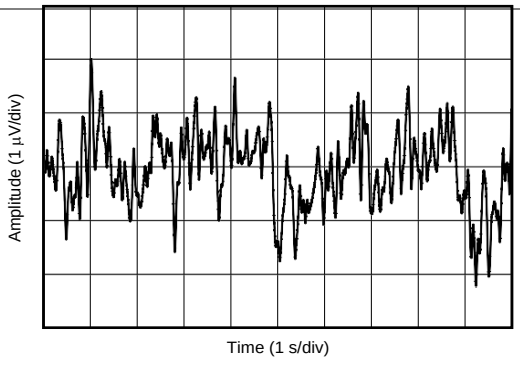


图 7-17. 0.1-Hz to 10-Hz Integrated Voltage Noise

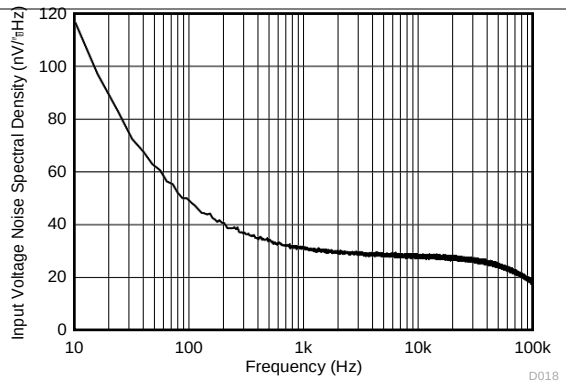
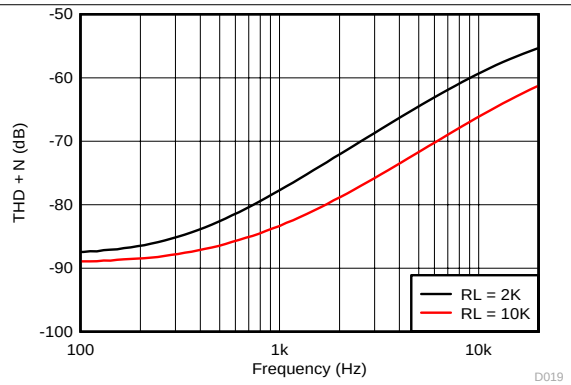


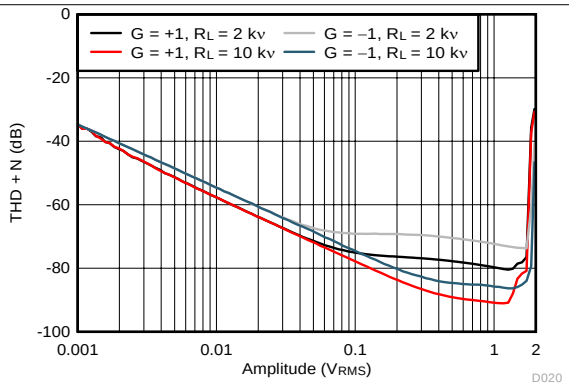
图 7-18. Input Voltage Noise Spectral Density

at T_A = 25°C, V+ = 2.75 V, V – = – 2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V V_{CM} = 2.5 V G = 1
BW = 80 kHz V_{OUT} = 0.5 V_{RMS}

图 7-19. THD + N vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V f = 1 kHz
G = 1 BW = 80 kHz

图 7-20. THD + N vs Amplitude

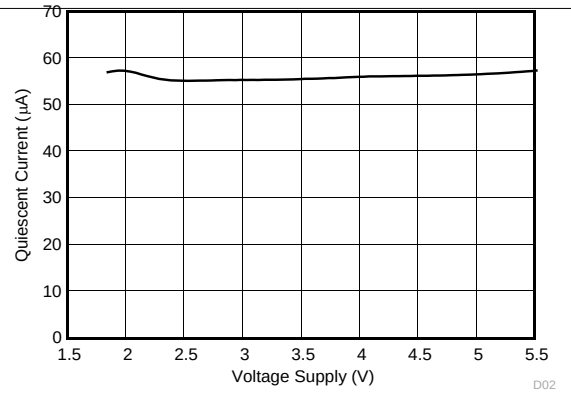


图 7-21. Quiescent Current vs Supply Voltage

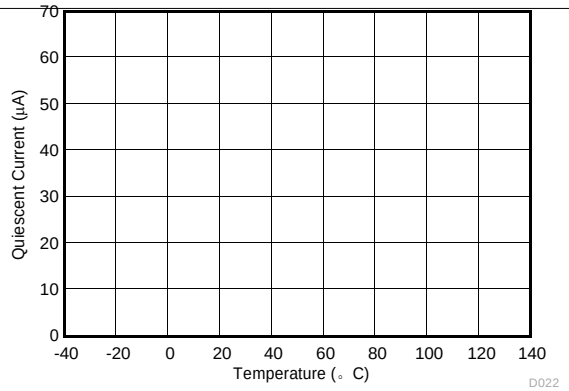


图 7-22. Quiescent Current vs Temperature

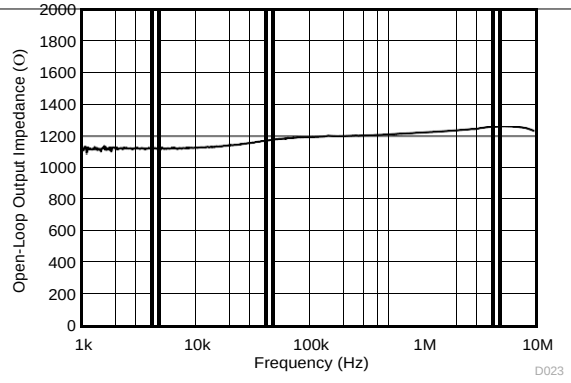
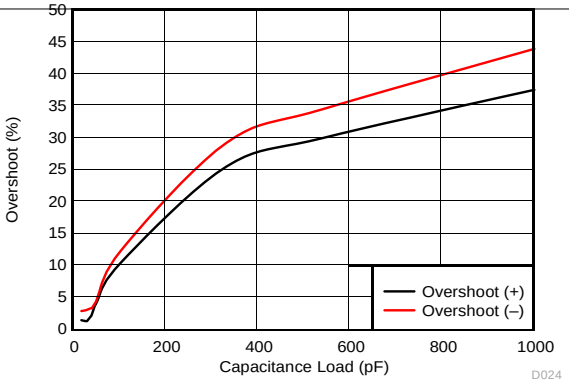


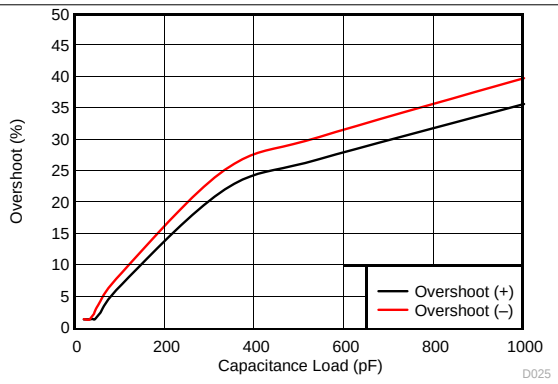
图 7-23. Open-Loop Output Impedance vs Frequency



G = 1 V_{IN} = 100 mVpp

图 7-24. Small Signal Overshoot vs Capacitive Load

at T_A = 25°C, V+ = 2.75 V, V – = – 2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = – 1 V_{IN} = 100 mVpp

图 7-25. Small Signal Overshoot vs Capacitive Load

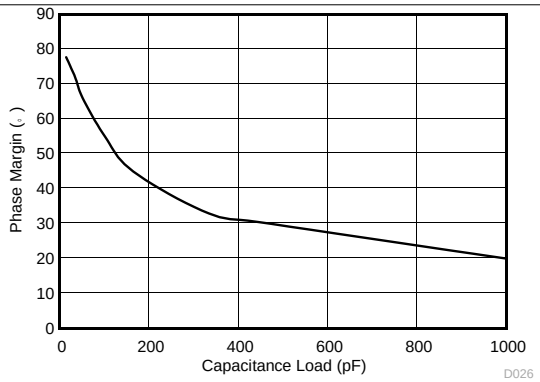
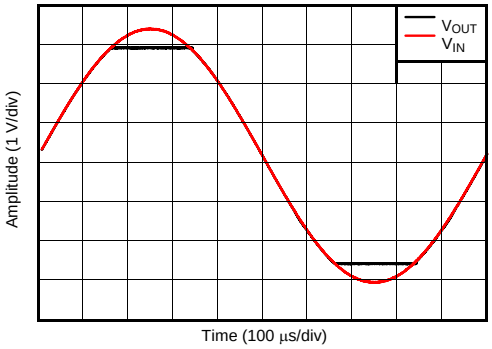
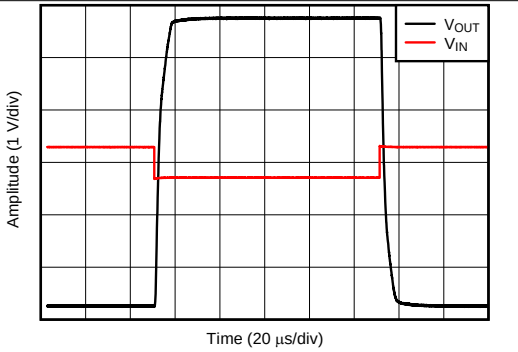


图 7-26. Phase Margin vs Capacitive Load



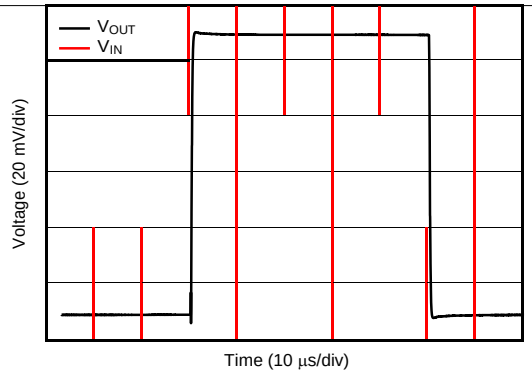
G = 1 V_{IN} = 6.5 V_{PP}

图 7-27. No Phase Reversal



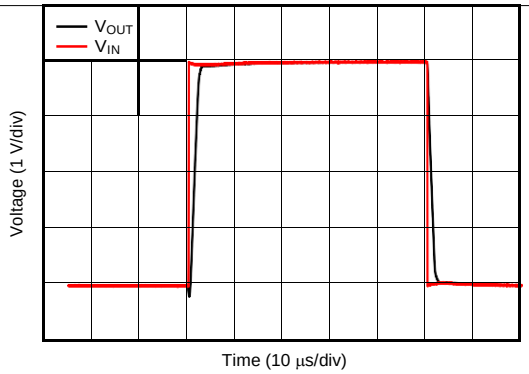
G = – 10 V_{IN} = 600 mV_{PP}

图 7-28. Overload Recovery



G = 1 V_{IN} = 100 mV_{PP} C_L = 10 pF

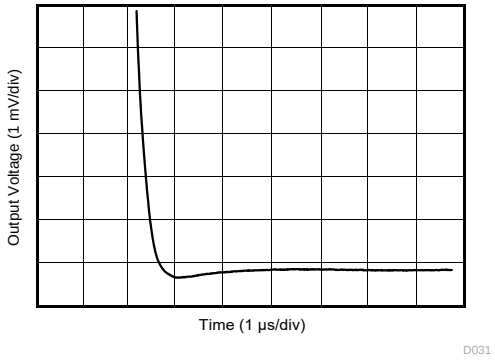
图 7-29. Small-Signal Step Response



G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

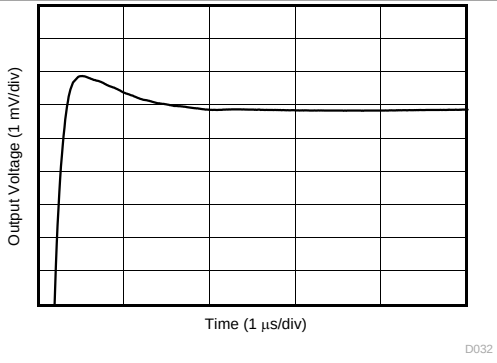
图 7-30. Large-Signal Step Response

at T_A = 25°C, V+ = 2.75 V, V－ = －2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 1　　C_L = 100 pF　　2-V step

图 7-31. Large-Signal Settling Time (Negative)



G = 1　　C_L = 100 pF　　2-V step

图 7-32. Large-Signal Settling Time (Positive)

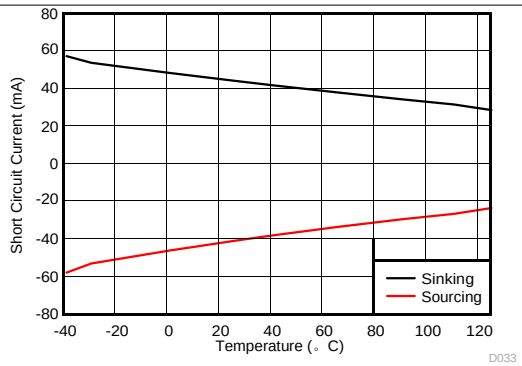


图 7-33. Short-Circuit Current vs Temperature

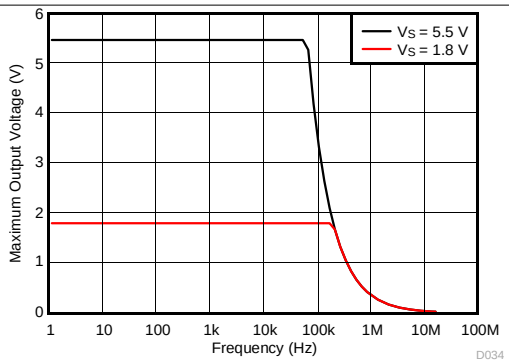


图 7-34. Maximum Output Voltage vs Frequency

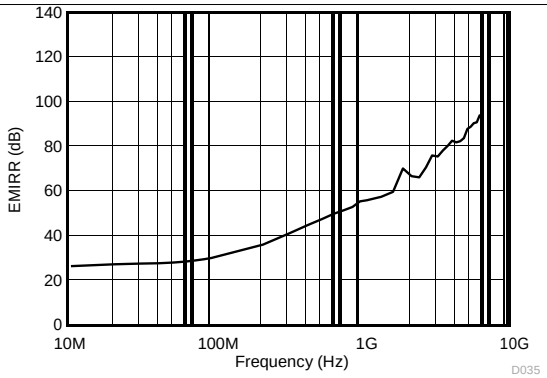


图 7-35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

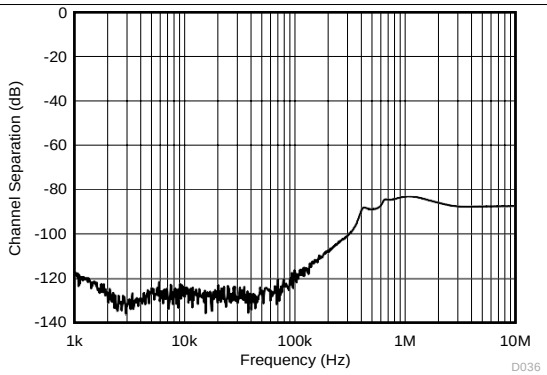


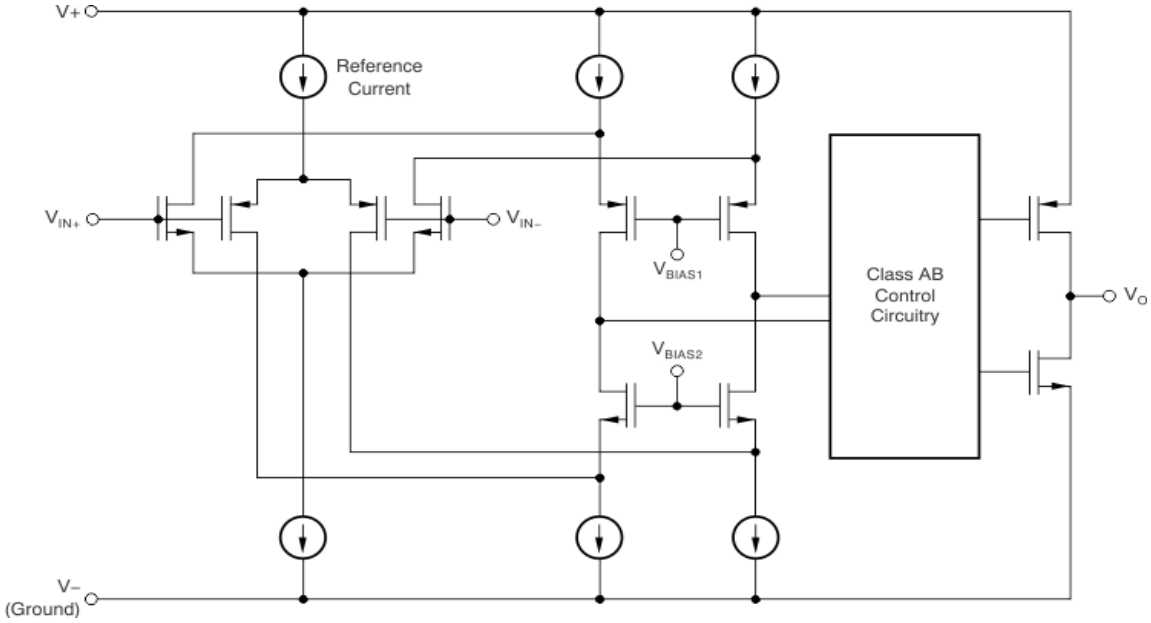
图 7-36. Channel Separation

8 Detailed Description

8.1 Overview

The HT900x is a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the HT900x family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The HT900x family of op amps are for operation from 1.8 V to 5.5 V. In addition, many specifications such as input offset voltage, quiescent current, offset current, and short circuit current apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in 节 7.11.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the HT900x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in 节 8.2. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 100-mV transition region can vary up to 100 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the HT900x family delivers a robust output drive capability. A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 20 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 EMI Rejection

The HT900x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the HT900x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 8-1 shows the results of this testing on the HT900x.

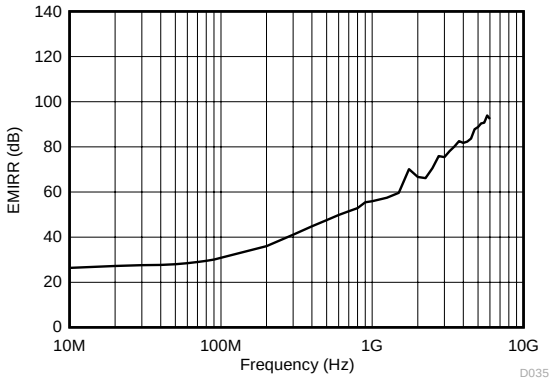


图 8-1. EMIRR Testing

表 8-1. HT900x EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB

8.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the HT900x family is approximately 850 ns.

8.5 Shutdown

The HT9001S, HT9002S, and HT9004S devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 µA. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 620 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V^- and V^- + 0.2 V. A valid logic high is defined as a voltage between V^- + 1.2 V and V+. The shutdown pin circuitry includes a pull-up resistor, which will inherently pull the voltage of the pin to the positive supply rail if not driven. Thus, to enable the amplifier, the $\overline{\text{SHDN}}$ pins should either be left floating or driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. While we highly recommend that the shutdown pin be connected to a valid high or a low voltage or driven, we have included a pull-up resistor connected to VCC. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5 V. Exceeding this voltage level will damage the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 70 µs for full shutdown of all channels; disable time is 4 µs. When disabled, the output assumes a high-impedance state. This architecture allows the HT9002S and HT9004S to operate as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the HT9001S, HT9002S, or HT9004S without a load, the resulting turnoff time significantly increases.

8.6 Device Functional Modes

The HT900x family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

9.1 Application Information

The HT900x family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable applications. The devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10- kΩ loads connected to any point between V+ and V－. The input common-mode voltage range includes both rails, and allows the HT900x devices to be used in any single-supply application.

9.2 Typical Application

9.2.1 HT900x Low-Side, Current Sensing Application

图 9-1 shows the HT900x configured in a low-side current sensing application.

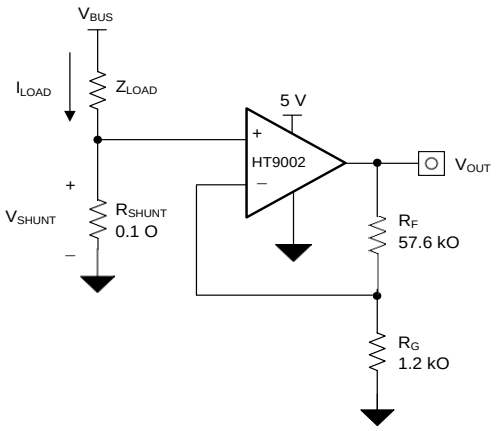


图 9-1. HT900x in a Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 9-1 is given in 方程式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using 方程式 2.

$$R_{SHUNT} \quad \frac{V_{SHUNT\_MAX}}{I_{LOAD\ MAX}} \quad \frac{100mV}{1A} \quad 100m\Omega \tag{2}$$

Using 方程式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the HT900x to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the HT900x to produce the necessary output voltage is calculated using 方程式 3.

$$Gain = \frac{\left(V_{OUT\_MAX} \quad V_{OUT\_MIN}\right)}{\left(V_{IN\ MAX} \quad V_{IN\ MIN}\right)} \tag{3}$$

Using 方程式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 方程式 4 sizes the resistors R_F and R_G, to set the gain of the HT900x to 49 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. 图 9-2 shows the measured transfer function of the circuit shown in 图 9-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

9.2.1.3 Application Curve

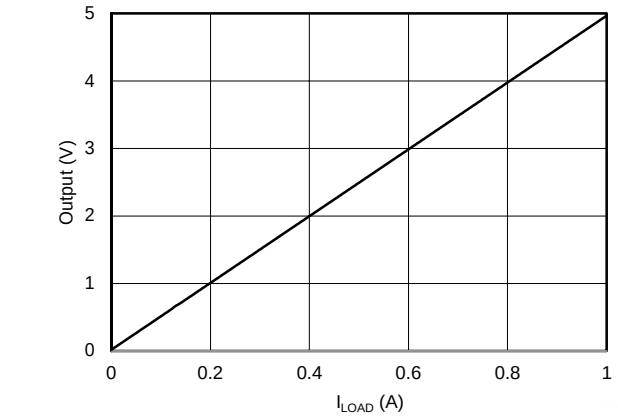


图 9-2. Low-Side, Current-Sense Transfer Function

9.2.2 Single-Supply Photodiode Amplifier

Photodiodes are used in many applications to convert light signals to electrical signals. The current through the photodiode is proportional to the photon energy absorbed, and is commonly in the range of a few hundred picoamps to a few tens of microamps. An amplifier in a transimpedance configuration is typically used to convert the low-level photodiode current to a voltage signal for processing in an MCU. The circuit shown in 图 9-3 is an example of a single-supply photodiode amplifier circuit using the HT9002.

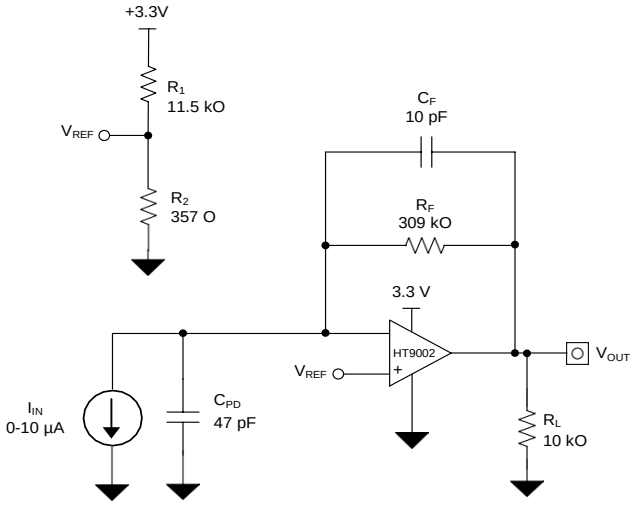


图 9-3. Single-Supply Photodiode Amplifier Circuit

9.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage: 3.3 V
- Input: 0 µA to 10 µA
- Output: 0.1 V to 3.2 V
- Bandwidth: 50 kHz

9.2.2.2 Detailed Design Procedure

The transfer function between the output voltage (V_{OUT}), the input current, (I_{IN}) and the reference voltage (V_{REF}) is defined in 方程式 5.

$$V_{OUT} = I_{IN} \times R_F + V_{REF} \tag{5}$$

Where:

$$V_{REF} = V_+ \times \frac{R_1 \times R_2)}{R + R_{\text{飞}\ 1\ \ 2)}} \tag{6}$$

Set V_{REF} to 100 mV to meet the minimum output voltage level by setting R1 and R2 to meet the required ratio calculated in 方程式 7.

$$\frac{V_{REF}}{V_+} = \frac{0.1\ V}{3.3\ V} = 0.0303 \tag{7}$$

The closest resistor ratio to meet this ratio sets R1 to 11.5 kΩ and R2 to 357 Ω.

The required feedback resistance can be calculated based on the input current and desired output voltage.

$$R_F = \frac{V_{OUT} \quad V_{REF}}{I_{IN}} = \frac{3.2\ V \quad 0.1\ V}{10\ \mu A} = 310 \frac{kV}{A} \text{ 但 } 309\ k\nu \tag{8}$$

Calculate the value for the feedback capacitor based on R_F and the desired –3-dB bandwidth, (f_{-3dB}) using 方程式 9.

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_{3dB}} = \frac{1}{2 \times \pi \times 309\ k\nu \times 50\ kHz} = 10.3\ pF \text{ 但 } 10\ pF \tag{9}$$

The minimum op amp bandwidth required for this application is based on the value of R_F, C_F, and the capacitance on the INx– pin of the HT9002 which is equal to the sum of the photodiode shunt capacitance, (CPD) the common-mode input capacitance, (CCM) and the differential input capacitance (CD) as 方 程 式 10 shows.

$$C_{IN} = C_{PD} + C_{CM} + C_D = 47\ pF + 5\ pF + 1\ pF = 53\ pF \tag{10}$$

The minimum op amp bandwidth is calculated in 方程式 11.

$$f_{=BGW} > \frac{C_{IN} + C_F}{2 \times \pi \times R_F \times C_F^{\ 2}} > 324\ kHz \tag{11}$$

The 1-MHz bandwidth of the HT900x meets the minimum bandwidth requirement and remains stable in this application configuration.

The measured current-to-voltage transfer function for the photodiode amplifier circuit is shown in 图 9-4. The measured performance of the photodiode amplifier circuit is shown in 图 9-5.

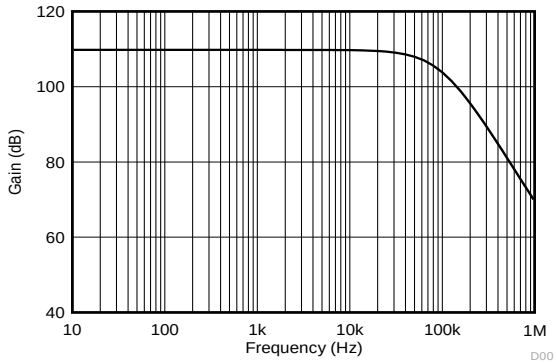


图 9-4. Photodiode Amplifier Circuit AC Gain Results

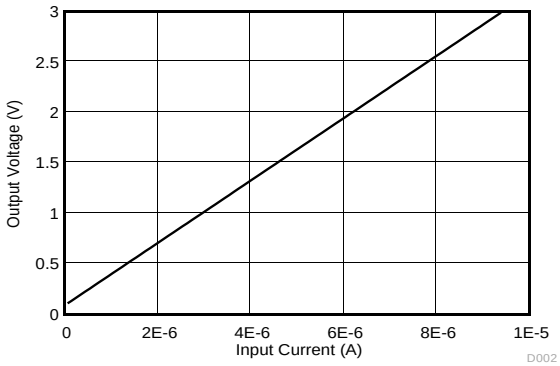


图 9-5. Photodiode Amplifier Circuit DC Results

10 Power Supply Recommendations

The HT900x family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. 节 7.11 presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see 节 7.1.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see 节 11.1.

10.1 Input and ESD Protection

The HT900x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA. 图 10-1 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

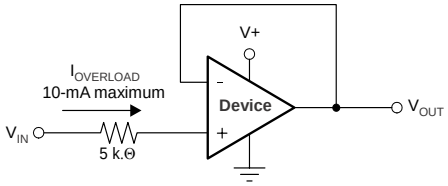


图 10-1. Input Current Protection

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in 图 11-2. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

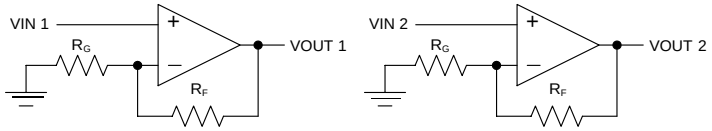


图 11-1. Schematic Representation

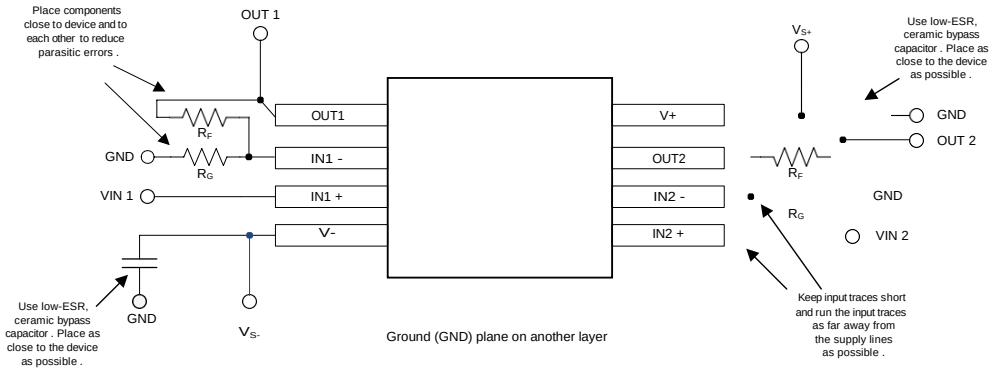
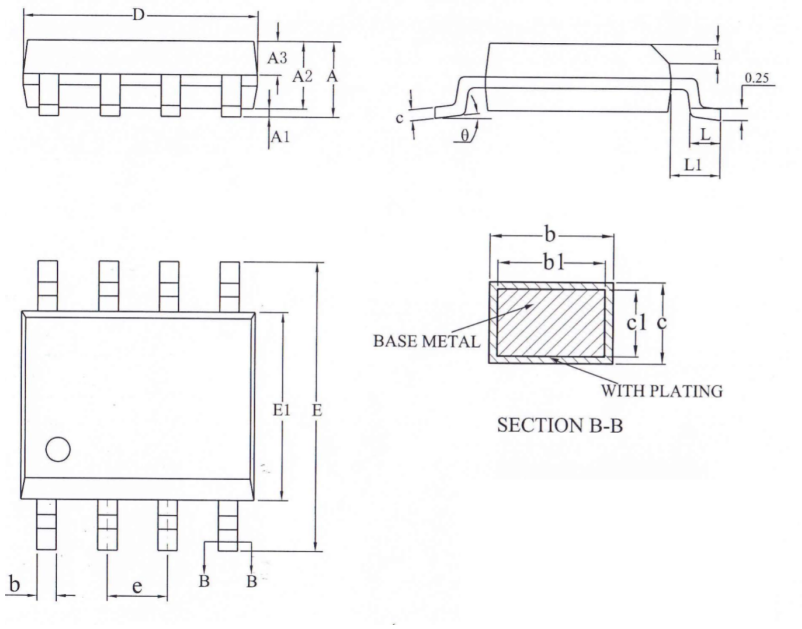


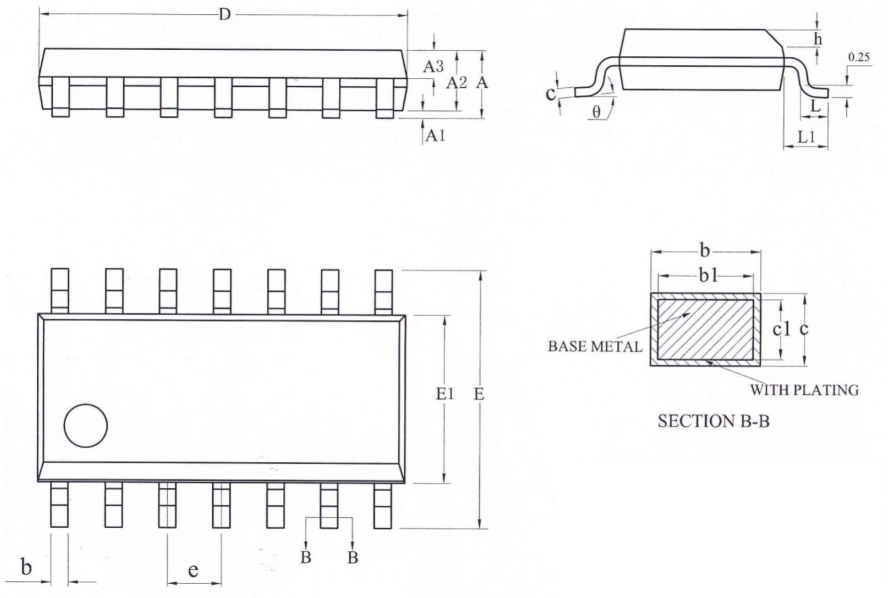
图 11-2. Layout Example

SOP8



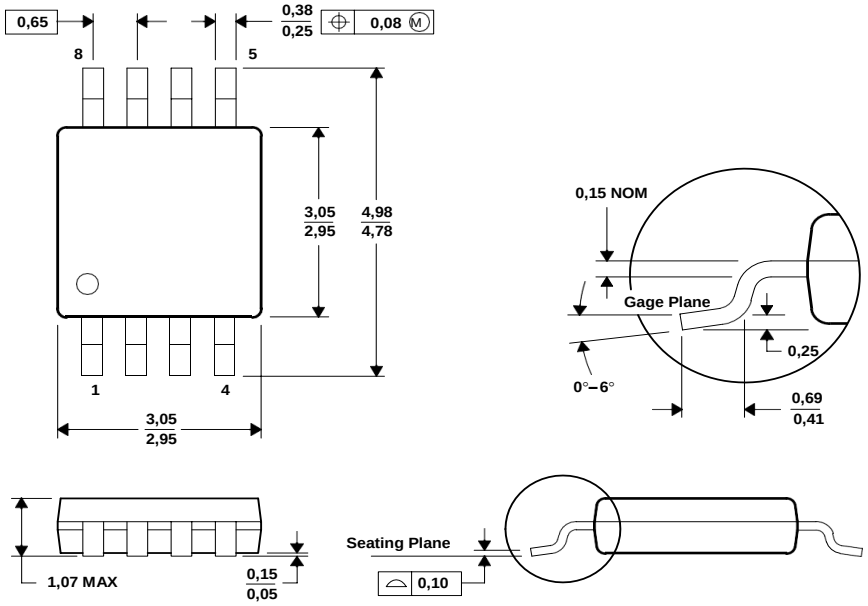
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
⚠ b	0.39	—	0.47
⚠ b1	0.38	0.41	0.44
⚠ c	0.20	—	0.24
c1	0.19	0.20	0.21
⚠ D	4.80	4.90	5.00
E	5.80	6.00	6.20
⚠ E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

SOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
⚠ b	0.39	—	0.47
⚠ b1	0.38	0.41	0.44
⚠ c	0.20	—	0.24
c1	0.19	0.20	0.21
⚠ D	8.55	8.65	8.75
E	5.80	6.00	6.20
⚠ E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

MSOP8



SOT23-8L