

SED3032G

**Dual N-Channel Enhancement-Mode MOSFET**

Revision: A

**General Description**

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

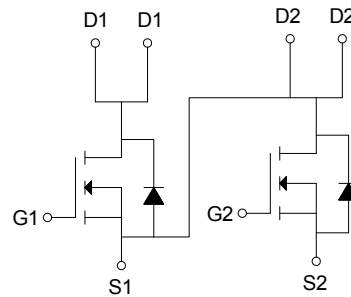
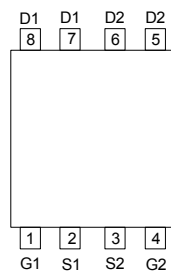
**Features**

For a single MOSFET

- $V_{DS} = 30V$
- $R_{DS(ON)} = 7.4m\Omega @ V_{GS}=10V$

**Pin configurations**

See Diagram below



**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current		Continuous	30
		Pulsed	170
Total Power Dissipation	@ $T_A=25^\circ C$	70	W
Operating Junction Temperature Range	$T_J$	-55 to 150	$^\circ C$

**Thermal Resistance**

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Junction to Ambient ( $t \leq 10s$ )	40	50	$^\circ C/W$

**SED3032G**

<b>Q1 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)</b>						
<b>Symbol</b>	<b>Parameter</b>	<b>Test Conditions</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Units</b>
<b>OFF CHARACTERISTICS (Note 2)</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0 V	30			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.6		2.7	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		7.4	8.5	mΩ
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		680		pF
C <sub>oss</sub>	Output Capacitance			102		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			71		pF
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		17.5		nC
Q <sub>gs</sub>	Gate Source Charge			43		nC
Q <sub>gd</sub>	Gate Drain Charge			4.1		nC
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>GEN</sub> =3Ω I <sub>D</sub> =20A		5		ns
t <sub>d(off)</sub>	Turn-Off Delay Time			19		ns
t <sub>d(r)</sub>	Turn-On Rise Time			12		ns
t <sub>d(f)</sub>	Turn-Off Fall Time			6		ns
<b>Source-Drain Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =24A			1.2	V
I <sub>S</sub>	Diode Forward Current				30	A
t <sub>rr</sub>	Reverse Recovery Time	T <sub>J</sub> =25°C, I <sub>F</sub> =20A		19		ns
Q <sub>rr</sub>	Reverse Recovery Charge	Di/dt=100A/μs		10		nC
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible(turn-on is dominated by LS)				

Typical Characteristics

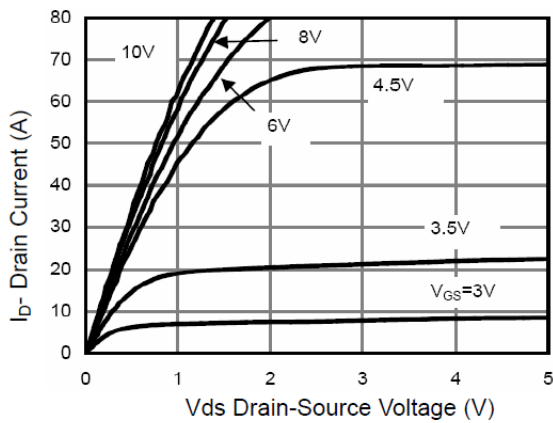


Figure 1 Output Characteristics

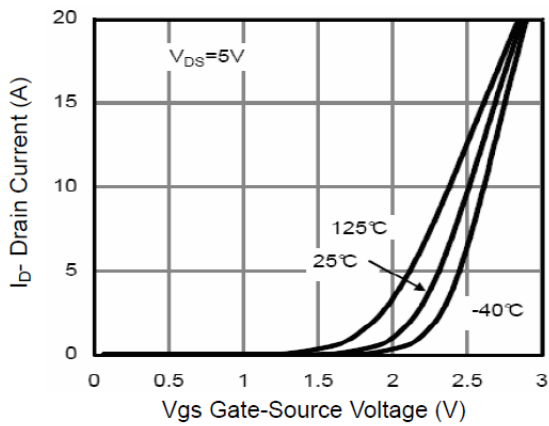


Figure 2 Transfer Characteristics

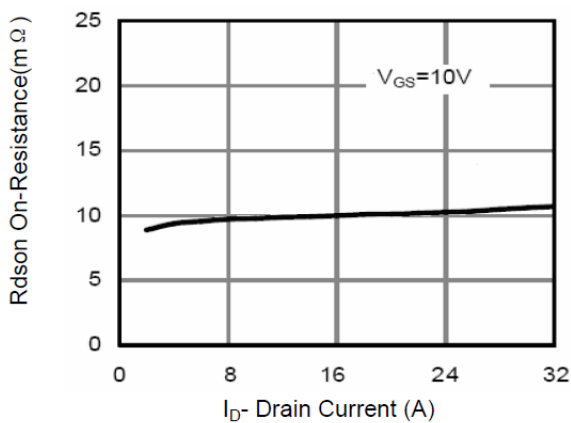


Figure 3  $R_{DS(on)}$ - Drain Current

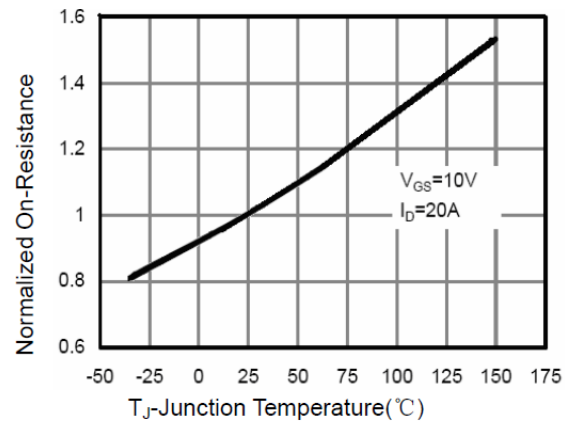


Figure 4  $R_{DS(on)}$ -Junction Temperature

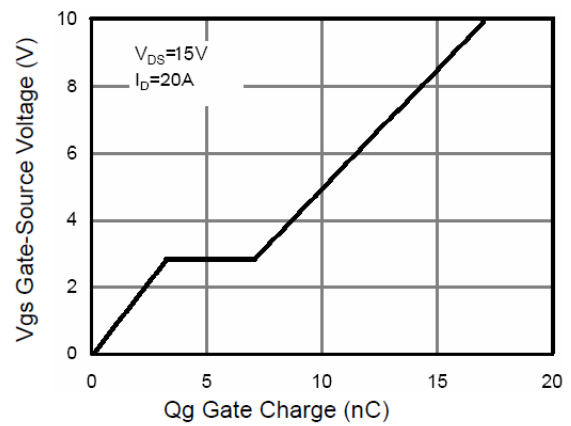


Figure 5 Gate Charge

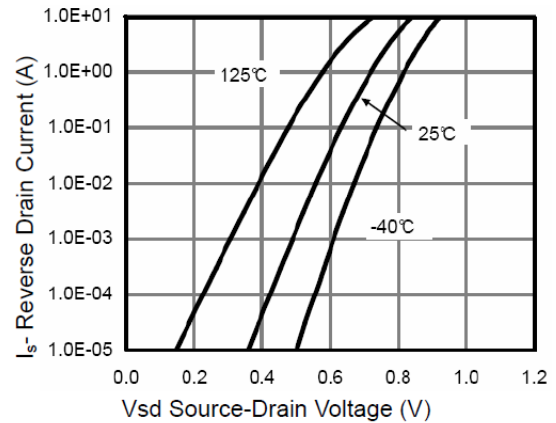


Figure 6 Source- Drain Diode Forward

Typical Characteristics

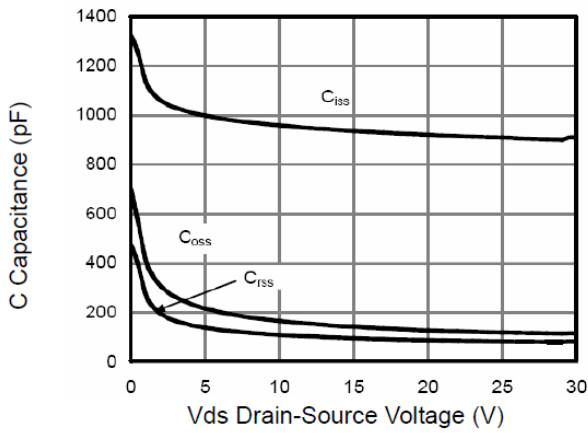


Figure 7 Capacitance vs Vds

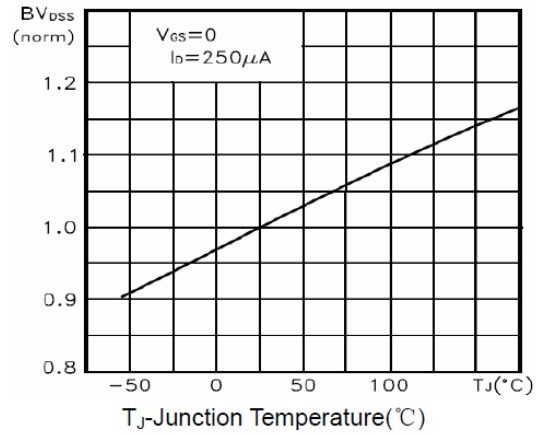


Figure 9  $BV_{DSS}$  vs Junction Temperature

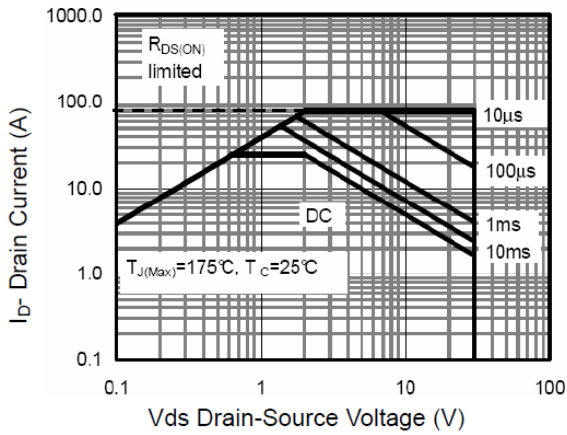


Figure 8 Safe Operation Area

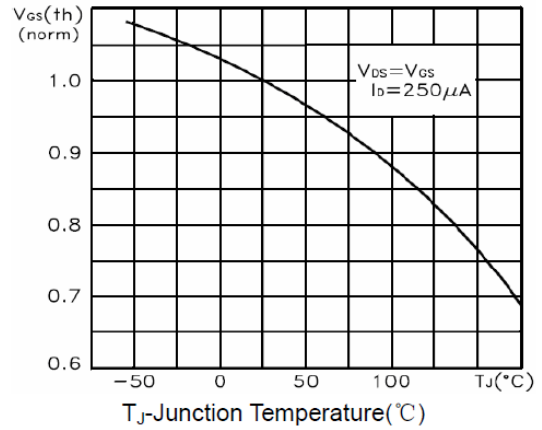


Figure 10  $V_{GS(th)}$  vs Junction Temperature

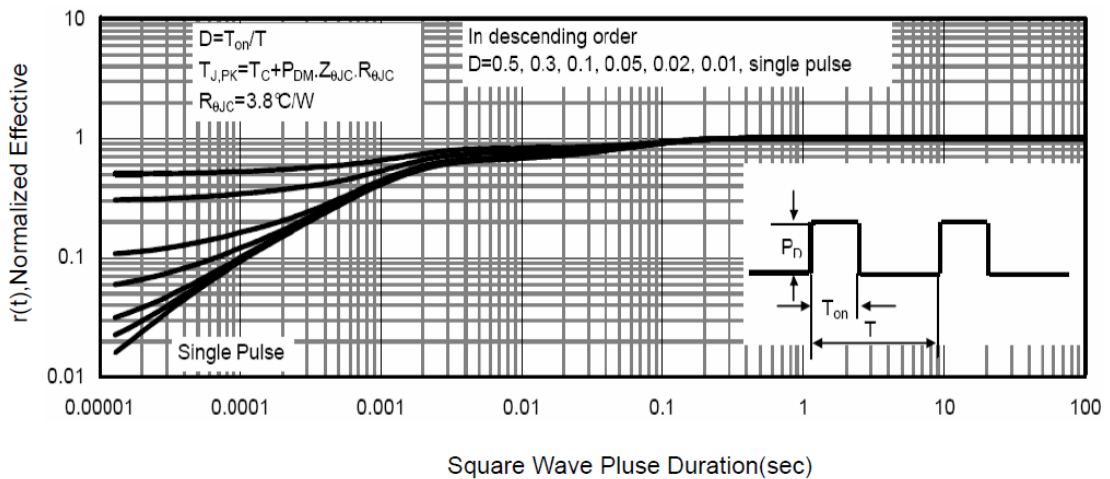
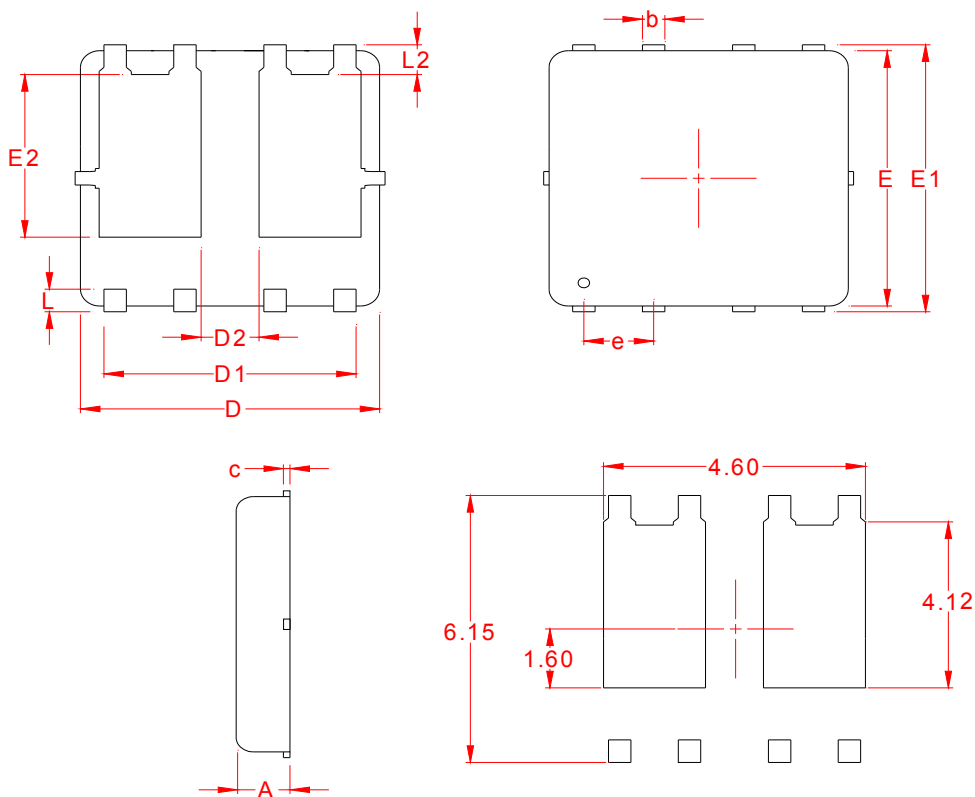


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5x6 EP2



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	—	0.05	0.000	—	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
D2	0.50	0.60	0.75	0.020	0.024	0.030
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.82 BSC			0.150 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	—	0.15	0	—	0.006
L2	0.68 REF			0.027 REF		
θ	0°	—	10°	0°	—	10°

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**SHANGHAI SINO-IC MICROELECTRONICS CO., LTD**

**Add:** Building 3, Room 3401-03, No.200 Zhangheng Road, ZhangJiang Hi-Tech Park, Pudong,  
Shanghai 201203, China

**Phone:** +86-21-33932402 33932403 33932405 33933508 33933608

**Fax:** +86-21-33932401

**Email:** szrxw002@126.com

**Website:** <http://www.sino-ic.net>