

SED2145

P-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Advanced trench technology to provide excellent RDS(ON), low gate charge and low operation voltage. This device is suitable for using as a load switch or in PWM applications.

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

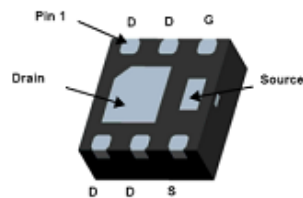
Features

For a single MOSFET

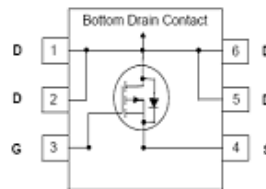
- $V_{DS} = -12V$
- $R_{DS(ON)} = 18.9m\Omega @ V_{GS}=-4.5 @ I_{DS}=-10A$
- $R_{DS(ON)} = 26m\Omega @ V_{GS}=-2.5 @ I_{DS}=-8.9A$

Pin configurations

See Diagram below



DFN2x2-6L Pin Assignment



Schematic diagram

Absolute Maximum Ratings

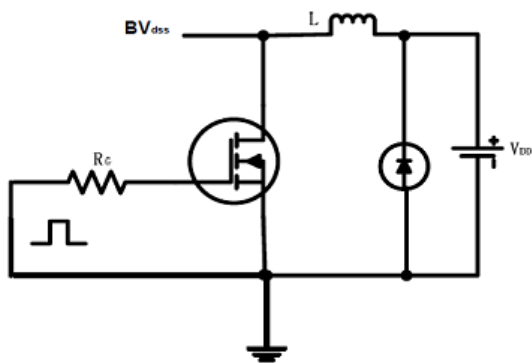
Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	± 8	V
Drain Current	Continuous	I_D	-12	A
	Pulsed		-28	
Total Power Dissipation	@TA=25°C	P_D	2.4	W
Operating Junction Temperature Range		T_J	-55 to 150	°C

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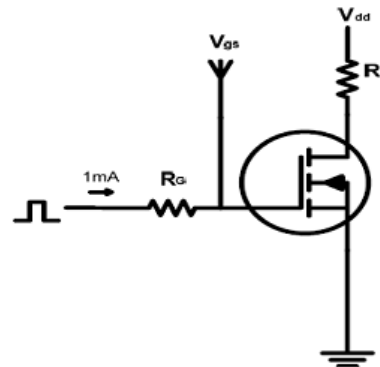
Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	-12			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = -12V, V _{GS} =0V			-1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = 8V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	-0.4		-1	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V, I _D =-10A	-	18.9	-	mΩ
		V _{GS} =-2.5V, I _D =-8.9A		26		
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-6V, f=1MHz	-	2138	-	pF
C _{oss}	Output Capacitance		-	685	-	pF
C _{rss}	Reverse Transfer Capacitance		-	650	-	pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =-4.5V, V _{DS} =-6V, I _D =-10A	-	21	-	nC
Q _{gs}	Gate Source Charge		-	2.5	-	nC
Q _{gd}	Gate Drain Charge		-	6	-	nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =-4.5V, V _{DS} =-6V, R _{GEN} =6Ω, I _D =-10A		30		ns
t _{d(off)}	Turn-Off Delay Time			97		ns
t _{d(r)}	Turn-On Rise Time			48		ns
t _{d(f)}	Turn-Off Fall Time			65		ns
Thermal Resistance						
Symbol	Parameter		Typ	Max		Units
R _{θJC}	Junction to Case		6.9	8		°C/W
R _{θJA}	Junction to Ambient (t ≤ 10s)		52	62.5		°C/W

Test Circuits and Waveform

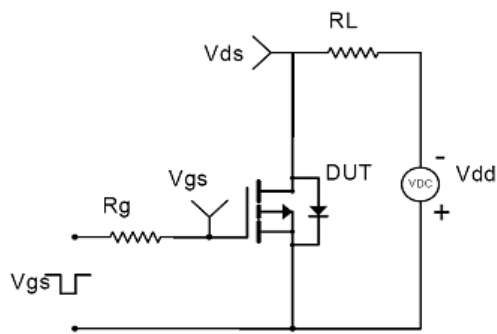
EAS test circuits:



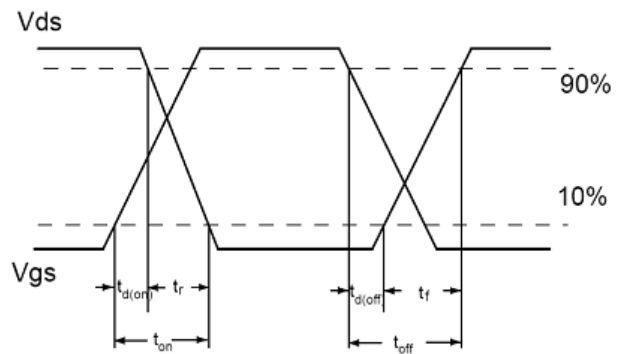
Gate charge test circuit:



Switch time test circuit:



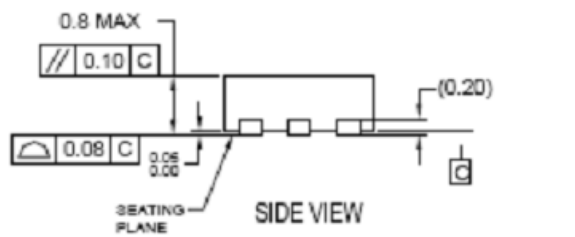
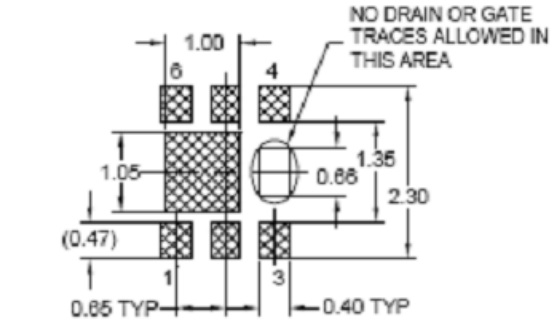
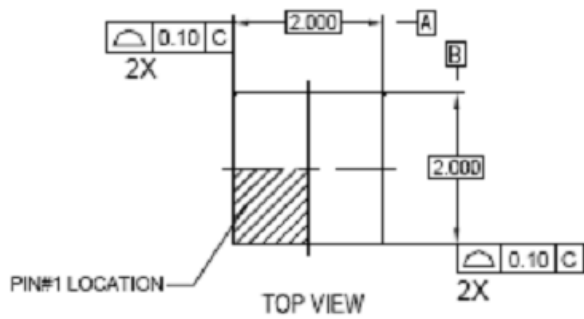
Switch Waveforms:



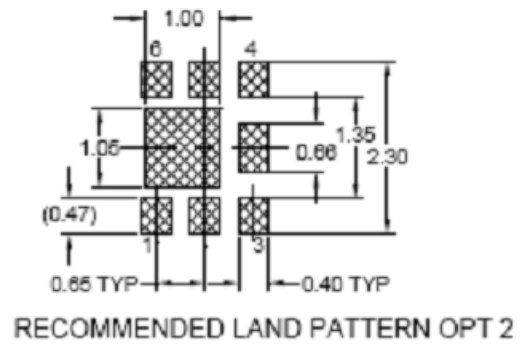
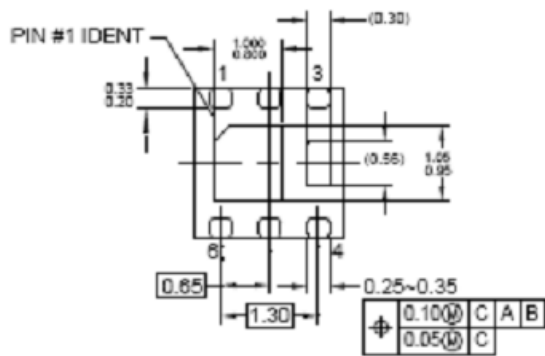
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Package Outline Dimension

DFN2 x 2-6L



RECOMMENDED LAND PATTERN OPT 1



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