

SESRXX
Low Capacitance TVS Diode Array

Revision:B

General Description

The SESRXX is a transient voltage suppressor designed to protect components which are connected to data and transmission lines against ESD. It clamps the voltage just above the logic level supply for positive transients and to a diode drop below ground for negative transients

Applications

- Ethernet – 10/100 Base
- Wireless Communications
- FireWire
- USB power & data line protection
- T1/E1 secondary IC side protection
- Portable electronics

Features

- 150 W Peak Pulse Power per Line (tp=8/20s)
- Low Clamping Voltage
- ESD Protection > 25 kilovolts
- Unidirectional Configuration
- Low Leakage Current
- Protects two I/O lines
- Low capacitance :0.6pF

Complies with the following standards

IEC61000-4-2

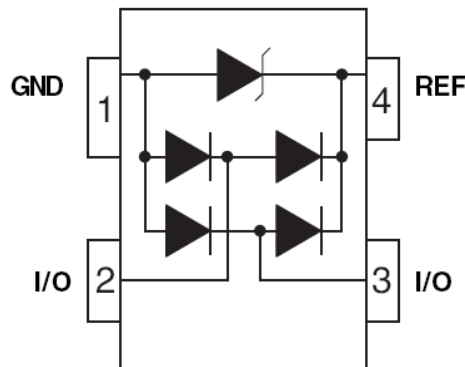
Level 4 15 kV (air discharge)

8 kV(contact discharge)

MIL STD 883E - Method 3015-7 Class 3

25 kV HBM (Human Body Model)

Functional diagram



Absolute Maximum Ratings @ 25°C Unless Otherwise Specified

Symbol	Parameter	Value	Units
P _{PP}	Peak Pulse Power (tp = 8/20μs) - See Fig1.	150	W
T _{STG}	Storage Temperature Range	-55 to 125	°C
T _J	Operating Junction Temperature Range	-55 to 125	°C
V _F	Peak Forward Voltage – I _F =1A, 2/20μs	1.5	Volts

Electrical Characteristics Per Line @ 25°C Unless Otherwise Specified

Electrical Characteristics($T_J=25^\circ\text{C}$ unless otherwise noted)

Part Numbers	V_{BR}			I_T	V_{RM}	I_{RM}	V_F	I_F	C
	Min.	Typ.	Max.				Max.		Typ.
	V	V	V				mA		V
SESR05	6.0	6.6	9.8	1	5.0	1	1.25	200	0.6
SESR12	13.3	14.0	16.5	1	12.0	1	1.25	200	0.6

Note 1:As shown in Figure 5,REF 1is connected to ground, REF 2 is connected to $+V_{cc}$ and input applies to $V_{cc}=5V, V_{sign}=30mV, F=1MHz$

Typical Characteristics

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

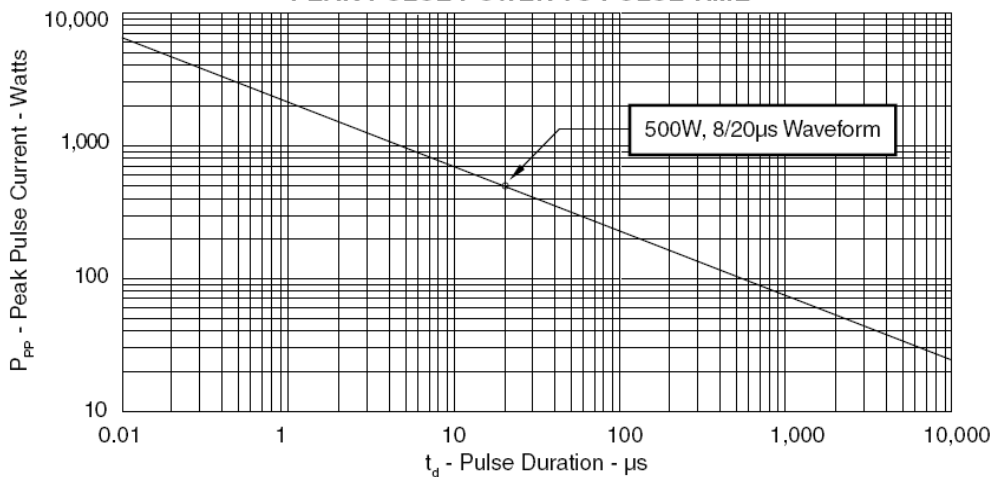
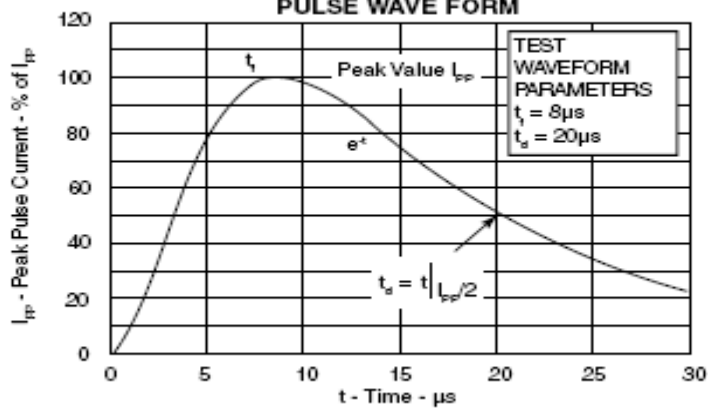
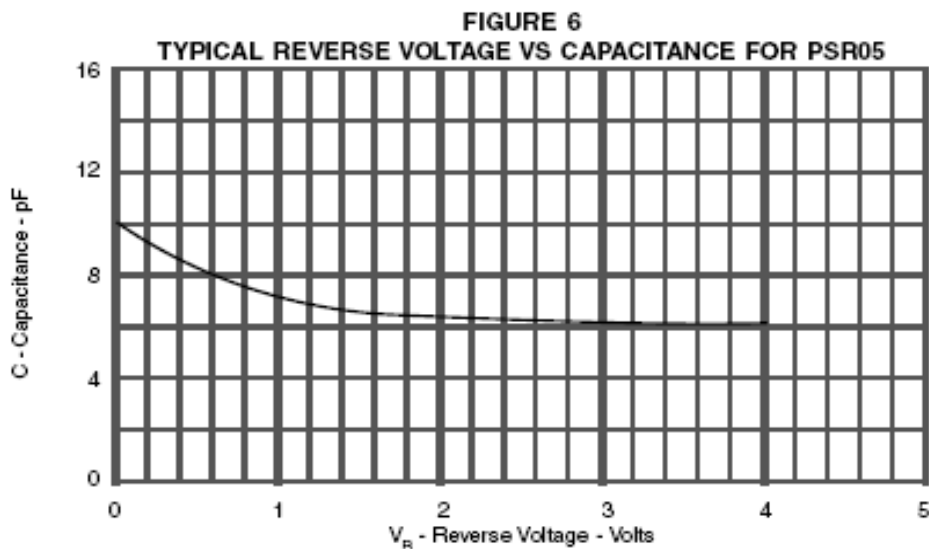
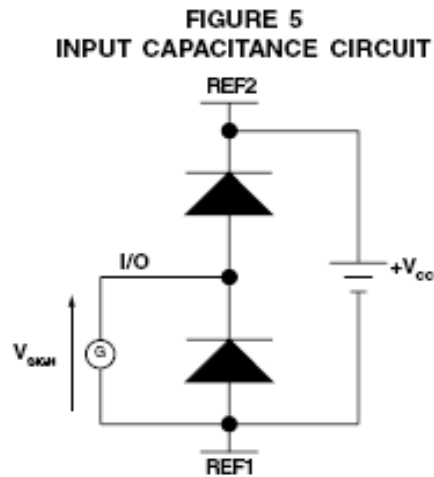
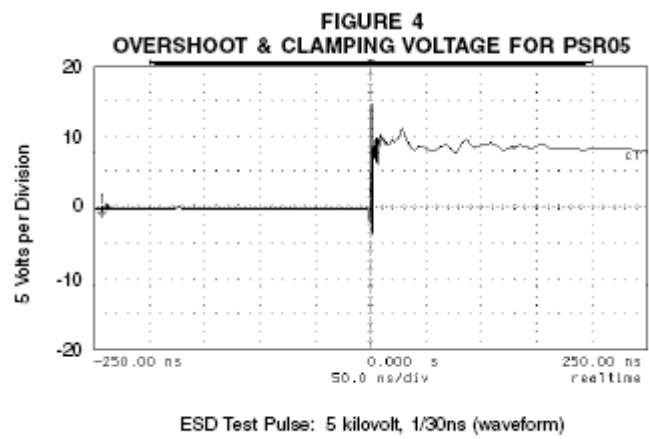
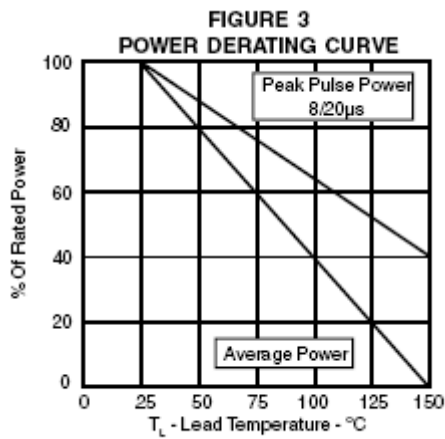


FIGURE 2
PULSE WAVE FORM





COMMON-MODE CONFIGURATION (Figure 1)

Ideal for use in USB applications, two SESR05 devices up to two (2) lines of protection(per device) in a common-mode configuration as depicted in Figure 1.

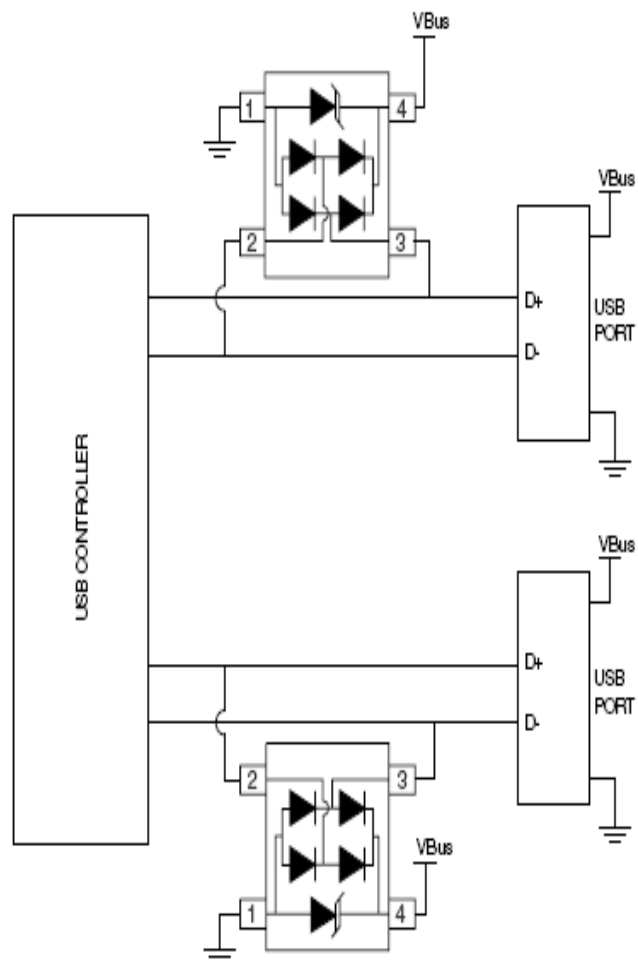
Circuit connectivity is as follows:

- Pins 2 and 3 are connected to the datalines.
- Pins 1 is connected to ground.
- Pin 4 is connected to the databus.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

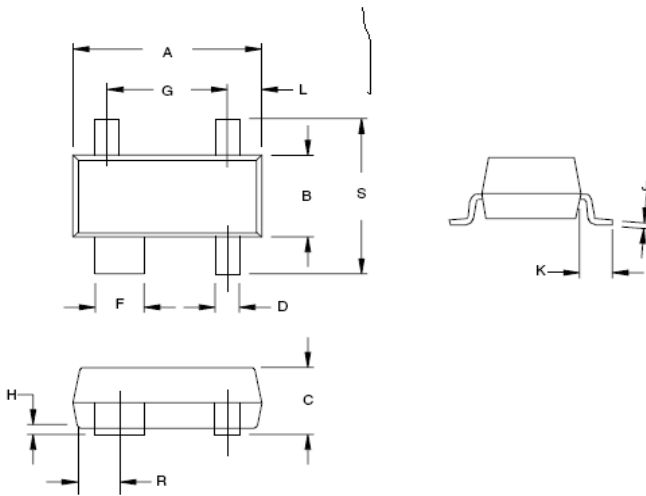
- Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:
 - The protection device should be placed near the input terminals or connectors, th device will divert the transient current immediately before it can be coupled into the nearby traces.
 - The path length between the TVS device and the protected line should be minimized.
 - All conductive loops including power and ground loops should be minimized.
 - The transient current return path to grouor should be kept as short as possible to reduce parasitic inductance.
 - Ground planes should be used whenever possible .For multilayer PCBs, use ground vias.

Figure 1. Typical Common-Mode USB Protection



PACKAGE Mechanical Data

PACKAGE OUTLINE



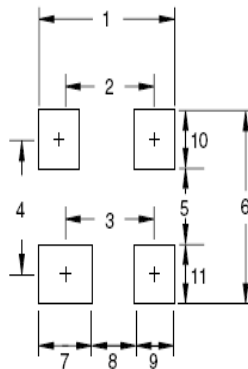
SOT-143



PACKAGE DIMENSIONS

MOUNTING PAD

TYPICAL		
DIM	Millimeters	Inches
1	2.85	0.112
2	2.00	0.079
3	1.80	0.071
4	1.90	0.075
5	1.05	0.041
6	2.75	0.108
7	1.20	0.047
8	0.80	0.031
9	0.85	0.033
10	0.85	0.033
11	0.85	0.033



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.84	1.14	0.033	0.045
D	0.39	0.50	0.015	0.020
F	0.79	0.93	0.031	0.037
G	1.78	2.03	0.070	0.080
H	0.013	0.10	0.0005	0.004
J	0.08	0.15	0.003	0.006
K	0.46	0.60	0.018	0.024
L	0.445	0.60	0.0175	0.024
R	0.72	0.83	0.028	0.033
S	2.11	2.48	0.083	0.098

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