Bidirectional charger with step-down discharging and step-up charging

1 Features

- 5A continuous output current capability
- 4.5V to 36V wide operating input range
- 2V to 32 V wide output range
- Integrated 40V, 9mΩ high side and 40V, 9mΩ low side power MOSFET switches
- Single Inductor, bidirectional charge Controller for Step-Down discharge and Step-Up charge
- Dynamical programming of input current, Output current and Output voltage using PWM signal or analog signal
- 1 Cell to 6 Cells battery charge management
- Adjustable Switching Frequency using resistor
- Frequency dithering for good EMI performance
- Integrated 2-A MOSFET Gate Drivers
- Comprehensive protection features including Output Short Protection (OSP), Cycle-by-Cycle input and output Peak Current Limit, thermal regulation, thermal shutdown, input UVLO, input OVP, output OVP etc.
- Input or Output Average Current Limiting with stable CC loop
- 5V/55mA low I_q LDO to power system MCU
- QFN6x6-48 Package

2 Applications

- Automotive Start-Stop Systems
- Backup Battery and Super capacitor Charging
- HUB / Power Bank / Car Charger
- Industrial PC Power Supplies
- USB Power Delivery

3 Description

PL8405Q integrates a high efficiency synchronous step-down switching regulator, which includes a 40V, 9mΩ high side and a 40V, 9mΩ low side MOSFETs to provide 5A continuous load current over 6.5V to 36V wide operating input voltage with 33V input over voltage protection. PL8405Q can operate at charger mode for 1, 2, 3, 4, 5 and 6 cells battery charge.

PL8405Q employs Constant ON time control. The switching frequency could be set to 150kHz, 300kHz, 600kHz or 1200kHz based on different resistor value between FREQ pin and GND pin. The device also features a programmable soft-start function and offers all kinds of protection features including cycle-by-cycle current limiting, input under voltage lockout (UVLO), output over voltage protection (OVP), input Over Voltage Protection, thermal shutdown and output short protection etc.

PL8405Q provides voltage control loop, constant current loop, and thermal regulation loop.

4 Typical Application Schematic

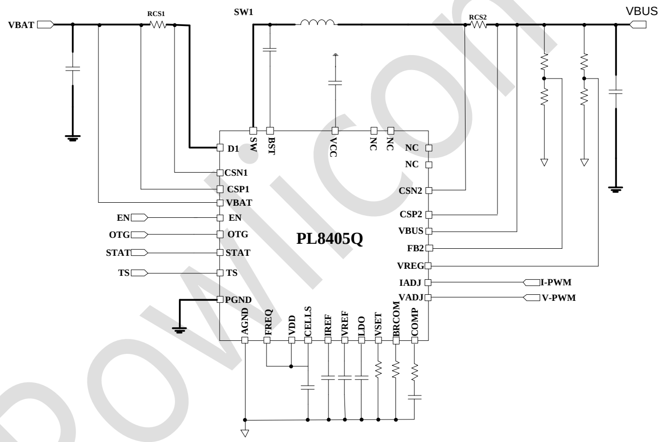


Fig. 1 Application Schematic

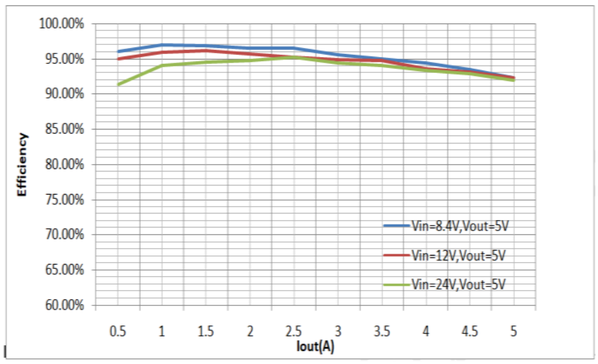


Fig.2 Efficiency

5 Pin Configuration and Functions

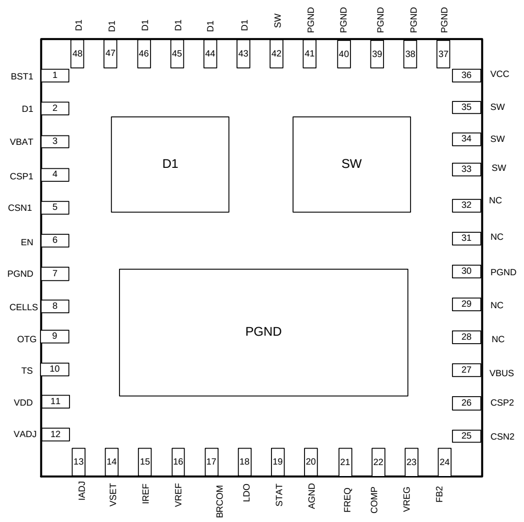


Fig. 3 Pin-Function (QFN6X6-48)

Pin		Description
Number	Name	
1	BST1	Boost pin for high side MOSFET driver1.
2,43,44,45,46,47,48	D1	Power node of VBAT. Connect to BAT input port. Work as the power output of the converter when in charging mode, and power input in discharging mode.
3	VBAT	Connect to the VBUS rail.
4	CSP1	The positive input of input current sense.
5	CSN1	The minus input of input current sense.
6	EN	Logic High will enable the converter. Logic Low will disable the whole PL8405Q except LDO. Only LDO is working to power system MCU when EN is low.
7,30,37,38,39,40,41	PGND	Power ground.
8	CELLS	Connect a resistor divider between VDD and GND to program battery cells.
9	OTG	Connect OTG to 0 to set PL8405Q in battery charging mode. Connect OTG to VDD to set PL8405Q in battery discharging mode.
10	TS	Batter temperature sense
11	VDD	5.4V power supply for PL8405Q control core.
12	VADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on VREF pin. Connect this pin to VDD will force VREF to constant 2V.
13	IADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on IREF pin. Connect this pin to VDD will force IREF to 2V.
14	VSET	Connect a resistor between VSET and GND to program battery cell type (4.2V, 4.35V, 4.4V, 4.5V) when OTG is low and PL8405Q is working in battery charging mode. When OTG is higher than 1.2V, voltage on VSET pin will be proportional to voltage difference between CSP2 and CSN2. Application processor can use this information to monitor discharging current in battery discharging mode.
15	IREF	Reference voltage for input and output current limiting loop.
16	VREF	Voltage reference for voltage control loop
17	BRCOM	Battery internal resistance compensation. The voltage on this pin will be proportional to voltage difference between CSP1 and CSN1. Application processor can use this information to monitor charging current in battery charging mode.

18	LDO	Low quiescent current 5V/55mA LDO. Directly powered from VBAT pin. LDO can be used as power supply for application processor such as MCU. When EN is low, only this LDO will be active to power MCU and keep low quiescent current for the whole system.
19	STAT	Charging status display when OTG=Low. PGOOD signal when OTG=High.
20	AGND	Analog ground. Connect PGND and AGND together at the thermal pad under IC.
21	FREQ	Connect to GND to set the switching frequency at 150kHz. Connect this pin to VDD to set switching frequency at 300kHz. Connect to a resistor divider between VDD and GND to set frequency to 600k and 1200k Hz.
22	COMP	Error Amplifier output.
23	VREG	Add a resistor divider to program VBUS regulation voltage. When VBUS is pulled down to be close to VREG setting point due to heavy charging current in battery charging mode, the VREG regulation loop will take over the control and lower down charging current to keep VBUS from being further pulled down. VREG is not active in discharging mode.
24	FB2	VBUS voltage feedback. Connect a resistor divider between VBUS and GND to FB2 to program VBUS voltage in battery discharging mode.
25	CSN2	The minus input of output current sense.
26	CSP2	The positive input of output current sense.
27	VBUS	Connect to the VBUS rail.
28,29, 31,32	NC	
33,34, 35,42	SW1	Connect this pin to the Switching point 1 of the power stage.
36	VCC	6.6V power supply for high side and low side driver.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL8405Q	**PL8405QIQN48**	**QFN6*6-48**	**2500**	**8405Q** **RAAYMD**

PL8405Q: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VBAT, VBUS, CSN1, CSN2, CSP1, CSP2, SW	-0.3	40	V
BST to SW	-0.3	7	
VCC to GND	-0.3	7	
CSP1 to CSN1	-0.3	0.6	
CSP2 to CSN2	-0.3	0.6	
VBAT to CSP1, CSN1	-0.3	0.6	
VBUS to CSP2, CSN2	-0.3	0.6	
Other Pins to GND	-0.3	6	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VBAT，VBUS	3.6	32	V
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN4X4-32	Unit
θ_{JA}	Junction to ambient thermal resistance	44	°C/W
θ_{JC}	Junction to case thermal resistance	9	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1” square of 1 oz copper.

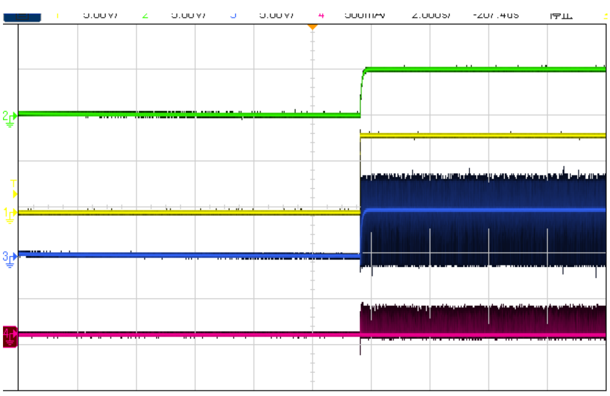
7.5 Electrical Characteristics (Typical at VBAT = 12V, T_J =25°C, unless otherwise noted.)

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VBAT	Battery voltage		4.5		32	V
$I_{Q\_}$ VBAT	VBAT Shutdown Current	EN=0V, VBAT=7.2V		15		uA
	VBAT Supply Current	No Switching, FB=2.1V		1000		uA
VBUS	Bus line voltage		2		30	V
I_{Q}_VBUS	VBUS Shutdown Current	EN=0V, VBUS=7.2V		15		uA
	VBUS Supply Current	No Switching, battery fully charged		1200		uA
V_{VCC}	Driver power supply voltage	VBAT =15V		6.6		V
V_{VDD}	Control core power supply voltage	VBAT =15V		5.4		V
V_{LDO}	LDO output voltage	VBAT =15V		5		V
I_{LDO}	LDO output current	V_{LDO} =5V			55	mA
UVLO/EN						
$VBAT_{\_UV}$	VBAT UVLO Rising			3.5		V
	UVLO Hysteresis			300		mV
$VBUS_{\_UV}$	VBUS UVLO Rising			3.5		V
	UVLO Hysteresis			300		mV
V_{EN_UV}	Operation Threshold		1.1	1.2	1.3	V
	Hysteresis			200		mV
OTG						
V_{TH_OTG}	OTG high voltage threshold			1.2		V
V_{HY_OTG}	OTG Hysteresis		200			mV
VREF						
V_{VREF_Dischg}	VREF voltage in discharge mode	VADJ connected to VDD		2		V
V_{VREF_chg}	VREF voltage in charge mode	VADJ connected to VDD		1.8		V
Battery charge setting						
V_{cell_num}	Battery cells number setting. V_{cell} is set by VSET pin.	VCELLS=0-0.9V		1*V_{cell}		V
		VCELLS=4.5-5.5V		2*V_{cell}		V
		VCELLS=0.9-1.8V		3*V_{cell}		V
		VCELLS=1.8-2.7V		4*V_{cell}		V
		VCELLS=2.7-3.6V		5*V_{cell}		V
		VCELLS=3.6-4.5V		6*V_{cell}		V
V_{TH_TRKL}	Trickle charge threshold. VBAT voltage			3		V
V_{HY_TRKL}	Trickle charge Hysteresis. VBAT voltage			0.5		V
V_{RECHAG}	Battery recharge voltage			4		V
$VBAT_{\_FULL}$	Batter full charge voltage	V_{VSET} :0.4-0.9V Rset:220k		4.2		V
		V_{VSET} :0.9-1.9V Rset:430k		4.35		V
		V_{VSET} :1.9-5.5V, short VSET pin to VDD.		4.4		V
		V_{VSET} :0-0.4V, short VSET pin to GND.		4.5		V
V_{REG}	Charge Input regulation voltage	VREG		1.2		V
Control loop						
V_{FB}	VFB regulation voltage in discharging mode	FB voltage		2		V
G_{mEA}	Error amplifier gm			450		uS
I_{SINK}	COMP sink/source current	VFB=VREF+100mV		15		uA
I_{SOURCE}	COMP source current	VFB=VREF-100mV		20		uA
I_{FB}	FB bias current	FB2 in regulation			100	nA
Frequency						
F_{SW}	Switching Frequency	FREQ 0-0.4V, short FREQ pin to GND.		150		KHz
		FREQ 1.8-5.4V, short FREQ pin to VDD.		300		KHz
		FREQ 0.4-0.85V		600		KHZ
		FREQ 0.85-1.8V		1200		KHZ

Current Limit				
I_{CCLIM_BAT}	Battery average current Limit, V_{CSP1}- V_{CSN1}	Discharging mode	80	mV
		Charging mode	40	mV
I_{CCLIM_BUS}	Bus average current Limit, V_{CSP2}- V_{CSN2}	Discharging mode	40	mV
		Charging mode	80	
Output Protection				
V_{OVP}	Output over voltage threshold		110	%
V_{UVP}	Output under voltage threshold		50	%
VADJ, IADJ				
V_{TH_VADJ} (Note 4)	VPWM low voltage		0.4	V
	VPWM high voltage		2.5	V
V_{TH_IADJ} (Note 4)	IPWM low voltage		0.4	V
	IPWM high voltage		2.5	V
T_{SD} (Note 4)	Thermal Shutdown Threshold		150	°C
T_{HYS} (Note 4)	Thermal Shutdown Hysteresis		20	°C

Notes:
4) Guaranteed by design.

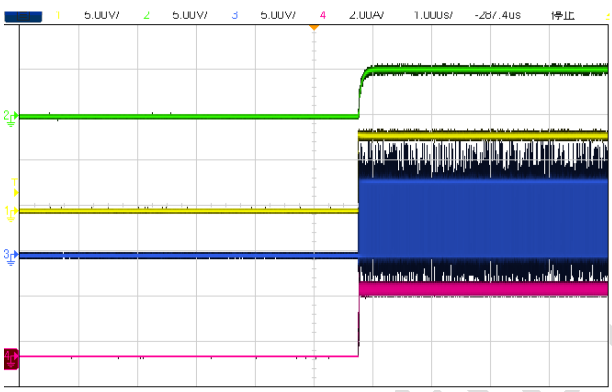
8 Typical Characteristics



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

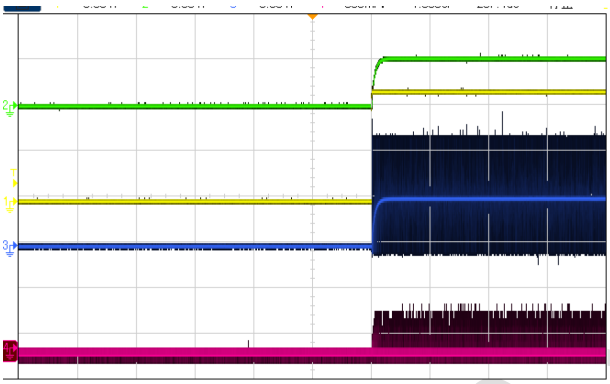
Fig.4 Start up waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

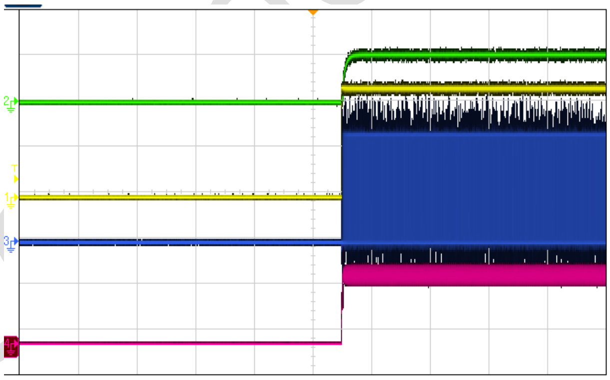
Fig.5 Start up waveform, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

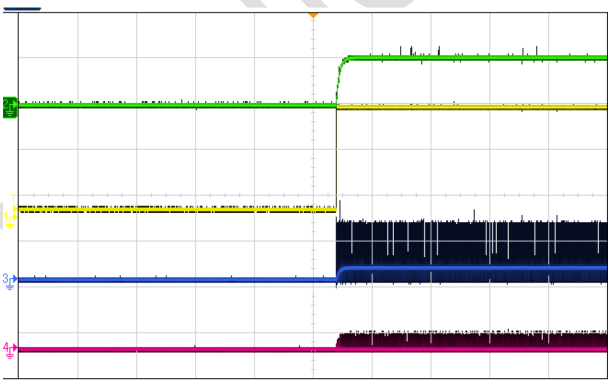
Fig.6 Start up waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

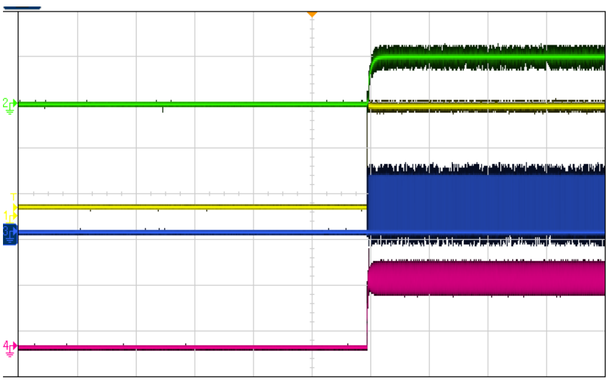
Fig.7 Start up waveform, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

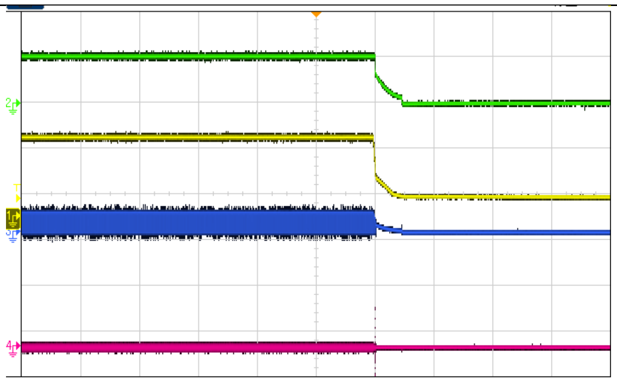
Fig.8 Start up waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

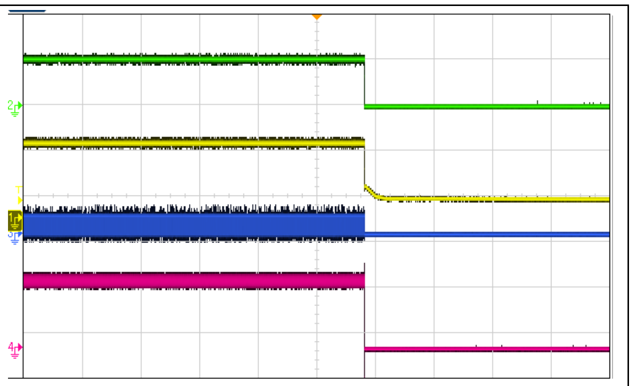
Fig.9 Start up waveform, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

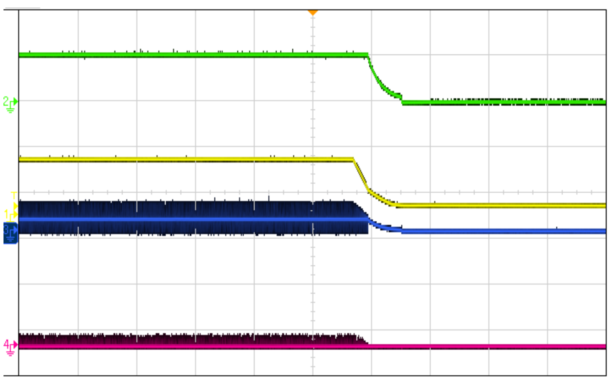
Fig.10 Shut down waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

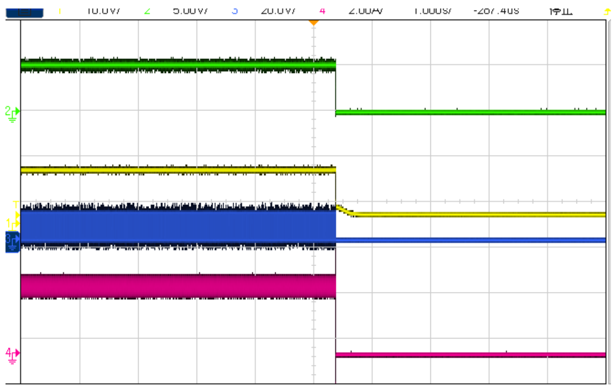
Fig.11 Shut down waveform, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

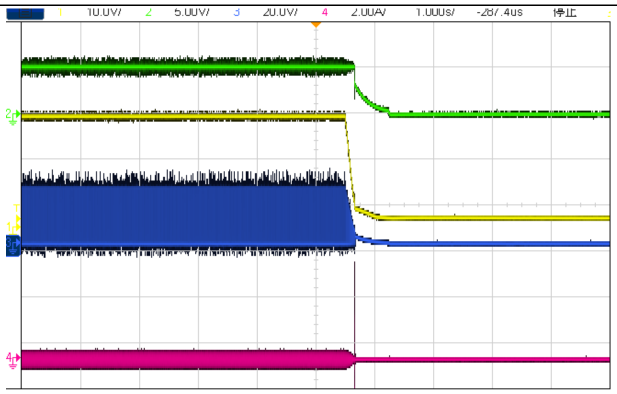
Fig.12 Shut down waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

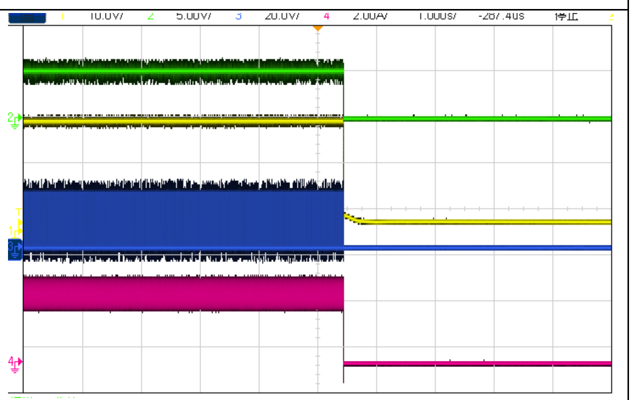
Fig.13 Shut down waveform, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

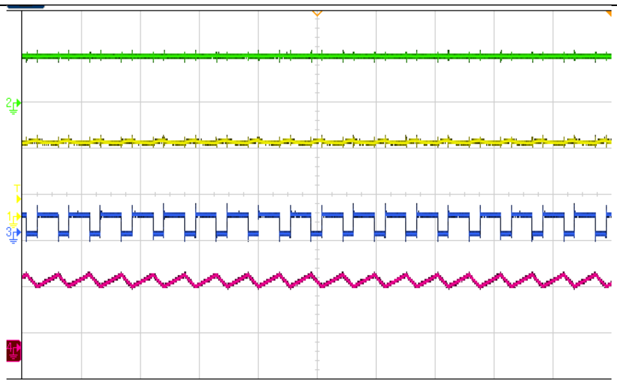
Fig.14 Shut down waveform, Iout =0A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

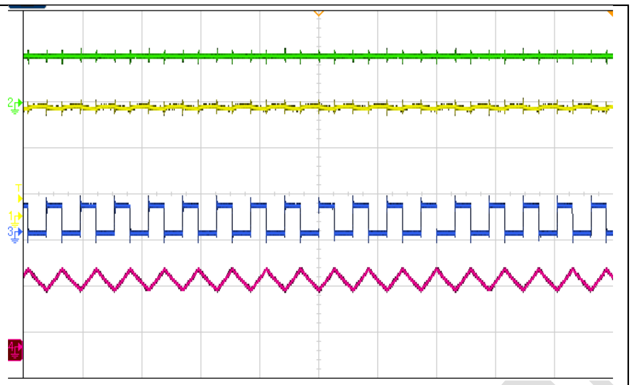
Fig.15 Shut down waveform, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

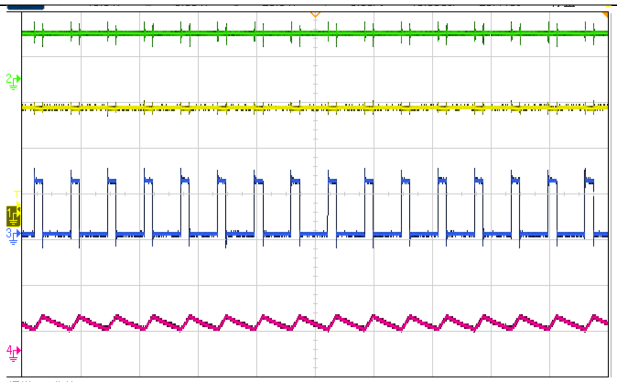
Fig.16 Steady State, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

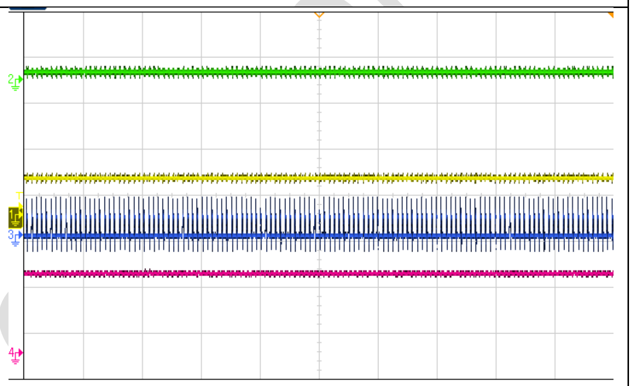
Fig.17 Steady State, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

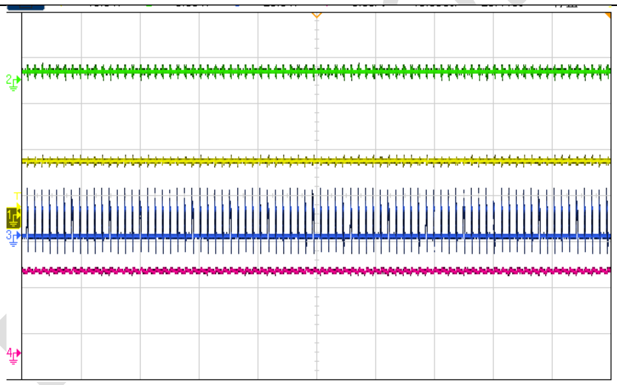
Fig.18 Steady State, Iout =5A



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=8.4V Vout=5V

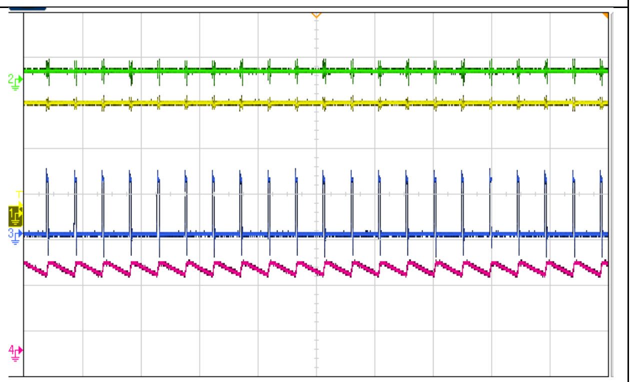
Fig.19 Short Circuit waveform



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=5V

Fig.20 Short Circuit waveform



CH1:Vin CH2:Vout CH3:SW CH4:IL

Vin=24V Vout=5V

Fig.21 Short Circuit waveform

9 Detailed Descriptions

9.1 Overview

PL8405Q integrates a high efficiency synchronous step-down switching regulator, which includes a 40V, 9mΩ high side and a 40V, 9mΩ low side MOSFETs to provide 5A continuous load current over 6.5V to 36V wide operating input voltage with 33V input over voltage protection. PL8405Q can operate at charger mode for 1, 2, 3, 4, 5 and 6 cells battery charge.

PL8405Q employs Constant ON time control. The switching frequency could be set to 150kHz, 300kHz, 600kHz or 1200kHz based on different resistor value between FREQ pin and GND pin. The device also features a programmable soft-start function and offers all kinds of protection features including cycle-by-cycle current limiting, input under voltage lockout (UVLO), output over voltage protection (OVP), input Over Voltage Protection, thermal shutdown and output short protection etc.

9.2 Functional Block Diagram

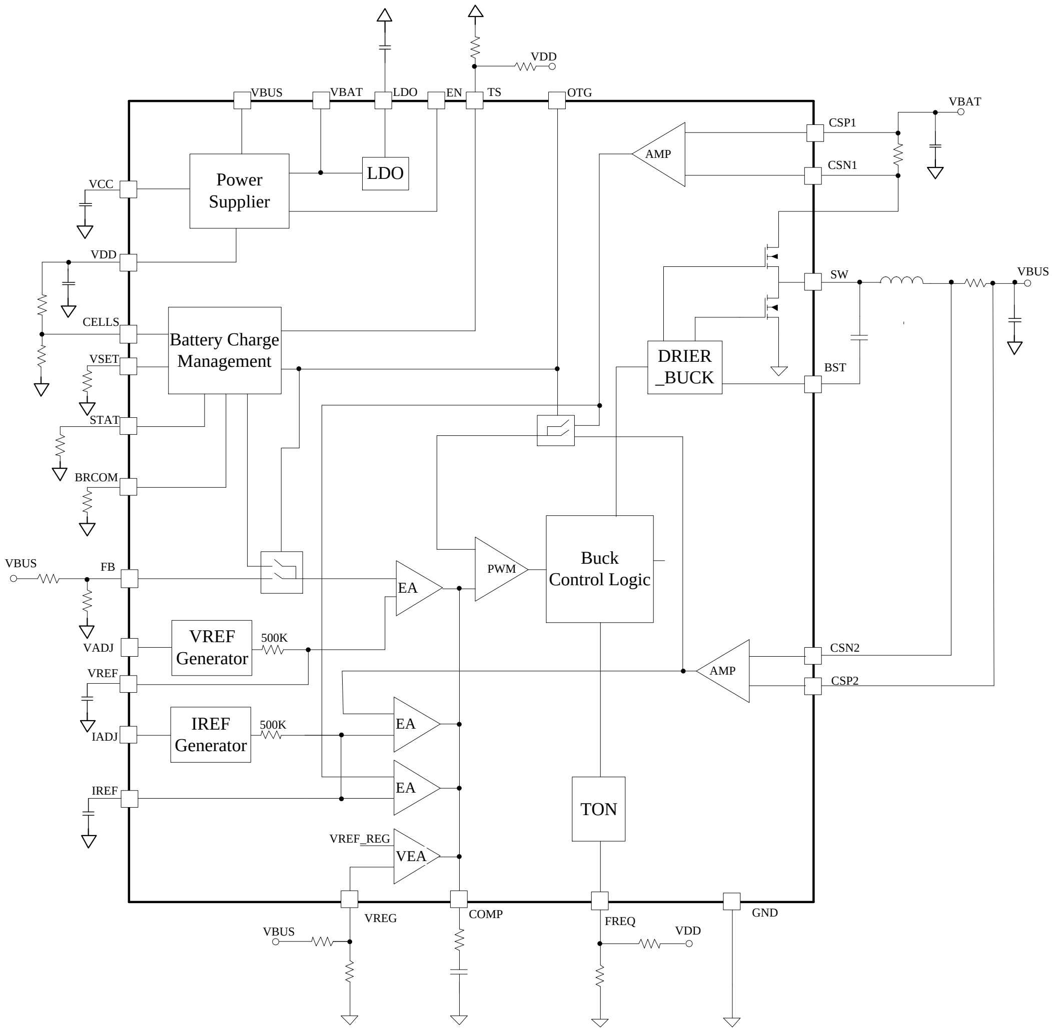


Fig. 22 PL8405Q Block Diagram

9.3 Enable/UVLO

When EN is greater than 1.2V operating threshold, the control loop starts to work and regulate output to target voltage. When EN pin is below the standby threshold (1.1V typical), PL8405Q stops working with only LDO is active to power MCU. EN is pulled high to 4V internally using a 2Meg resistor.

9.4 Over current Protection and short circuit protection

PL8405Q provides cycle-by-cycle current limit to protect against over current and short circuit conditions. When VOUT is drop to UV threshold, PL8405Q will go into hiccup mode to lower down power consumption.

9.5 Average Input/Output Current Limiting

PL8405Q provides optional average current limiting capability to limit either the input or the output current. The average current limiting circuit uses an additional current sense resistor connected in series with the input supply or output voltage of the converter. A current sense gm amplifier with inputs at the CSP1 and CSN1 pins monitors the voltage across the sensing resistor and compares it with an internal 40 mV reference. If the drop across the sense resistor is greater than 40 mV, the gm amplifier regulates COMP voltage to lower down input or output current. The target constant current is given by Equation 1:

$$I_{CL(AVG)} = \frac{40\ mV}{R_{SNS}} \quad (1)$$

The average current loop can be disabled by shorting CSP1 to CSN1 or CSP2 to CSN2.

9.6 Frequency Setting (FREQ) and frequency dithering

PL8405Q switching frequency can be programmed at 150 kHz, 300 kHz or 600 kHz and 1200 kHz by voltage at FREQ pin to GND. When FREQ is connected to AGND, the switching frequency is set at 150 kHz. When FREQ is connected to VDD, the switching frequency is set at 300 kHz. A voltage divider between VDD and GND pin can be used to program switching frequency if 600 kHz or 1200 kHz is required.

9.7 Thermal Shutdown

PL8405Q is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 160°C (typical). The soft-start capacitor is discharged when thermal shutdown is triggered and the gate drivers are disabled. The converter automatically restarts when the junction temperature drops by the thermal shutdown hysteresis of 15°C below the thermal shutdown threshold.

9.8 Thermal sensing TS

PL8405Q use TS pin to sense battery temperature. A voltage divider can be used at TS pin to program the protection trigger point in charging mode or discharging mode.

9.9 Battery internal resistor compensation

BRCOMP pin is used to compensate battery internal resistance during high current charging period. A resistor between BRCOMP pin and GND is used to program voltage compensation as the following equation:

$$\Delta Vbat = \frac{Rcs * Ibat * Aisense * 8k}{Rbrcom} \quad (2)$$

$\Delta Vbat$ is the compensated batter voltage change. Rcs is current sensing resistor at VBAT side. Ibat is battery charging current. Aisense is current sensing gain at VBAT side, which is normally around 50. Rbrcom is resistor value between BRCOM pin and GND.

9.10 Status display STAT and power good signal

PL8405Q use STAT pin as charging status display in battery charging mode and power good signal in discharging mode. When single battery voltage is less than 3V, STAT will send out a PWM signal at 0.6s period with 50% duty cycle. When battery voltage is higher than 3V, STAT pin will be constant low to indicate high current charging status. When battery voltage is higher than 4V and charging current is lower than the termination current level, STAT will send out constant high signal to indicate the battery is charged fully.

In discharging mode, STAT will act as a power good signal. STAT will be constant high when FB voltage is not in OV or UV status.

9.11 VREF and IREF

VREF pin is the final reference voltage used in the voltage regulation loop. When VADJ is connected to VDD, VREF will be 2V in discharging mode and 1.8V in charging mode. When VADJ is connected to a PWM signal, PWM signal will first be chopped to 2V and filter out using an internal resistor and external capacitor on VREF pin. The capacitor on VREF pin is also acting as soft-start capacitor at power up or in output voltage transition period. It is recommend using a relatively large capacitor such as 470nF for VREF pin and IREF pin.

The same mechanism works for IADJ and IREF pin.

10 Applications and Implementation

The typical application on the first page is a basic PL8405Q application circuit. External component selection is driven by the load requirement, and begins with the selection of RS1, RS2 and the inductor value. Next, the power MOSFETs need to be selected. Finally, C_{IN} and C_{OUT} are selected. This circuit can be configured for operation up to an input voltage of 32V.

10.1 R_{CS} Selection

As shown in Figures 4 and , Figures 5, input/output current sense resistor RCS1/RCS2 should be placed between the bulk capacitor for VBAT/VBUS and the decoupling capacitor. A low pass filter formed by RF and CF is recommended to reduce the switching noise and stabilize the current loop. If input/output current limit is not desired, then CSP1/CSN1 and CSP2/CSN2 pins should be shorted to either VBAT or VBUS.Place CSP1/CSN1, CSP2/CSN2 symmetrically and keep them away switching signals such as BST SW, VBAT, VBUS etc.

10.2 Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L > \frac{V_{OUT}*(V_{IN(MAX)}-V_{OUT})*1000}{f*\Delta I_L*V_{IN(MAX)}}\ uH \quad (3)$$

where: f is operating frequency, kHz

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

10.3 C_{IN} and C_{OUT} Selection

Input capacitor C_{IN} is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current, input RMS current is given by:

$$I_{CIN}=I_{OUT(MAX)}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

This input current has a maximum at $V_{IN} = 2V_{OUT}$, $I_{CIN(MAX)} = I_{OUT(MAX)}/2$.

The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage.

V_{OUT} ripple is given by:

$$\Delta V_{OUT} \le \Delta I_L*\left(ESR+\frac{1}{8*f*C_{OUT}}\right) \quad (5)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

10.4 Output voltage setting

The PL8405Q output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The 1% resistance accuracy of this resistor divider is preferred. The resultant feedback signal is compared with the internal precision 2V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 2V*\left(1+\frac{R_1}{R_2}\right) \quad (6)$$

Where R_1 is the upper resistor and R_2 is the lower resistor in the feedback network.

11 PCB Layout

11.1 Guideline

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R1 and R2, should be kept close to the FB pin. Keep VBUS sensing path away from noisy nodes and preferably through a layer on the other side of shielding layer.
2. The input /output bypass capacitor must be placed as close as possible to the VBAT/VBUS pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VBAT and VBUS pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. Current sensing pairs (CSP1,CSN1), (CSP2,CSN2) need to be placed carefully, Layout the lines symmetrically and keep them away from noisy nodes such as BST, SW etc. Connect these nodes directly to the two terminals of current sensing resistors Rcs1, Rcs2 to form an accurate Kelvin connection.

11.2 Application Examples

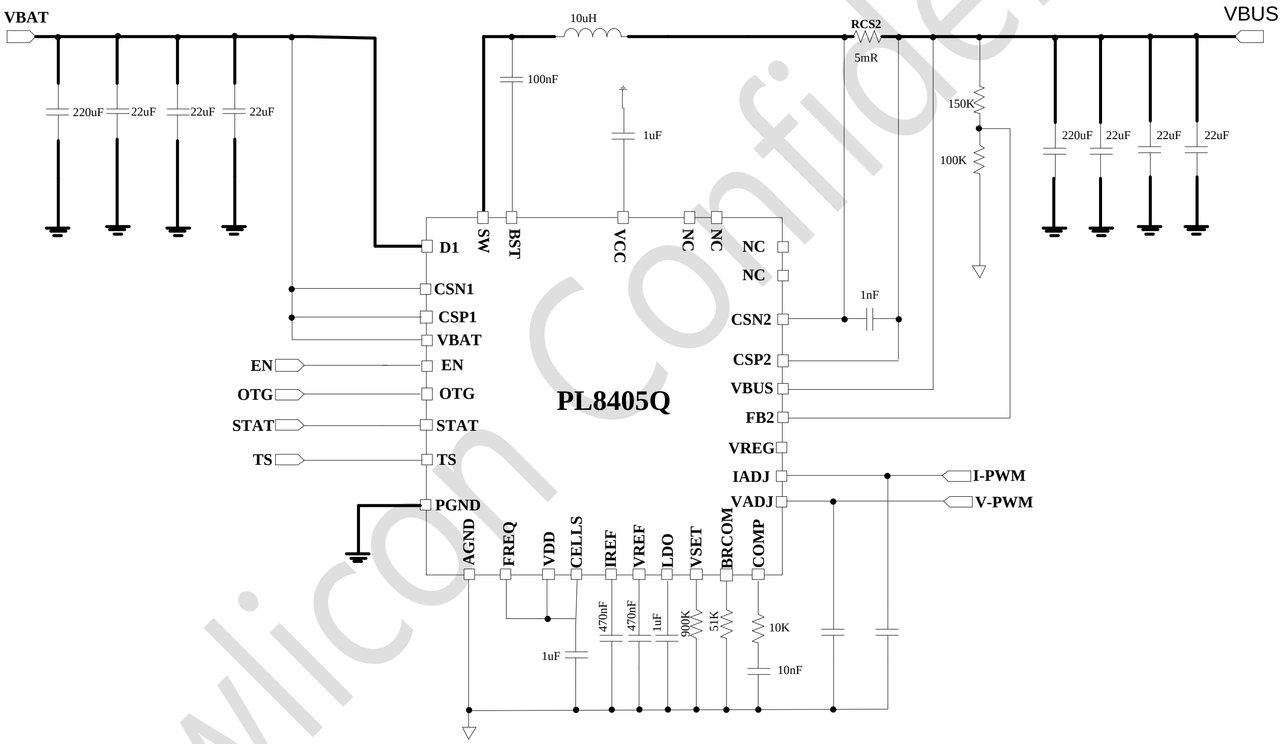
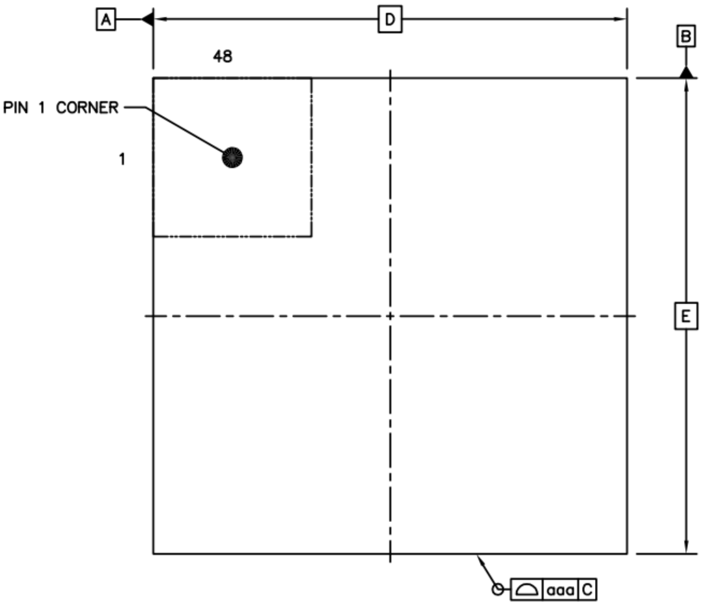


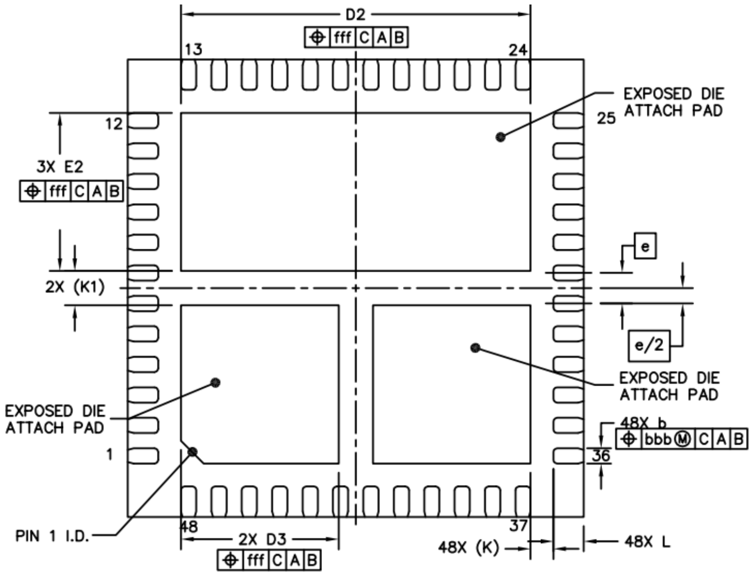
Fig. 23 Application Schematic (VABT:24V VBUS:5V IOUT:5A)

12 Packaging Information

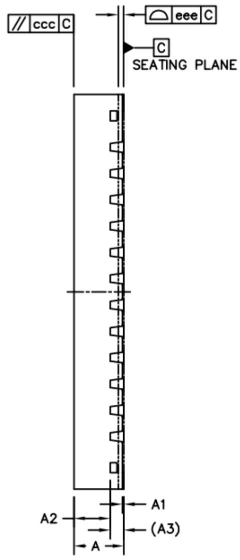


TOP VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	4.5	4.6	4.7
		D3	1.975	2.075	2.175
	Y	E2	1.975	2.075	2.175
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PAD TO PAD		K1		0.45 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	



BOTTOM VIEW



SIDE VIEW

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