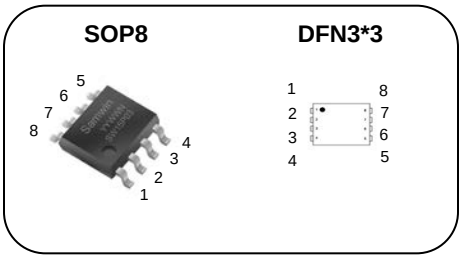
*P-channel Enhanced mode SOP8/DFN3*3 MOSFET*

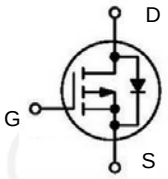
Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 14mΩ)@V_{GS}=-4.5V
  Low $R_{DS(ON)}$ (Typ 10mΩ)@V_{GS}=-10V
- Low Gate Charge (Typ 48nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: Adaptor Input Switch for Notebook PC



SOP8/DFN3*3: 4.Gate 5,6,7,8.Drain 1,2,3.Source

BV_{DSS} : -30V
I_D : -15A
$R_{DS(ON)}$: 14mΩ @V_{GS}=-4.5V
10mΩ @V_{GS}=-10V



General Description

This power MOSFET is produced with advanced technology of SAMWIN.
This technology enable the power MOSFET to have better characteristics, including Fast switching time, low on resistance, low gate charge and especially excellent Avalanche characteristics.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW K 15P03	SW15P03	SOP8	REEL
2	SW H 15P03	SW15P03	DFN3*3	REEL

Absolute maximum ratings

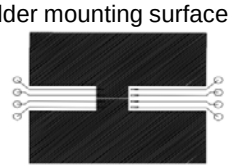
Symbol	Parameter		Value		Unit
			SOP8	DFN3*3	
V_{DSS}	Drain to source voltage		-30		V
I_D	Continuous drain current (@T_C=25°C)		-15*		A
	Continuous drain current (@T_C=100°C)		-9.5*		A
I_{DM}	Drain current pulsed	(note 1)	-60		A
V_{GS}	Gate to source voltage		±25		V
E_{AS}	Single pulsed avalanche energy	(note 2)	81		mJ
dv/dt	Peak diode recovery dv/dt	(note 3)	5		V/ns
P_D	Total power dissipation (@T_a=25°C)		2.5	2.1	W
	Derating factor above 25°C		0.02	0.017	W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature		-55 ~ + 150		°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value		Unit
		SOP8	DFN3*3	
R_{thja}	Thermal resistance, Junction to ambient（note）	50	60	°C/W

Note: R_{thja} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{thjc} is guaranteed by design while R_{thca} is determined by the user's board design.



SOP8： 50°C/W on a 1 in^2 pad of 2oz copper.
DFN3*3：60°C/W on a 1 in2 pad of 2oz copper.

Electrical characteristic (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=-250uA	-30			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=-250uA, referenced to 25°C		0.02		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=-30V, V_{GS}=0V			-1	uA
		V_{DS}=-24V, T_C=125°C			-50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=-25V, V_{DS}=0V			-100	nA
	Gate to source leakage current, reverse	V_{GS}=25V, V_{DS}=0V			100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=-250uA	-1		-2.5	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=-4.5V, I_D=-7.5A		14	22	mΩ
		V_{GS}=-10V, I_D=-7.5A		10	14	mΩ
G_{fs}	Forward transconductance	V_{DS}=-10V, I_D=-7.5A		29		S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		3290		pF
C_{oss}	Output capacitance			344		
C_{rss}	Reverse transfer capacitance			277		
$t_{d(on)}$	Turn on delay time	V_{DS}=-15V, I_D=-15A, R_G=25Ω, V_{GS}=-10V (note 4,5)		15		ns
t_r	Rising time			90		
$t_{d(off)}$	Turn off delay time			214		
t_f	Fall time			150		
Q_g	Total gate charge	V_{DS}=-24V, V_{GS}=-10V, I_D=-15A (note 4,5)		48		nC
Q_{gs}	Gate-source charge			7		
Q_{gd}	Gate-drain charge			10		
R_g	Gate resistance	V_{DS}=0V, Scan F mode		14		Ω

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			-15	A
I_{SM}	Pulsed source current				-60	A
V_{SD}	Diode forward voltage drop.	I_S=-15A, V_{GS}=0V			-1.4	V
t_{rr}	Reverse recovery time	I_S=-15A, V_{GS}=0V, dI_F/dt=100A/us		17		ns
Q_{rr}	Reverse recovery charge			3.5		nC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L =4.5mH, I_{AS} =-6A, V_{DD} = -25V, R_G=25Ω, Starting T_J = 25°C
3. I_{SD} ≤-15A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

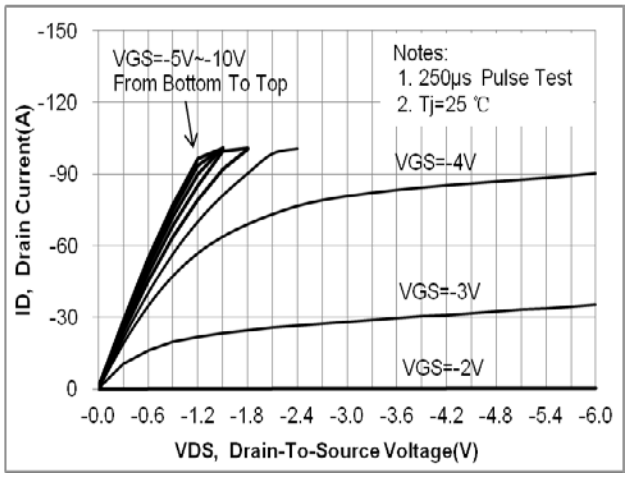


Fig. 2. On-resistance variation vs. drain current and gate voltage

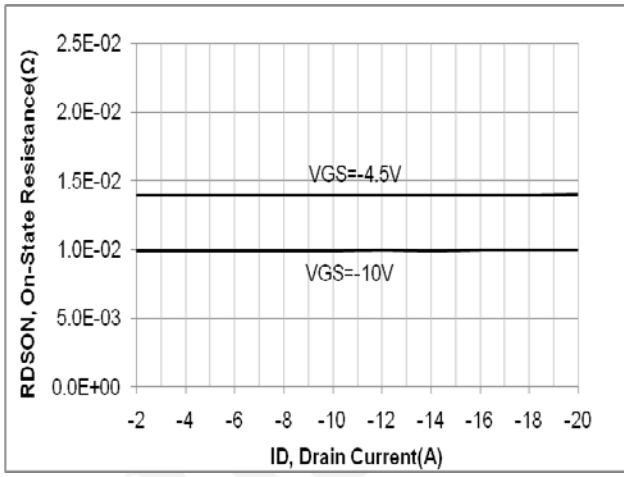


Fig. 3. Gate charge characteristics

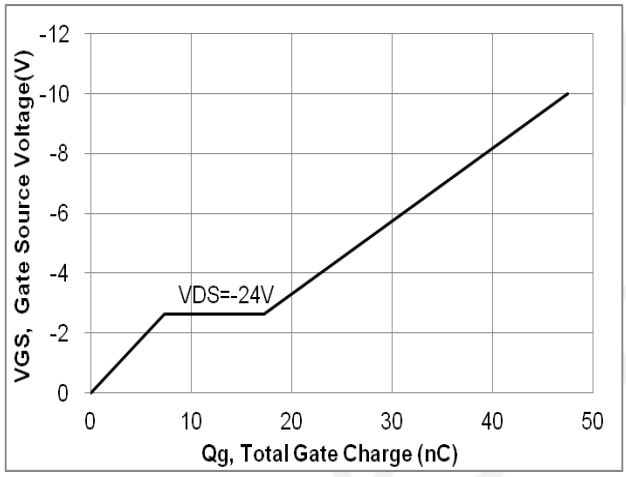


Fig. 4. On state current vs. diode forward voltage

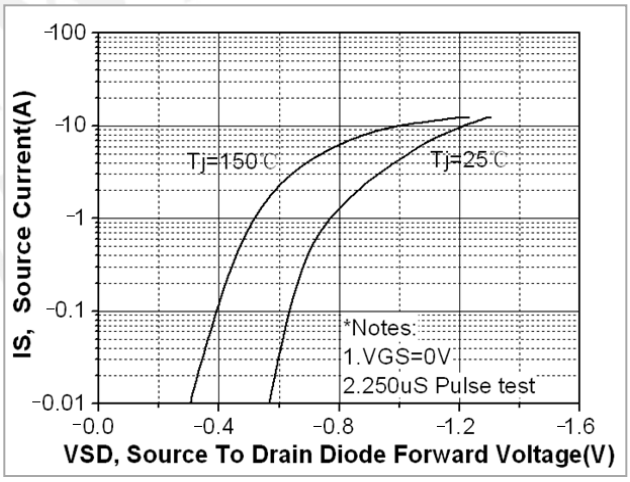


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

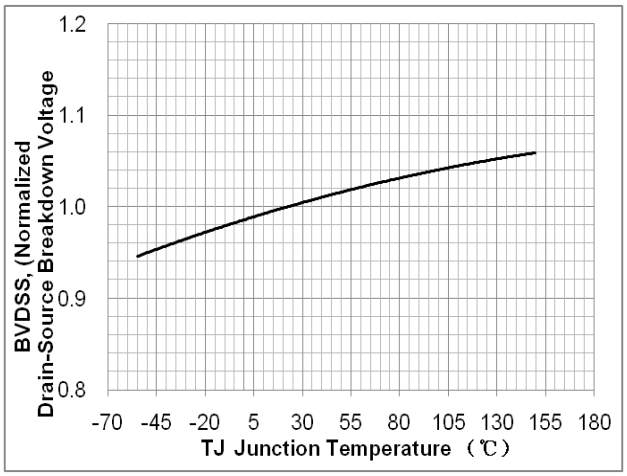


Fig. 6. On resistance variation vs. junction temperature

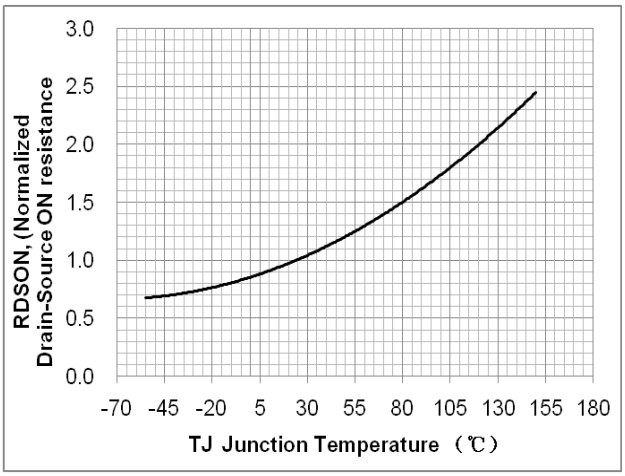


Fig. 7. Capacitance Characteristics

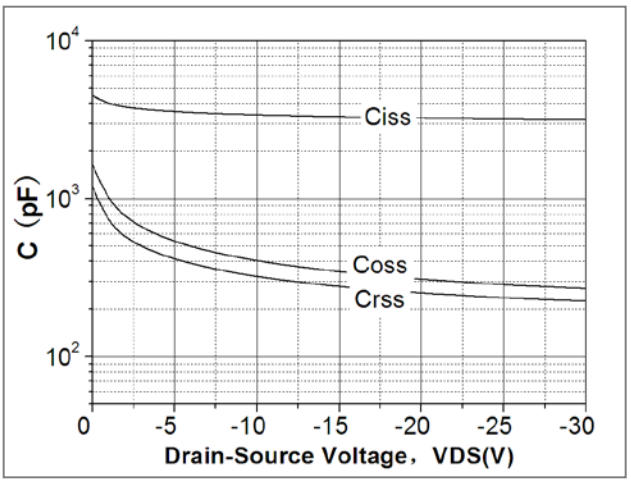


Fig. 8. Maximum safe operating area（SOP8）

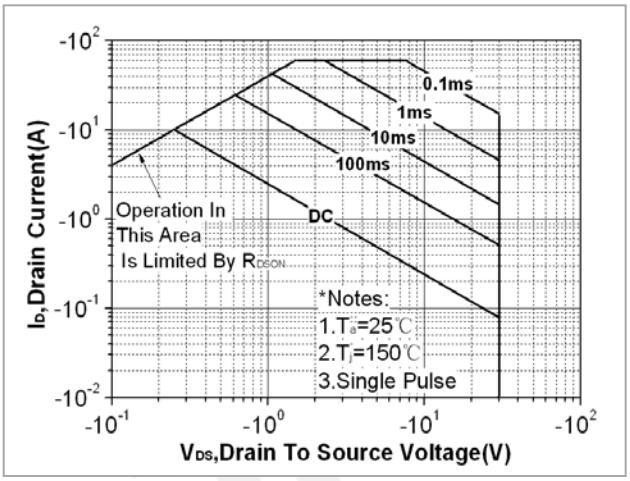


Fig. 9. Maximum safe operating area（DFN3*3）

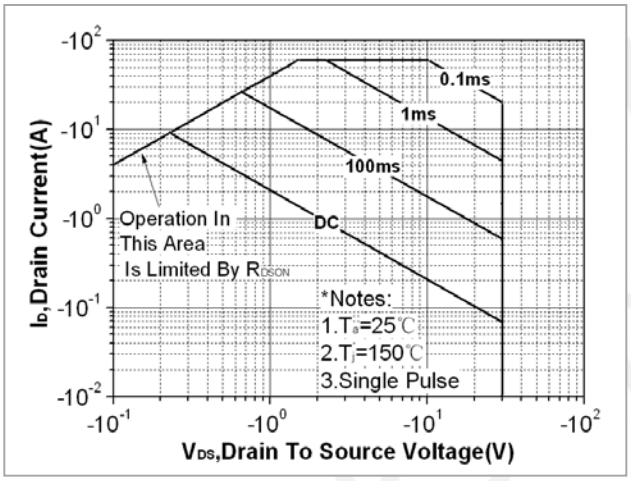


Fig. 10. Transient thermal response curve（SOP8）

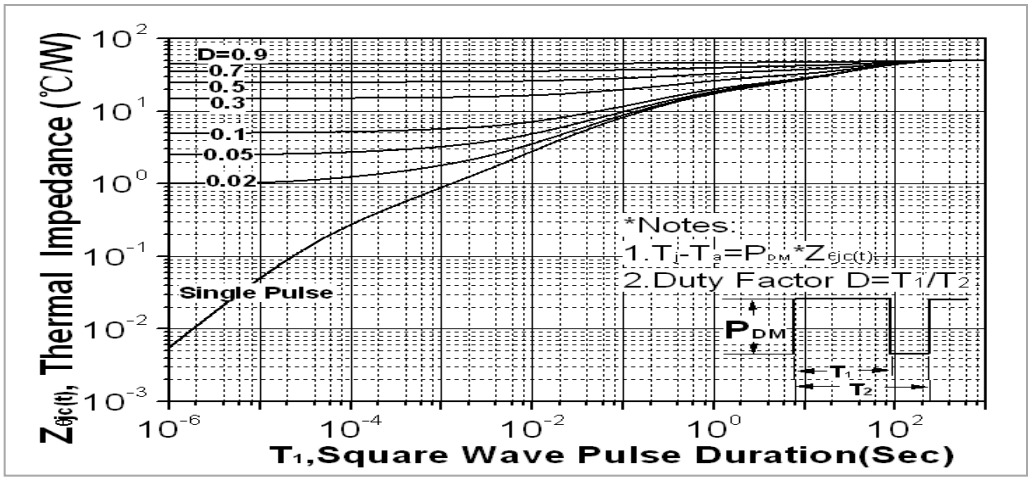


Fig. 11. Transient thermal response curve（DFN3*3）

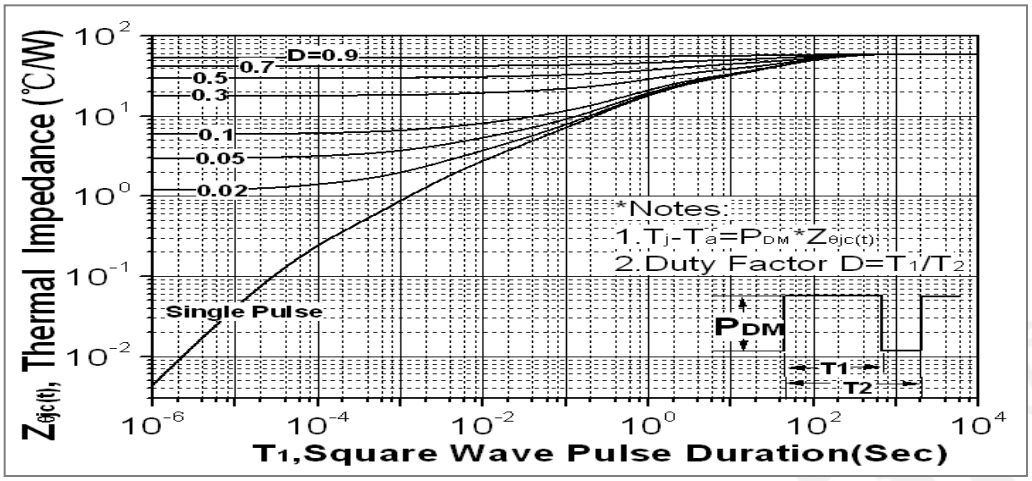


Fig. 12. Gate charge test circuit & waveform

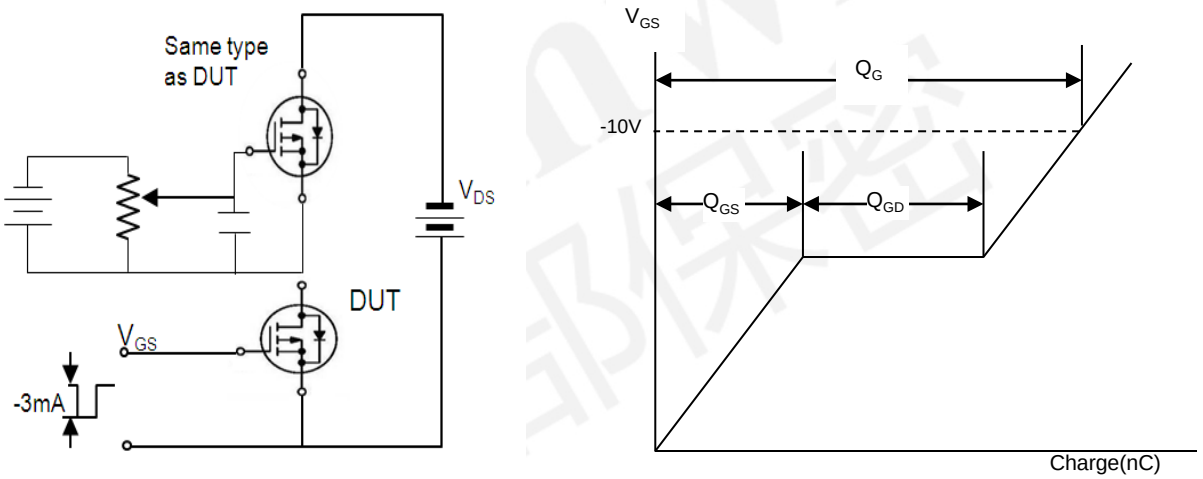


Fig. 13. Switching time test circuit & waveform

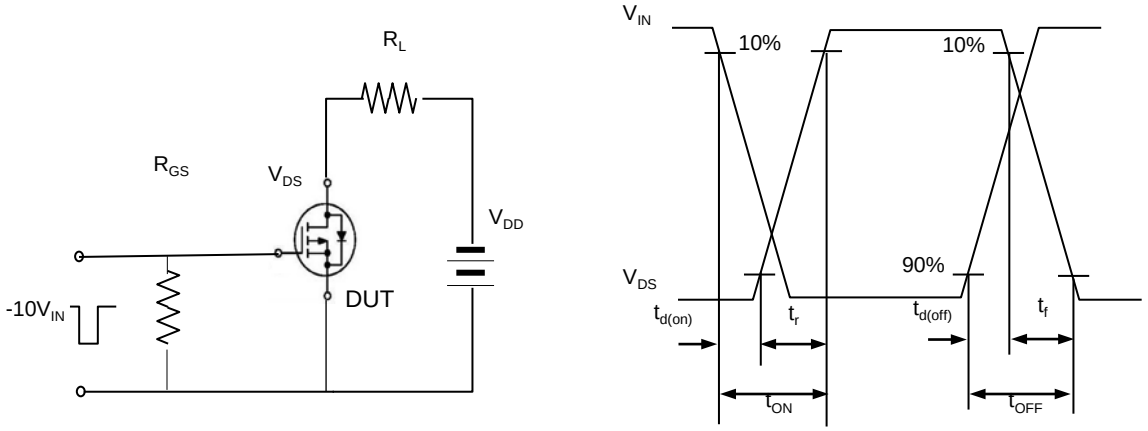


Fig. 14. Unclamped Inductive switching test circuit & waveform

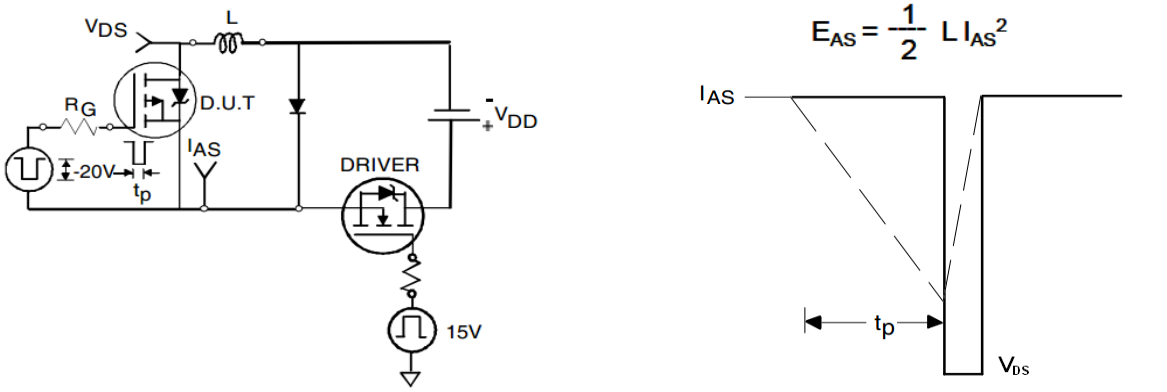
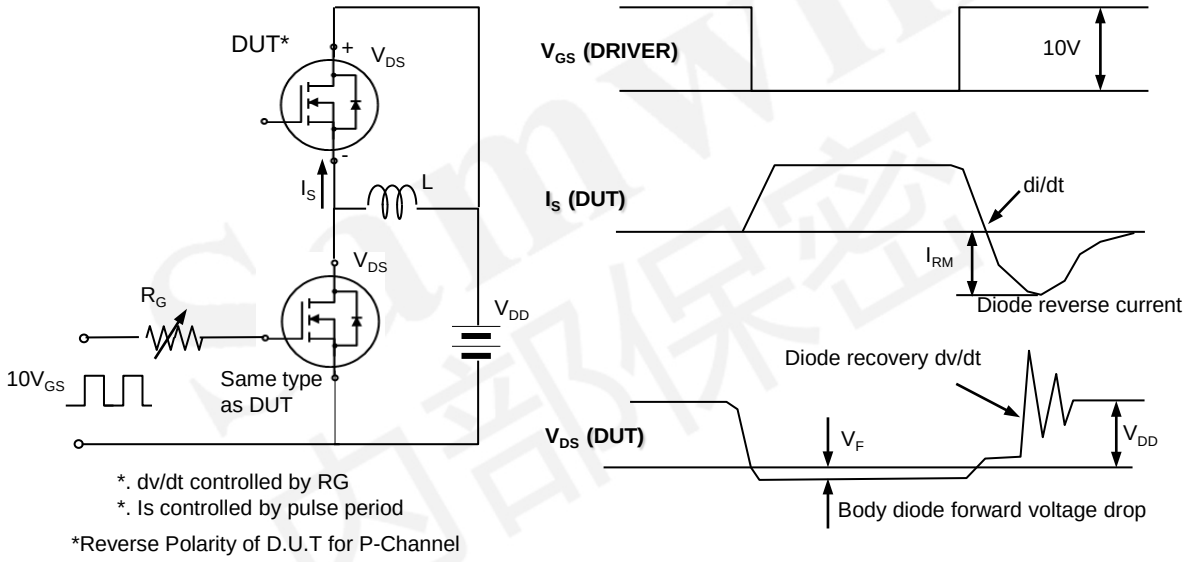


Fig. 15. Peak diode recovery dv/dt test circuit & waveform



*. dv/dt controlled by RG
*. Is controlled by pulse period

*Reverse Polarity of D.U.T for P-Channel

DISCLAIMER

* All the data & curve in this document was tested in XI'AN SEMIPOWER TESTING & APPLICATION CENTER.
* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.
* Qualification standards can also be found on the Web site (**http://www.semipower.com.cn**)
* Suggestions for improvement are appreciated, Please send your suggestions to **samwin@samwinsemi.com**