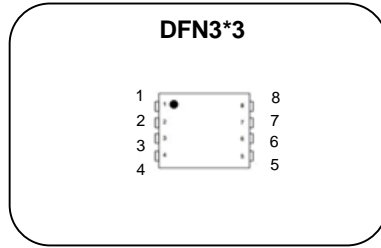


### N-channel Enhanced mode DFN3\*3 MOSFET

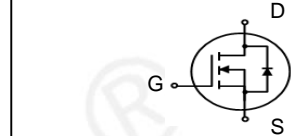
#### Features

- High ruggedness
- Low  $R_{DS(ON)}$  (Typ 4.6m $\Omega$ )@ $V_{GS}=2.5V$   
Low  $R_{DS(ON)}$  (Typ 3.7m $\Omega$ )@ $V_{GS}=4.5V$   
Low  $R_{DS(ON)}$  (Typ 3.3m $\Omega$ )@ $V_{GS}=10V$
- Low Gate Charge (Typ 50nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: DC-DC Converter, Motor Control Synchronous Rectification



Gate:4 Drain:5,6,7,8 Source:1,2,3

$BV_{DSS}$	: 20V
$I_D$	: 20A
$R_{DS(ON)}$	: 4.6m $\Omega$ @ $V_{GS}=2.5V$ 3.7m $\Omega$ @ $V_{GS}=4.5V$ 3.3m $\Omega$ @ $V_{GS}=10V$



#### General Description

This power MOSFET is produced with advanced technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

#### Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW H 045R02VT	SW045R02V	DFN3*3	REEL

#### Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain to source voltage	20	V
$I_D$	Continuous drain current (@ $T_C=25^\circ C$ )	20*	A
	Continuous drain current (@ $T_C=100^\circ C$ )	18*	A
$I_{DM}$	Drain current pulsed (note 1)	80	A
$I_{DSM}$	Continuous drain current (@ $T_a=25^\circ C$ )	20	A
	Continuous drain current (@ $T_a=70^\circ C$ )	18	A
$V_{GS}$	Gate to source voltage	$\pm 12$	V
$E_{AS}$	Single pulsed avalanche energy (note 2)	122	mJ
$E_{AR}$	Repetitive avalanche energy (note 1)	9	mJ
dv/dt	Peak diode recovery dv/dt (note 3)	5	V/ns
$P_D$	Total power dissipation (@ $T_C=25^\circ C$ )	30.5	W
	Total power dissipation (@ $T_a=25^\circ C$ )	2.6	W
$T_{STG}, T_J$	Operating junction temperature & storage temperature	-55 ~ + 150	$^\circ C$

\*. Drain current is limited by junction temperature.

#### Thermal characteristics

Symbol	Parameter	Value	Unit
$R_{thjc}$	Thermal resistance, Junction to case	4.1	$^\circ C/W$
$R_{thja}$	Thermal resistance, Junction to ambient	48	$^\circ C/W$

Note:  $R_{thja}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{thjc}$  is guaranteed by design while  $R_{thca}$  is determined by the user's board design.



DFN3\*3  $R_{thja}$  : 48 $^\circ C/W$  on a 1 in<sup>2</sup> pad of 2oz copper.

## Electrical characteristic ( T<sub>J</sub> = 25°C unless otherwise specified )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Off characteristics</b>						
BV <sub>DSS</sub>	Drain to source breakdown voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown voltage temperature coefficient	I <sub>D</sub> =250uA, referenced to 25°C		0.02		V/°C
I <sub>DSS</sub>	Drain to source leakage current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	uA
		V <sub>DS</sub> =16V, T <sub>J</sub> =125°C			50	uA
I <sub>GSS</sub>	Gate to source leakage current, forward	V <sub>GS</sub> =12V, V <sub>DS</sub> =0V			100	nA
	Gate to source leakage current, reverse	V <sub>GS</sub> =-12V, V <sub>DS</sub> =0V			-100	nA
<b>On characteristics</b>						
V <sub>GS(TH)</sub>	Gate threshold voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	0.45		1.3	V
R <sub>DS(ON)</sub>	Drain to source on state resistance	V <sub>GS</sub> =2.5V, I <sub>D</sub> =10A, T <sub>J</sub> =25°C		4.6	5.8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A, T <sub>J</sub> =25°C		3.7	4.6	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =10A, T <sub>J</sub> =25°C		3.3	4.1	mΩ
		V <sub>GS</sub> =10V, I <sub>D</sub> =10A, T <sub>J</sub> =125°C		4.6		mΩ
G <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =10A		56		S
<b>Dynamic characteristics</b>						
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =10V, f=1MHz		3480		pF
C <sub>oss</sub>	Output capacitance			545		
C <sub>rss</sub>	Reverse transfer capacitance			509		
t <sub>d(on)</sub>	Turn on delay time	V <sub>DS</sub> =10V, I <sub>D</sub> =20A, R <sub>G</sub> =4.7Ω, V <sub>GS</sub> =10V (note 4,5)		5		ns
t <sub>r</sub>	Rising time			36		
t <sub>d(off)</sub>	Turn off delay time			104		
t <sub>f</sub>	Fall time			32		
Q <sub>g</sub>	Total gate charge	V <sub>DS</sub> =16V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A, I <sub>G</sub> =3mA (note 4,5)		50		nC
Q <sub>gs</sub>	Gate-source charge			5.6		
Q <sub>gd</sub>	Gate-drain charge			19		
R <sub>g</sub>	Gate resistance		V <sub>DS</sub> =0V, Scan F mode		1.0	

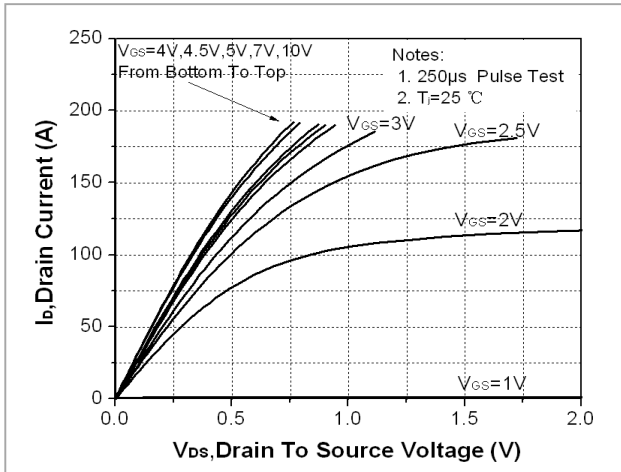
## Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			20	A
I <sub>SM</sub>	Pulsed source current				80	A
V <sub>SD</sub>	Diode forward voltage drop.	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.4	V
t <sub>rr</sub>	Reverse recovery time	I <sub>S</sub> =20A, V <sub>GS</sub> =0V, di <sub>f</sub> /dt=100A/us		19		ns
Q <sub>rr</sub>	Reverse recovery charge				3.3	nC

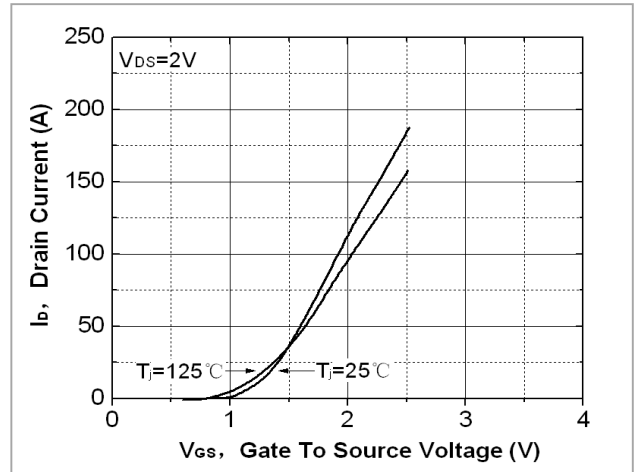
### ※. Notes

1. Repeattive rating : pulse width limited by junction temperature.
2. L =0.27mH, I<sub>AS</sub> =30A, V<sub>DD</sub>=15V, R<sub>G</sub>=25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 20A, di/dt = 100A/us, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

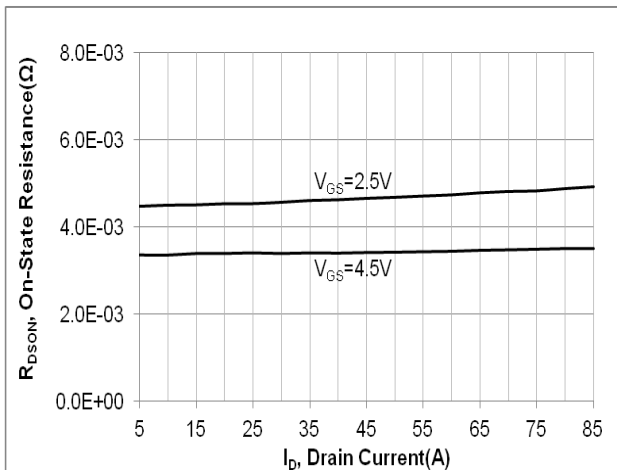
**Fig. 1. On-state characteristics**



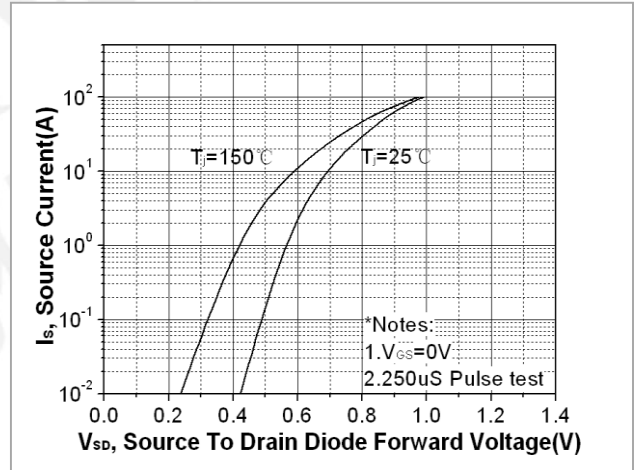
**Fig. 2. Transfer characteristics**



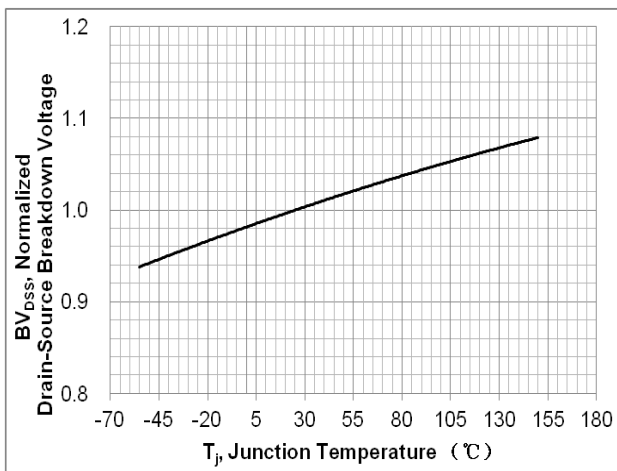
**Fig. 3. On-resistance variation vs. drain current and gate voltage**



**Fig. 4. On-state current vs. diode forward voltage**



**Fig 5. Breakdown voltage variation vs. junction temperature**



**Fig. 6. On-resistance variation vs. junction temperature**

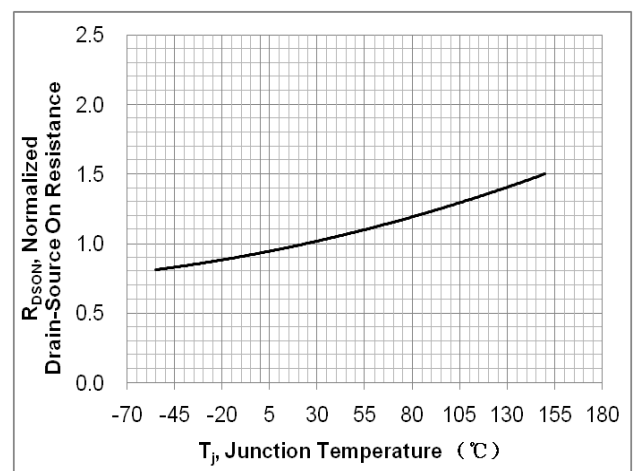


Fig. 7. Gate charge characteristics

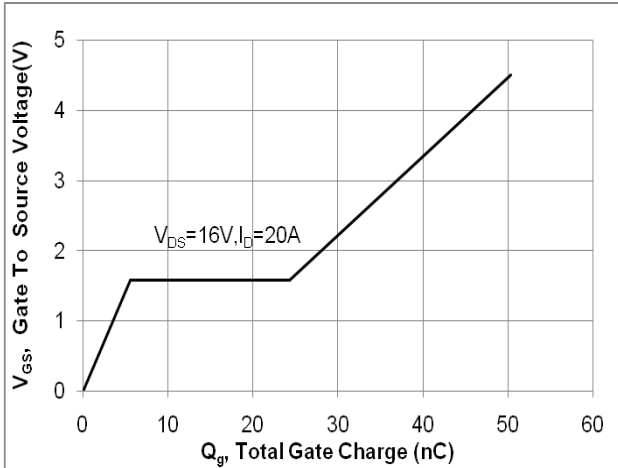


Fig. 8. Capacitance Characteristics

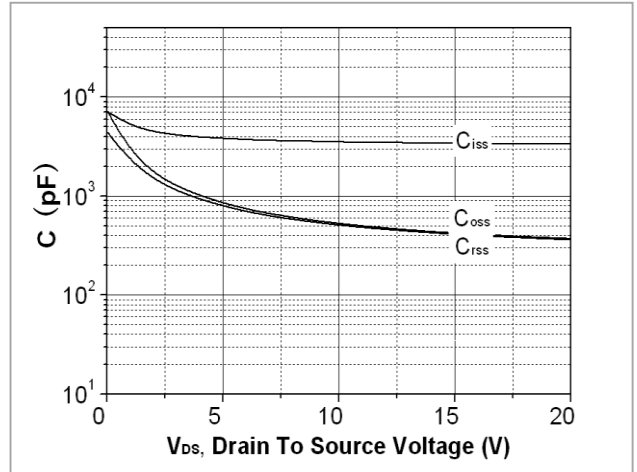


Fig. 9. Maximum safe operating area

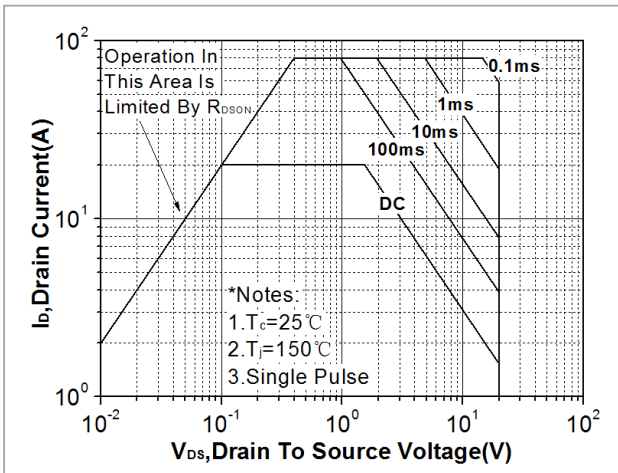


Fig. 10. Maximum drain current vs. case temperature

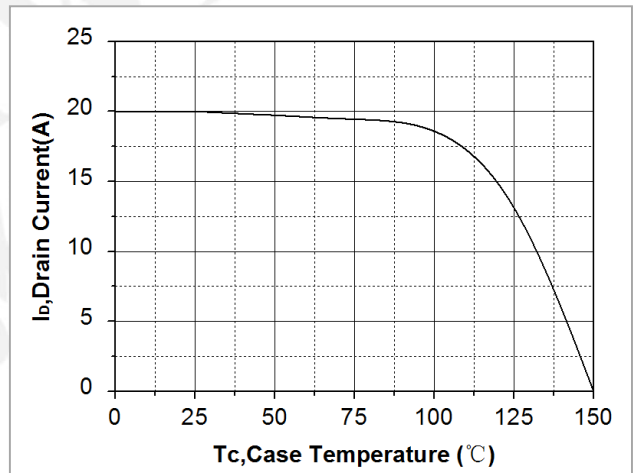
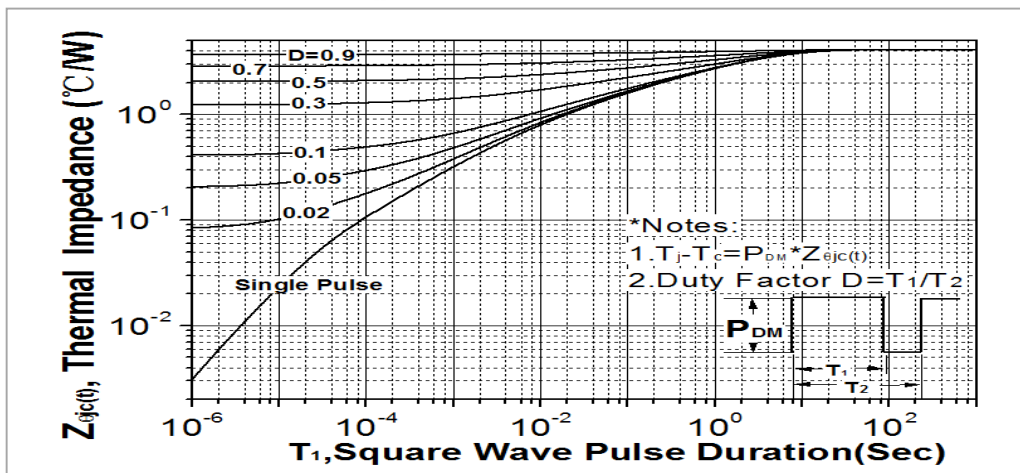
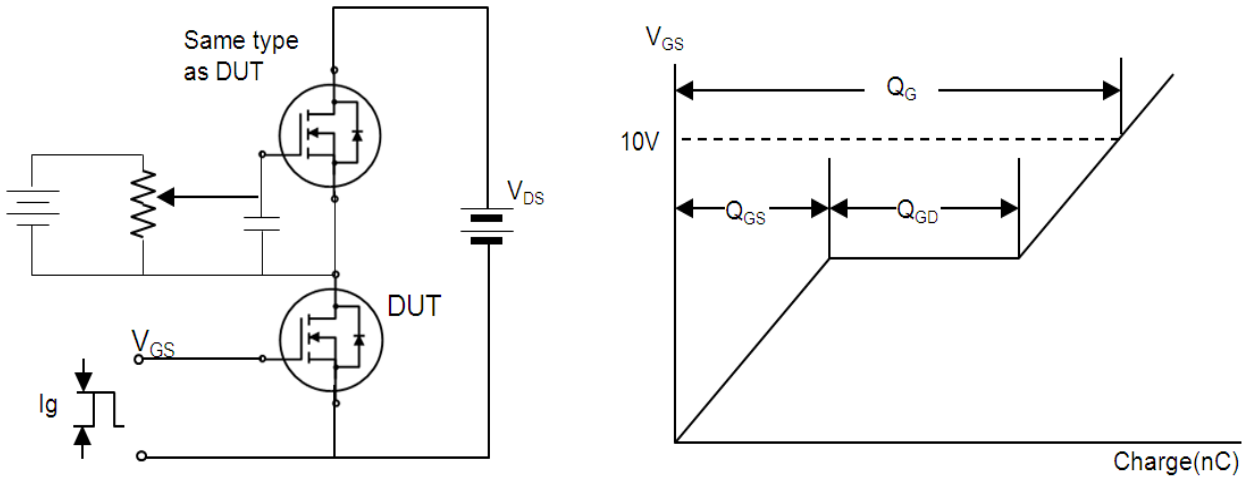


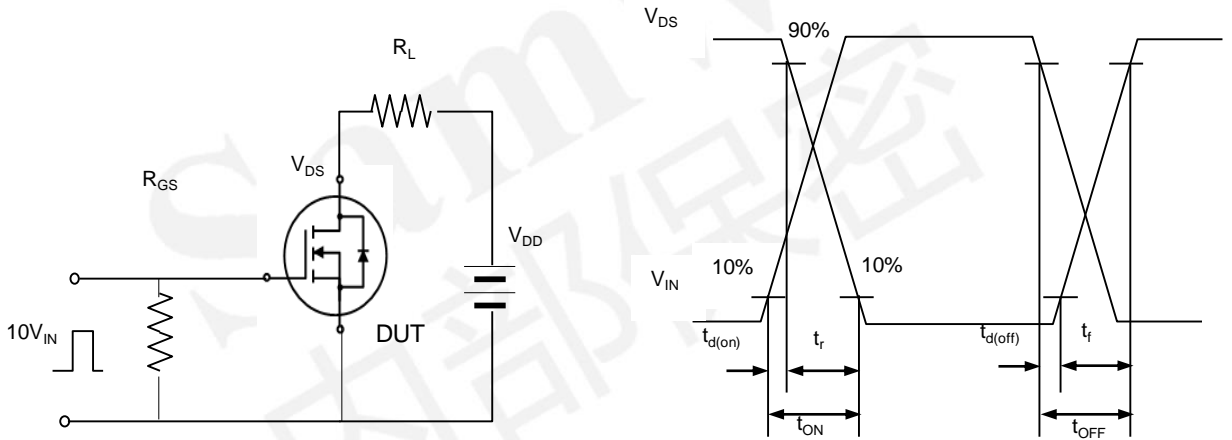
Fig. 11. Transient thermal response curve



**Fig. 12. Gate charge test circuit & waveform**



**Fig. 13. Switching time test circuit & waveform**



**Fig. 14. Unclamped Inductive switching test circuit & waveform**

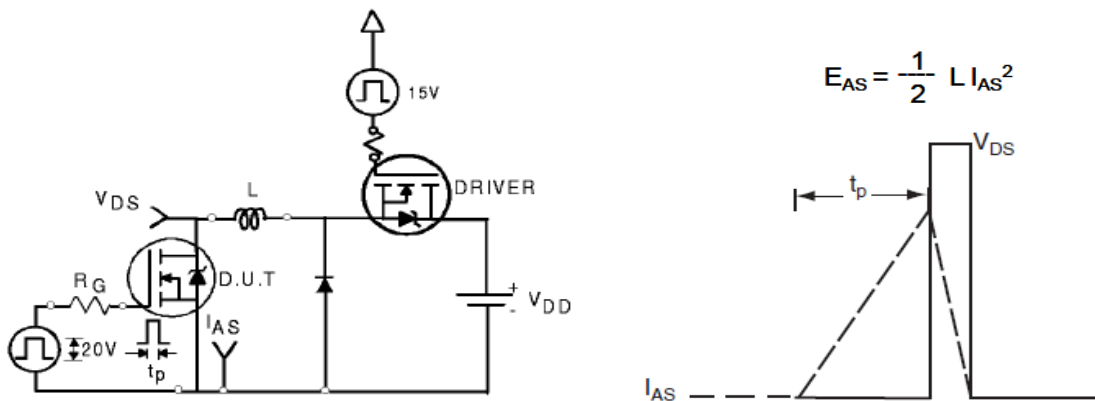
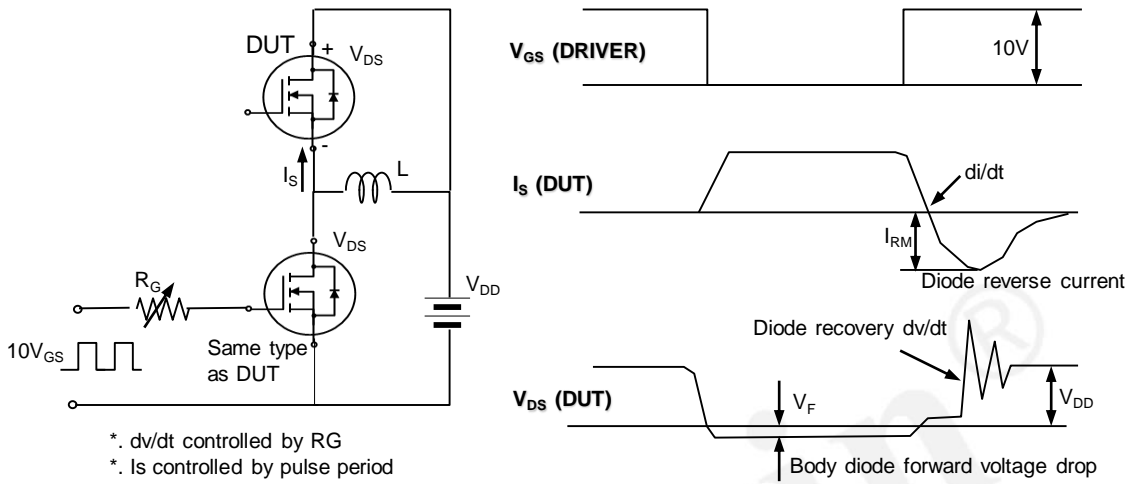


Fig. 15. Peak diode recovery dv/dt test circuit & waveform



### DISCLAIMER

\* All the data & curve in this document was tested in XI'AN SEMIPOWER TESTING & APPLICATION CENTER.

\* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.

\* Qualification standards can also be found on the Web site (<http://www.semipower.com.cn>) 

\* Suggestions for improvement are appreciated, Please send your suggestions to [samwin@samwinsemi.com](mailto:samwin@samwinsemi.com)