maximum semiconductor

MS3205STRLPBF

100A, 55V, 0.008 Ohm, N-Channel, Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

NOTE: Calculated continuous current based on maximum allowable junction temperature. Package limited to 75A continuous, see Figure 9.

Ordering Information

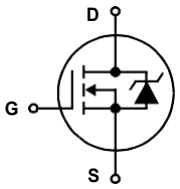
PART NUMBER	PACKAGE	BRAND
MS3205	TO-220AB	MS3205TR
MS3205S	TO-263AB	MS3205STRLPBF

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HRF3205ST.

Features

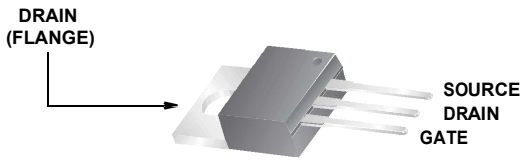
- 100A, 55V (See Note)
- Low On-Resistance, $r_{DS(ON)} = 0.008\Omega$
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

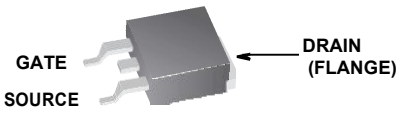


Packaging

TO-220AB



TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Othewise Specified

Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	±20V	V
Drain Current			
Continuous	I_D	100	A
Pulsed Drain Current (Note 2)	I_{DM}	390	A
Pulsed Avalanche Rating	E_{AS}	Figure 10	
Power Dissipation	P_D	175	W
Derate Above 25^oC		1.17	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

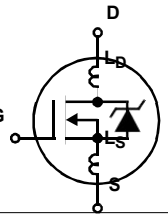
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

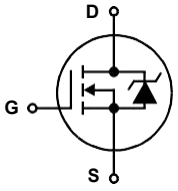
1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		55	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55V, V_{GS} = 0V		-	-	25	μA
		V_{DS} = 44V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25^oC, I_D = 250μA		-	0.057	-	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 59A, V_{GS} = 10V (Figure 4)		-	0.0065	0.008	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 28V, $I_D \cong$ 59A, R_L = 0.47Ω, V_{GS} = 10V, R_{GS} = 2.5Ω		-	14	-	ns
Rise Time	t_r			-	100	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	43	-	ns
Fall Time	t_f			-	70	-	ns
Total Gate Charge	Q_g	V_{DD} = 44V, $I_D \cong$ 59A, V_{GS} = 10V, $I_{g(REF)}$ = 3mA (Figure 6)		-	-	170	nC
Gate to Source Charge	Q_{gs}			-	-	32	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	-	74	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 5)		-	4000	-	pF
Output Capacitance	C_{OSS}			-	1300	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	480	-	pF
Internal Source Inductance	L_S	Measured From the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances	-	7.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die					
Internal Drain Inductance	L_D	Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	4.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.85	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220		-	-	62	$^oC/W$
		TO-263 (PCB Mount, Steady State)		-	-	40	$^oC/W$



Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	MOSFET Symbol Showing The Integral Reverse P-N Junction Diode 	-	-	100 (Note 1	A
Pulsed Source to Drain Current (Note 2)	I_{SDM}		-	-	390	A
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 59A (Note 4)	-	-	1.3	V
Reverse Recovery Time	t_{rr}	I_{SD} = 59A, dI_{SD}/dt = 100A/μs (Note 4)	-	110	170	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 59A, dI_{SD}/dt = 100A/μs (Note 4)	-	450	680	nC

NOTE:

2. Repetitive rating; pulse width limited by maximum junction temperature (See Figure 11)

Typical Performance Curves

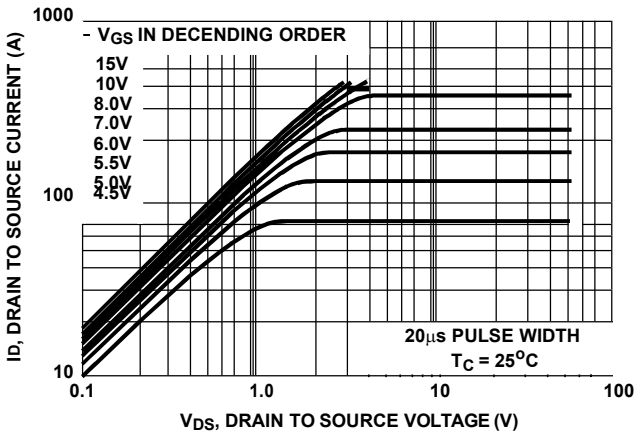


FIGURE 1. OUTPUT CHARACTERISTICS

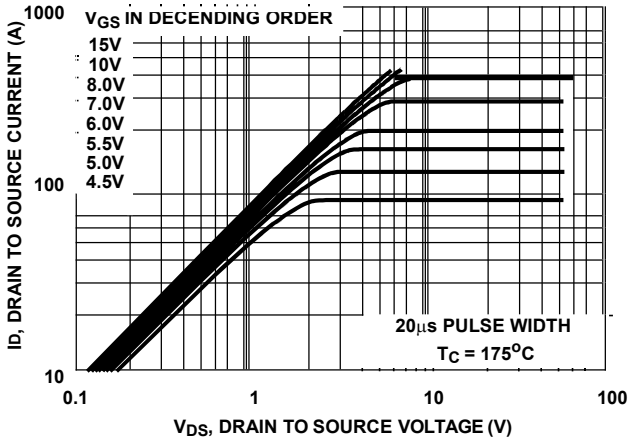


FIGURE 2. OUTPUT CHARACTERISTICS

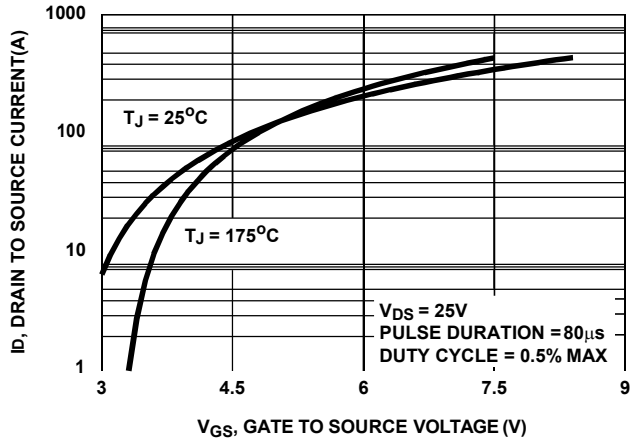


FIGURE 3. TRANSFER CHARACTERISTICS

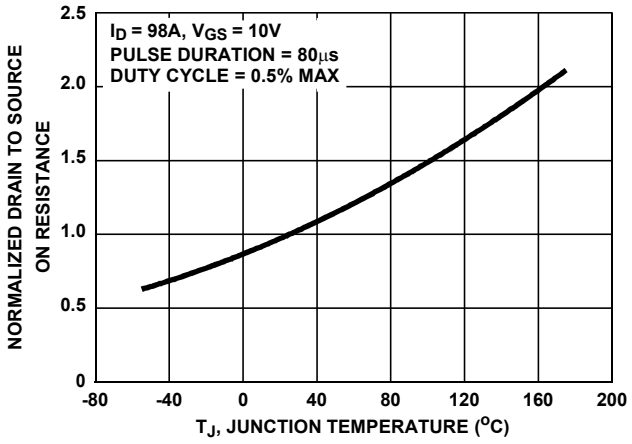


FIGURE 4. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

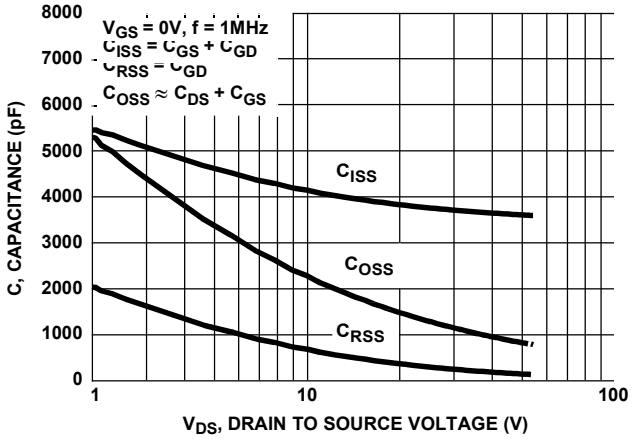


FIGURE 5. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

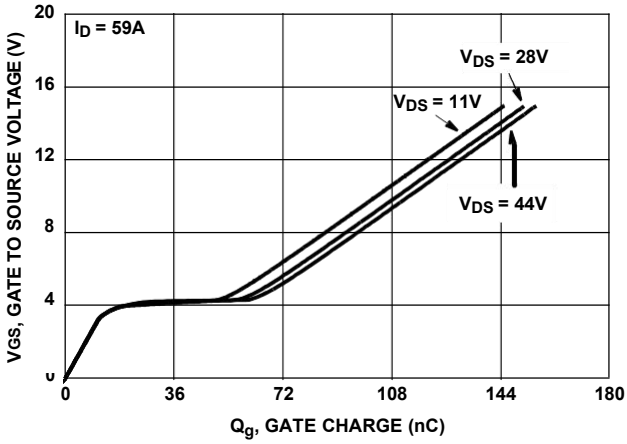


FIGURE 6. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

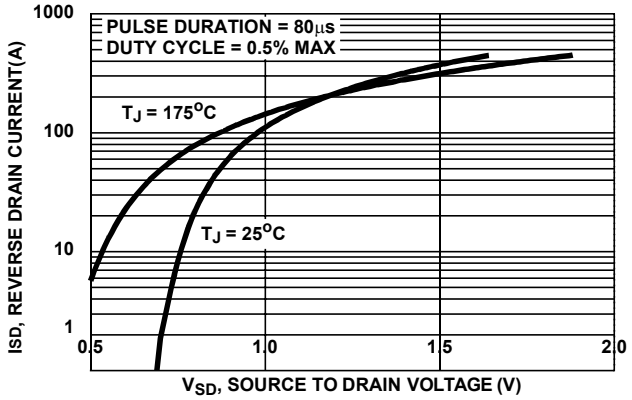


FIGURE 7. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

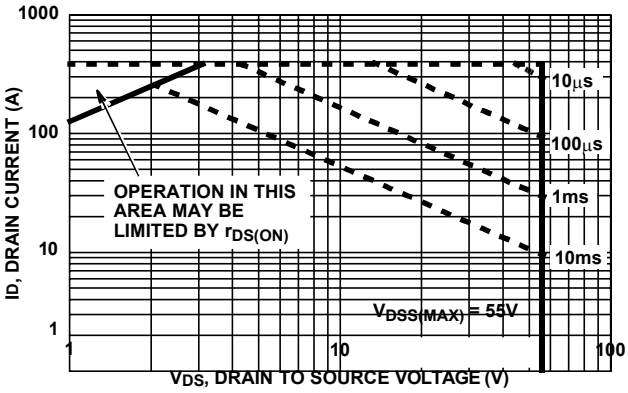


FIGURE 8. FORWARD BIAS SAFE OPERATING AREA

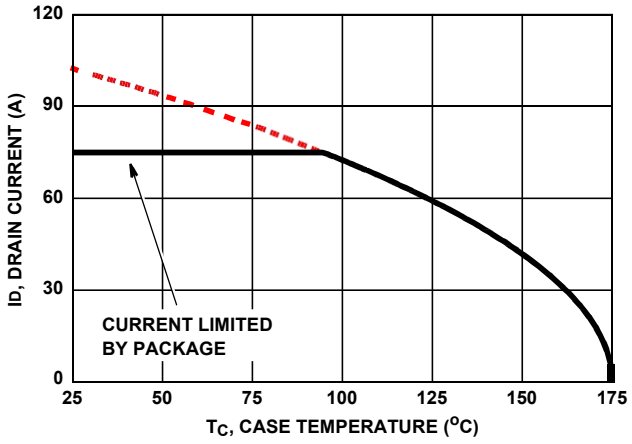


FIGURE 9. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

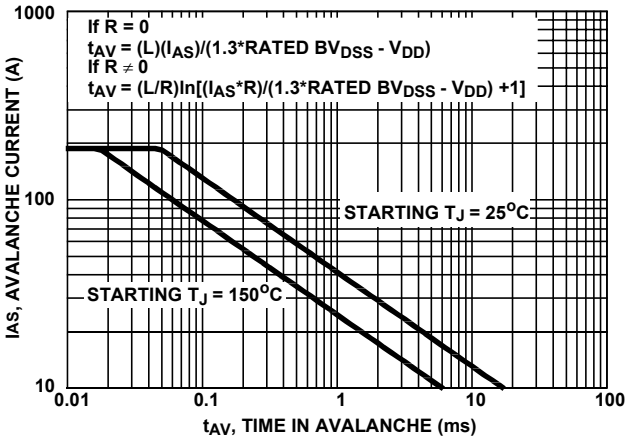


FIGURE 10. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

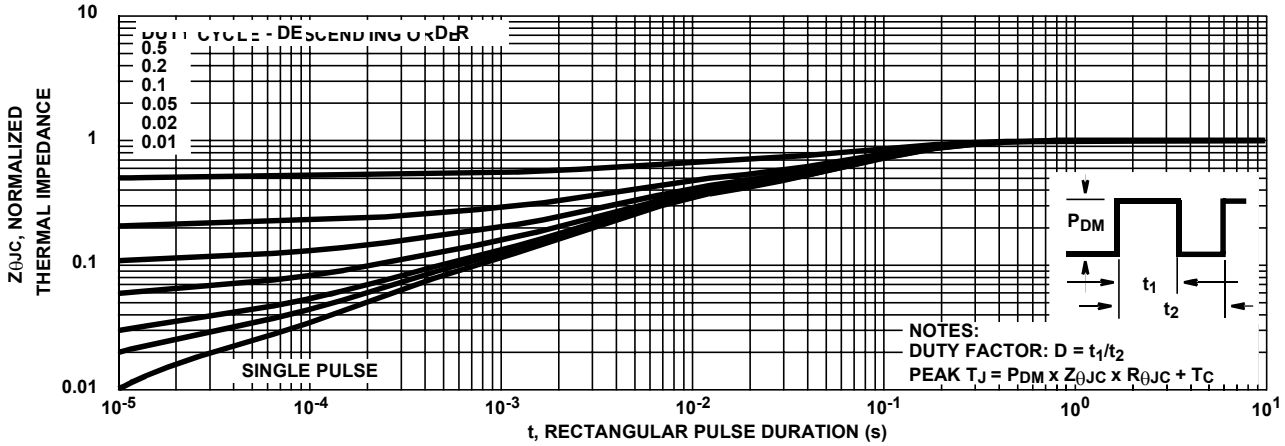


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

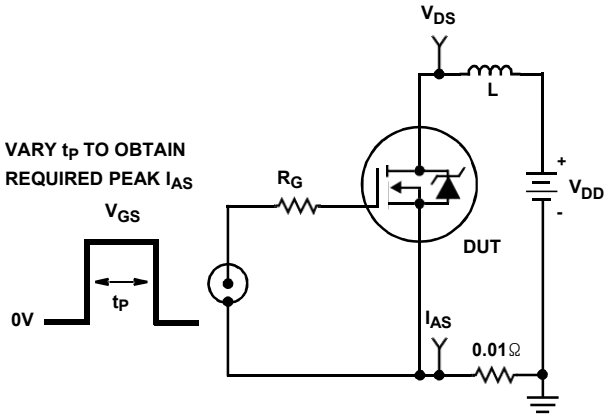


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

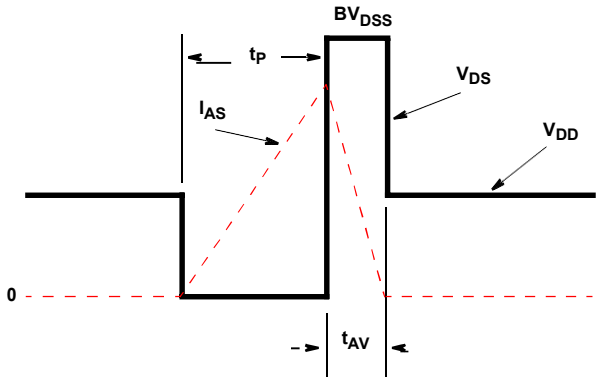


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

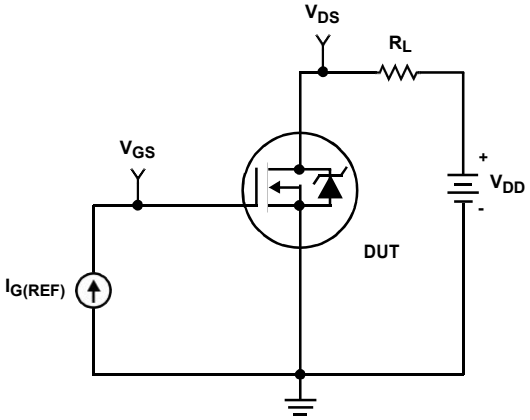


FIGURE 14. GATE CHARGE TEST CIRCUIT

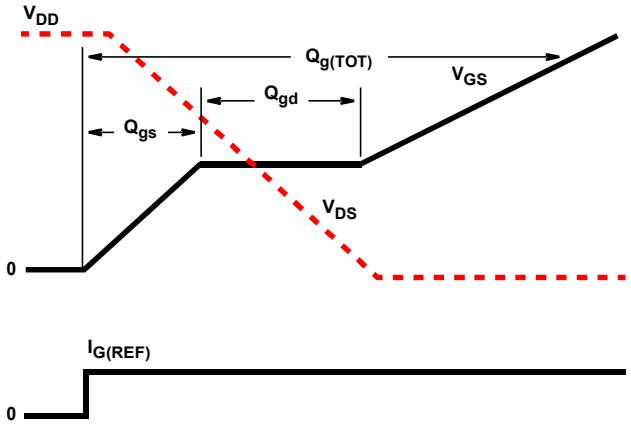


FIGURE 15. GATE CHARGE WAVEFORM

Test Circuits and Waveforms (Continued)

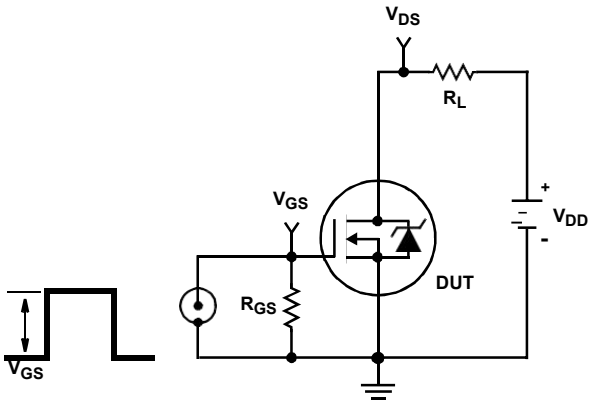


FIGURE 16. SWITCHING TIME TEST CIRCUIT

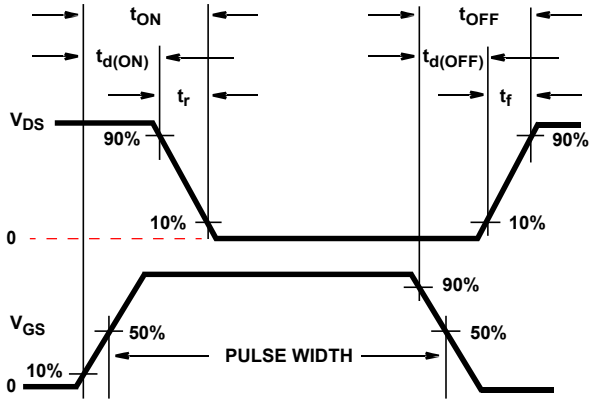


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS