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RTL8316E
LAYER 2 16-PORT 10/100M SINGLE-CHIP SWITCH CONTROLLER

RTL8324E
LAYER 2 24-PORT 10/100M SWITCH CONTROLLER WITH ONE XSMII

DATASHEET
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8316E/RTL8324E chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2013/04/24	First release.

Table of Contents

1. GENERAL DESCRIPTION 1

2. FEATURES 2

3. BLOCK DIAGRAMS 3

3.1. RTL8316E BLOCK DIAGRAM 3
3.2. RTL8324E BLOCK DIAGRAM 4

4. SYSTEM APPLICATIONS 5

4.1. RTL8316E: 16*10/100M SWITCH 5
4.2. RTL8324E: 24*10/100M SWITCH 6

5. PIN ASSIGNMENTS AND DESCRIPTIONS (RTL8316E) 7

5.1. PIN ASSIGNMENTS FIGURE (RTL8316E) 7
5.2. PACKAGE IDENTIFICATION 7
5.3. PIN ASSIGNMENTS TABLE DEFINITIONS (RTL8316E) 8
5.4. PIN ASSIGNMENTS TABLE (RTL8316E) 8
5.5. PIN DESCRIPTIONS (RTL8316E) 10
5.5.1. Media Connection Pins (RTL8316E) 10
5.5.2. Serial LED/LED IC Interface Pins (RTL8316E) 11
5.5.3. SCAN LED Interface Pins (RTL8316E) 11
5.5.4. Miscellaneous Interface Pins (RTL8316E) 11
5.5.5. Configuration Strapping Pins (RTL8316E) 12
5.5.6. Power and GND Pins (RTL8316E) 13

6. PIN ASSIGNMENTS AND DESCRIPTIONS (RTL8324E) 14

6.1. PIN ASSIGNMENTS FIGURE (RTL8324E) 14
6.2. PACKAGE IDENTIFICATION 14
6.3. PIN ASSIGNMENTS TABLE DEFINITIONS (RTL8324E) 15
6.4. PIN ASSIGNMENTS TABLE (RTL8324E) 15
6.5. PIN DESCRIPTIONS (RTL8324E) 17
6.5.1. Media Connection Pins (RTL8324E) 17
6.5.2. Serial LED Interface Pins (RTL8324E) 18
6.5.3. Miscellaneous Interface Pins (RTL8324E) 18
6.5.4. Configuration Strapping Pins (RTL8324E) 18
6.5.5. XSMII Interface Pins (RTL8324E) 19
6.5.6. Power and GND Pins (RTL8324E) 19

7. PHYSICAL LAYER FUNCTIONAL OVERVIEW 20

7.1. MDI INTERFACE 20
7.2. 100BASE-TX TRANSMIT FUNCTION 20
7.3. 100BASE-TX RECEIVE FUNCTION 20
7.4. 10BASE-T TRANSMIT FUNCTION 20
7.5. 10BASE-T RECEIVE FUNCTION 20
7.6. AUTO-NEGOTIATION FOR UTP 21
7.7. CROSSOVER DETECTION AND AUTO CORRECTION 21
7.8. POLARITY CORRECTION 21

8. SWITCH FUNCTION DESCRIPTION 22

8.1. HARDWARE RESET AND SOFTWARE RESET 22
8.1.1. Hardware Reset 22
8.1.2. Software Reset 22

8.2. Layer 2 Learning and Forwarding 22
8.2.1. Learning *22*
8.2.2. Forwarding *22*
8.2.3. Address Table Aging *22*
8.3. Reserved Multicast Address Handling 23
8.4. IEEE 802.3x Flow Control 23
8.5. Half Duplex Backpressure 24
8.5.1. Collision-Based Backpressure (Jam Mode) *24*
8.5.2. Carrier-Based Backpressure (Defer Mode) *25*
8.6. IEEE 802.3az Energy Efficient Ethernet (EEE) 25
8.7. Green Ethernet 25
8.7.1. Link Down Power Saving *25*
8.8. IEEE 802.1p and IEEE 802.1Q (VLAN) 25
8.9. Loop Detection 26
8.10. Layer 2 Traffic Suppression (Storm Control) 26
8.11. IEEE 802.3ad Link Aggregation Protocol 26
8.12. Bandwidth Control 26
8.12.1. Input Bandwidth Control *26*
8.12.2. Output Bandwidth Control *26*
8.13. Quality of Service (QoS) 27
8.13.1. Priority Arbitration *27*
8.13.2. Port-Based Priority Assignment *27*
8.13.3. IEEE 802.1Q-Based Priority Assignment *27*
8.13.4. DSCP-Based Priority Assignment *27*
8.13.5. Internal Priority to Queue ID Table *27*
8.14. Packet Scheduling (WRR and WFQ) 28
8.15. Egress Packet Remarking 28
8.16. Ingress and Egress Port Mirror 28
8.17. Management Information Base (MIB) 28
8.18. Realtek Cable Tester 29
8.19. EEPROM Configuration 29

9. INTERFACE DESCRIPTIONS 30

9.1. XSMII Interconnection 30
9.2. I2C-Like LED 30
9.3. Serial LED Connection 31
9.4. Scan LED for RTL8316E (Not Supported in the RTL8324E) 32
9.5. I2C Master for EEPROM 33
9.6. Serial CPU Interface 33

10. ELECTRICAL AC/DC CHARACTERISTICS 34

10.1. Absolute Maximum Ratings 34
10.2. Operating Range 34
10.3. DC Characteristics 34
10.4. AC Characteristics 35
10.4.1. XSMII Transmitter Signal Electrical Characteristics *35*
10.4.2. XSMII Receiver Signal Electrical Characteristics *35*
10.4.3. Serial LED Signal Timing *35*
10.4.4. Scan LED Mode Signal Timing (RTL8316E) *36*
10.4.5. I2C Master for EEPROM Timing *36*
10.4.6. SCK/SDA Power on Timing *37*
10.4.7. EEPROM Auto-Load Timing *37*
10.4.8. I2C Master Mode Timing Characteristics *37*
10.4.9. Serial CPU Interface Timing *38*
10.4.10. Serial CPU Interface Timing Characteristics *38*

10.5. SMI TIMING CHARACTERISTICS (RTL8324E ONLY) 38
11. MECHANICAL DIMENSIONS 39
12. ORDERING INFORMATION 40

List of Tables

TABLE 1. PIN ASSIGNMENTS TABLE (RTL8316E) 8
TABLE 2. MEDIA CONNECTION PINS (RTL8316E) 10
TABLE 3. SERIAL LED/LED IC INTERFACE PINS (RTL8316E) 11
TABLE 4. SCAN LED INTERFACE PINS (RTL8316E) 11
TABLE 5. MISCELLANEOUS INTERFACE PINS (RTL8316E) 11
TABLE 6. CONFIGURATION STRAPPING PINS (RTL8316E) 12
TABLE 7. POWER AND GND PINS (RTL8316E) 13
TABLE 8. RTL8324E PIN ASSIGNMENTS TABLE (RTL8324E) 15
TABLE 9. MEDIA CONNECTION PINS (RTL8324E) 17
TABLE 10. LED INTERFACE PINS (RTL8324E) 18
TABLE 11. MISCELLANEOUS INTERFACE PINS (RTL8324E) 18
TABLE 12. CONFIGURATION STRAPPING PINS (RTL8324E) 18
TABLE 13. XSMII INTERFACE PINS (RTL8324E) 19
TABLE 14. POWER AND GND PINS (RTL8324E) 19
TABLE 15. RESERVED MULTICAST ADDRESS DEFAULT ACTIONS 23
TABLE 16. ABSOLUTE MAXIMUM RATINGS 34
TABLE 17. RECOMMENDED OPERATING RANGE 34
TABLE 18. DC CHARACTERISTICS 34
TABLE 19. XSMII TRANSMITTER SIGNAL ELECTRICAL CHARACTERISTICS 35
TABLE 20. XSMII RECEIVER SIGNAL ELECTRICAL CHARACTERISTICS 35
TABLE 21. I2C MASTER MODE TIMING CHARACTERISTICS 37
TABLE 22. SERIAL CPU INTERFACE TIMING CHARACTERISTICS 38
TABLE 23. SMI TIMING CHARACTERISTICS (RTL8324E ONLY) 38
TABLE 24. ORDERING INFORMATION 40

List of Figures

FIGURE 1. RTL8316E BLOCK DIAGRAM 3
FIGURE 2. RTL8324E BLOCK DIAGRAM 4
FIGURE 3. RTL8316E: 16*10/100M SWITCH 5
FIGURE 4. RTL8324E: 24*10/100M SWITCH 6
FIGURE 5. PIN ASSIGNMENTS (RTL8316E) 7
FIGURE 6. PIN ASSIGNMENTS (RTL8324E) 14
FIGURE 7. CONCEPTUAL EXAMPLE OF POLARITY CORRECTION 21
FIGURE 8. TX PAUSE FRAME FORMAT 23
FIGURE 9. FLOW CONTROL STATE MACHINE 24
FIGURE 10. COLLISION-BASED BACKPRESSURE SIGNAL TIMING 24
FIGURE 11. XSMII INTERCONNECTION 30
FIGURE 12. SERIAL LED CONNECTION 31
FIGURE 13. SCAN LED MODE CONNECTION 32
FIGURE 14. LARGE SIZE (32KB~512KB) EEPROM READ/WRITE TIMING 33
FIGURE 15. SMALL SIZE (4KB~8KB) EEPROM READ/WRITE TIMING 33
FIGURE 16. SERIAL CPU INTERFACE ACCESS DATA SEQUENCE 33
FIGURE 17. SERIAL LED SIGNAL TIMING 35
FIGURE 18. SCAN LED MODE SIGNAL TIMING (RTL8316E) 36
FIGURE 19. I2C MASTER MODE TIMING 36
FIGURE 20. SCK/SDA POWER ON TIMING 37
FIGURE 21. EEPROM AUTO-LOAD TIMING 37
FIGURE 22. SERIAL CPU INTERFACE TIMING 38

1. General Description

The RTL8316E and RTL8324E are Layer 2 16/24-port 10/100M switch controllers that integrate 16/24 MACs and 16 physical layer transceivers for 100Base-TX and 10Base-T operation.

The RTL8324E (only) supports one XSMII (Eight Serial Media Independent Interface), which can be connected to an Octal PHY RTL8208D to provide a convenient solution for a 24-port Fast Ethernet switch.

The RTL8316E/RTL8324E provides an 8K-entry L2 table with a 4-way hash algorithm for MAC address learning and searching. The RTL8316E/RTL8324E supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning) for flexible network topology architecture. The RTL8316E/RTL8324E has a 512-entry VLAN table and 16-entry VLAN CAM table for VLAN operation.

Per-port ingress/egress bandwidth control and per-port/per-queue egress bandwidth control are supported, with four physical queues in each port. The RTL8316E/RTL8324E provides three types of packet scheduling, including SP (Strict Priority), WRR (Weighted Round Robin) and WFQ (Weighted Fair Queuing).

A loop-detection function provides notification of network loops. The RTL8316E/RTL8324E also supports port mirror configuration to mirror ingress and egress traffic, and link aggregation to increase link bandwidth and redundancy.

2. Features

- Hardware Interface
  - RTL8316E: 16-port 10/100M high performance Ethernet switch controller, and 16 FE PHYs for 100Base-TX and 10Base-T
  - RTL8324E: 24-port 10/100M high performance Ethernet switch controller, and 16 FE PHYs for 100Base-TX and 10Base-T
  - RTL8324E (only) supports XSMII interface to connect with octal FE PHY
  - RTL8316E (only) supports SCAN LED
  - RTL8316E/RTL8324E Support serial LED interface
- MAC Function
  - Supports 2KB jumbo frames
  - 8K-entry L2 MAC table with 4-way hashing algorithm
  - Supports source MAC blocking and Destination MAC blocking
  - Supports Reserved Multicast Addresses processing
  - Supports MAC Address learning constraints on each port
- VLAN Function
  - Supports IVL, SVL, and IVL/SVL
  - Supports IEEE 802.1Q VLAN
    - 512-entry VLAN Table
    - Port-based VLAN
- L2 Miscellaneous Functions
  - Supports RLDP (Realtek Loop Detection Protocol)
  - Supports cable diagnostics technology
  - Supports broadcast, multicast, unknown-multicast, and unknown-unicast packet suppression control
  - Supports IEEE 802.3az (Energy Efficient Ethernet, EEE) and Realtek Green Ethernet
  - Supports TX and RX Port Mirroring
  - Supports Link Aggregation (IEEE 802.3ad) for 4 groups of link aggregators with up to 8 ports per-group
  - Port isolation function enhances port security
- QoS Functions
  - Four priority queues per port
  - Supports SP, WRR, WFQ scheduling
  - Ingress and egress rate limiting per port
- MIB Functions
  - RFC2819 -- RMON MIB group 1, 2, 3, 9
  - RFC3635/RFC2863/RFC1213/RFC4188 /RFC4363
- Others
  - 55nm CMOS process
  - 3.3V/1.2V dual-power input
  - LQFP128 E-PAD package

3. Block Diagrams

3.1. RTL8316E Block Diagram

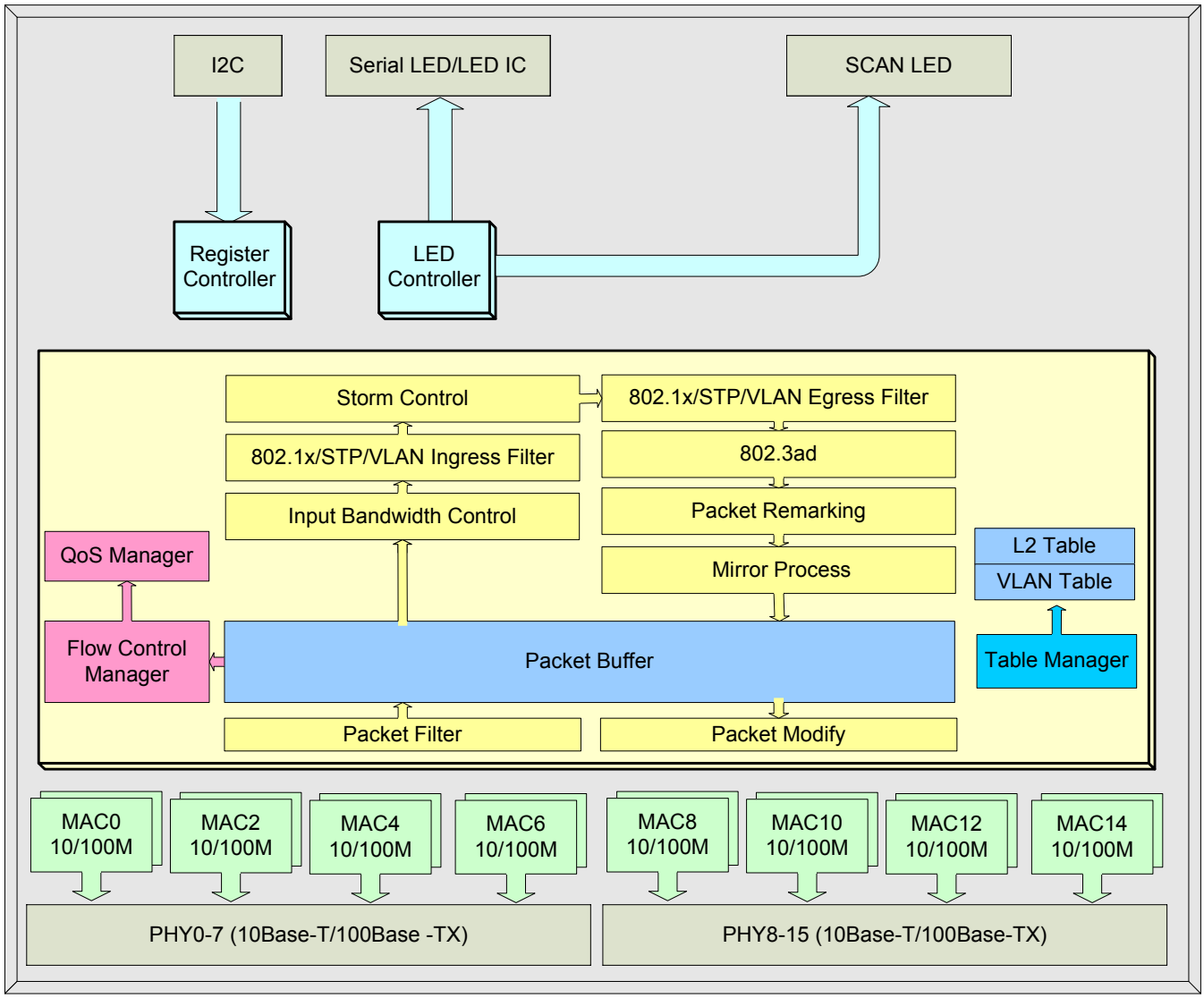


Figure 1. RTL8316E Block Diagram

3.2. RTL8324E Block Diagram

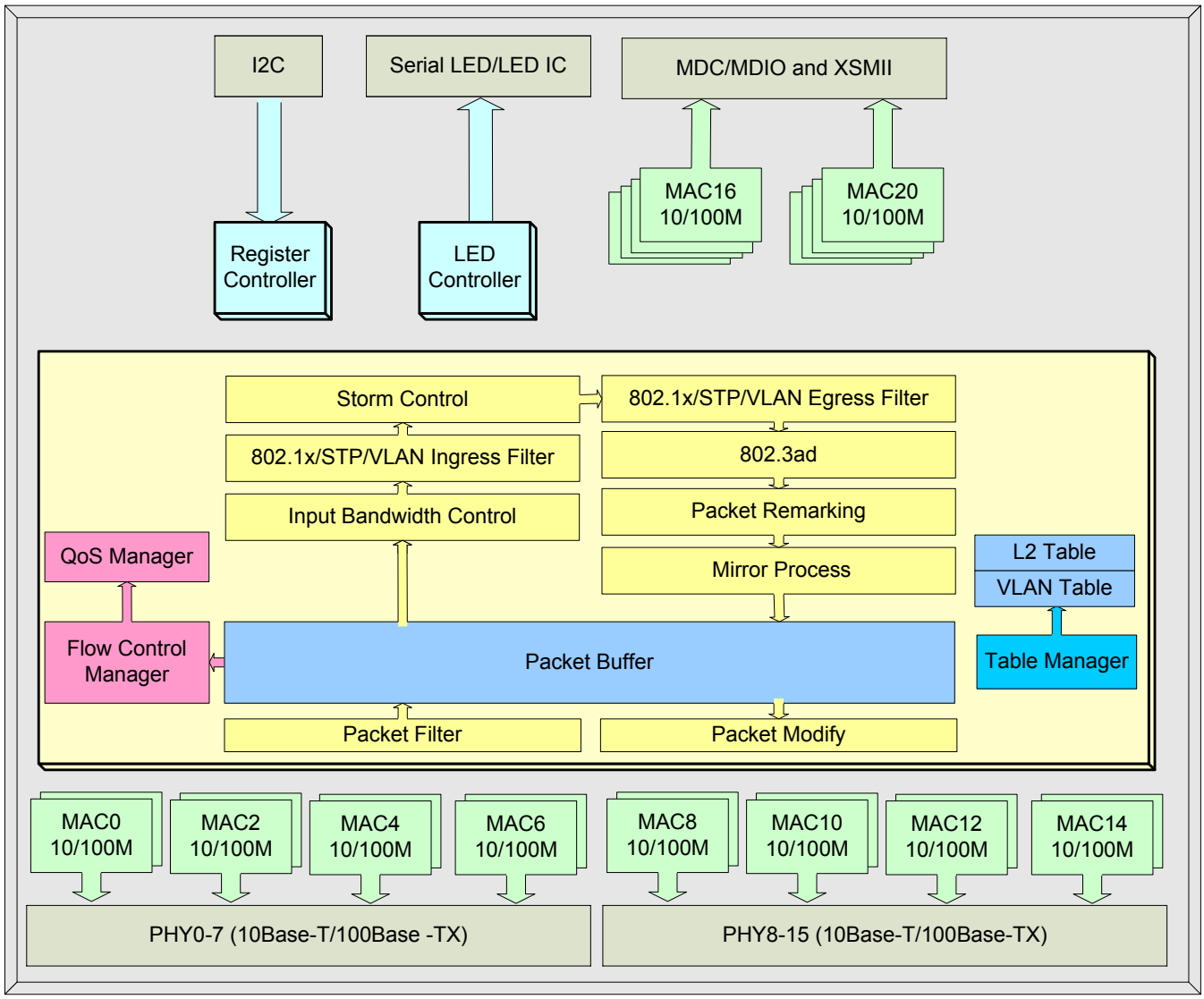


Figure 2. RTL8324E Block Diagram

4. System Applications

*4.1. RTL8316E: 16*10/100M Switch*

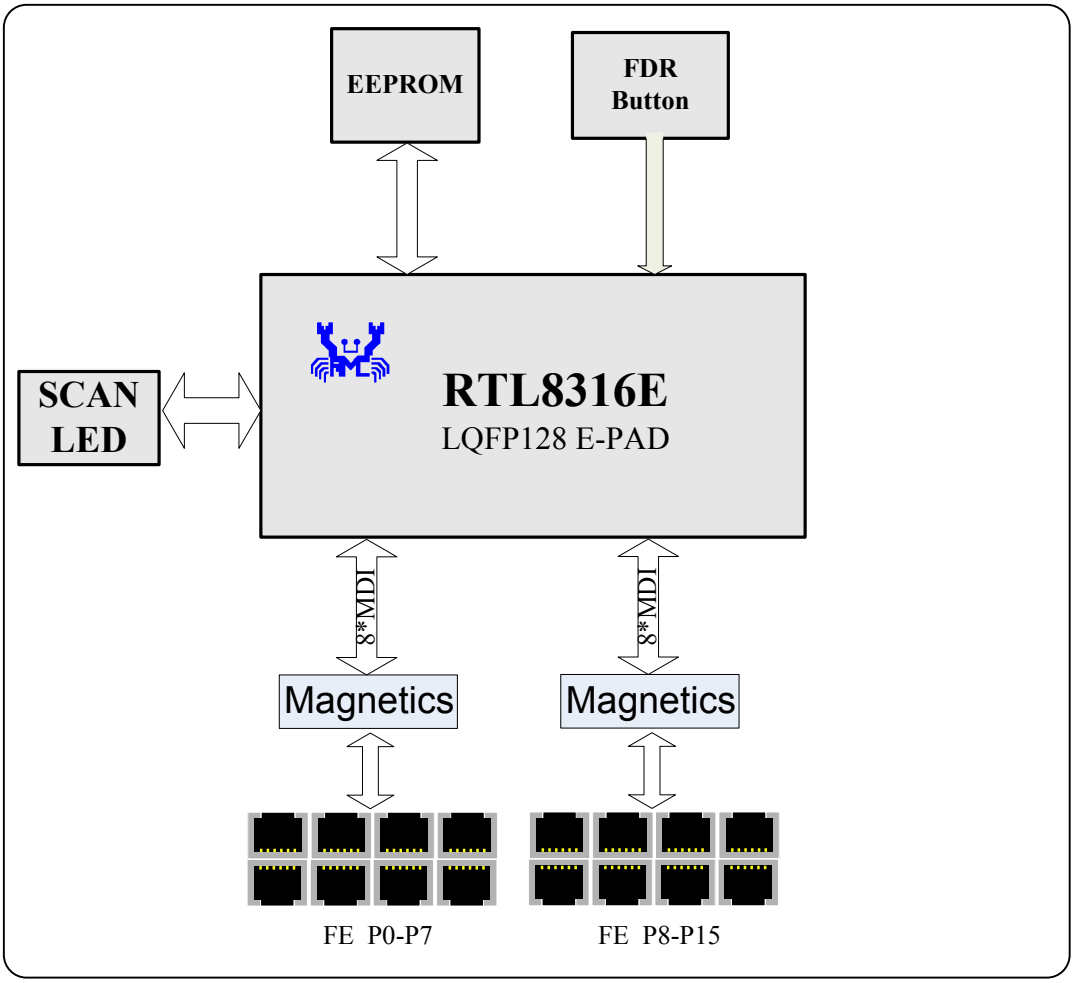


Figure 3. RTL8316E: 16*10/100M Switch

4.2. RTL8324E: 24*10/100M Switch

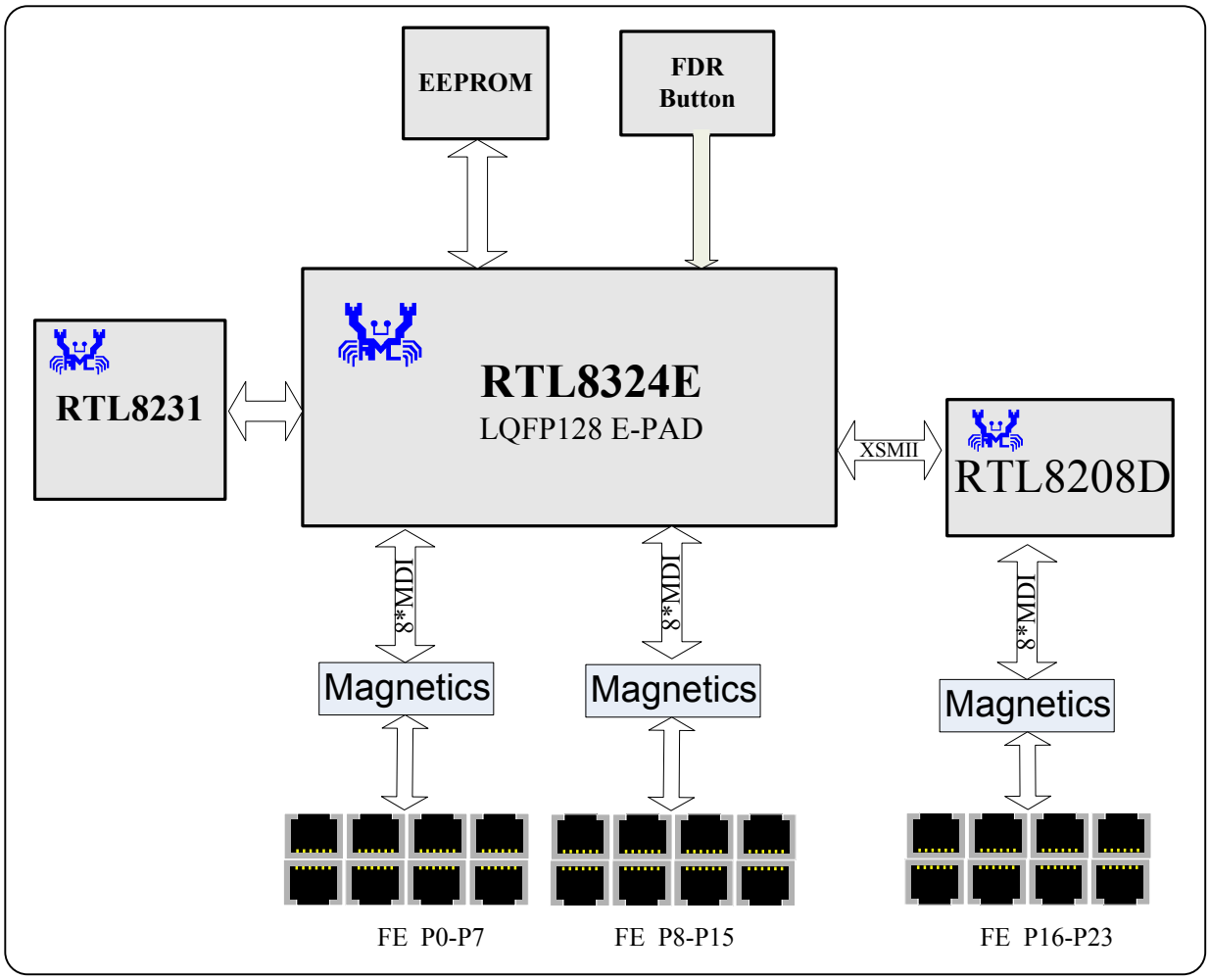


Figure 4. RTL8324E: 24*10/100M Switch

5. Pin Assignments and Descriptions (RTL8316E)

For RTL8324E Pin Assignments and Descriptions, see section 6, page 14.

5.1. Pin Assignments Figure (RTL8316E)

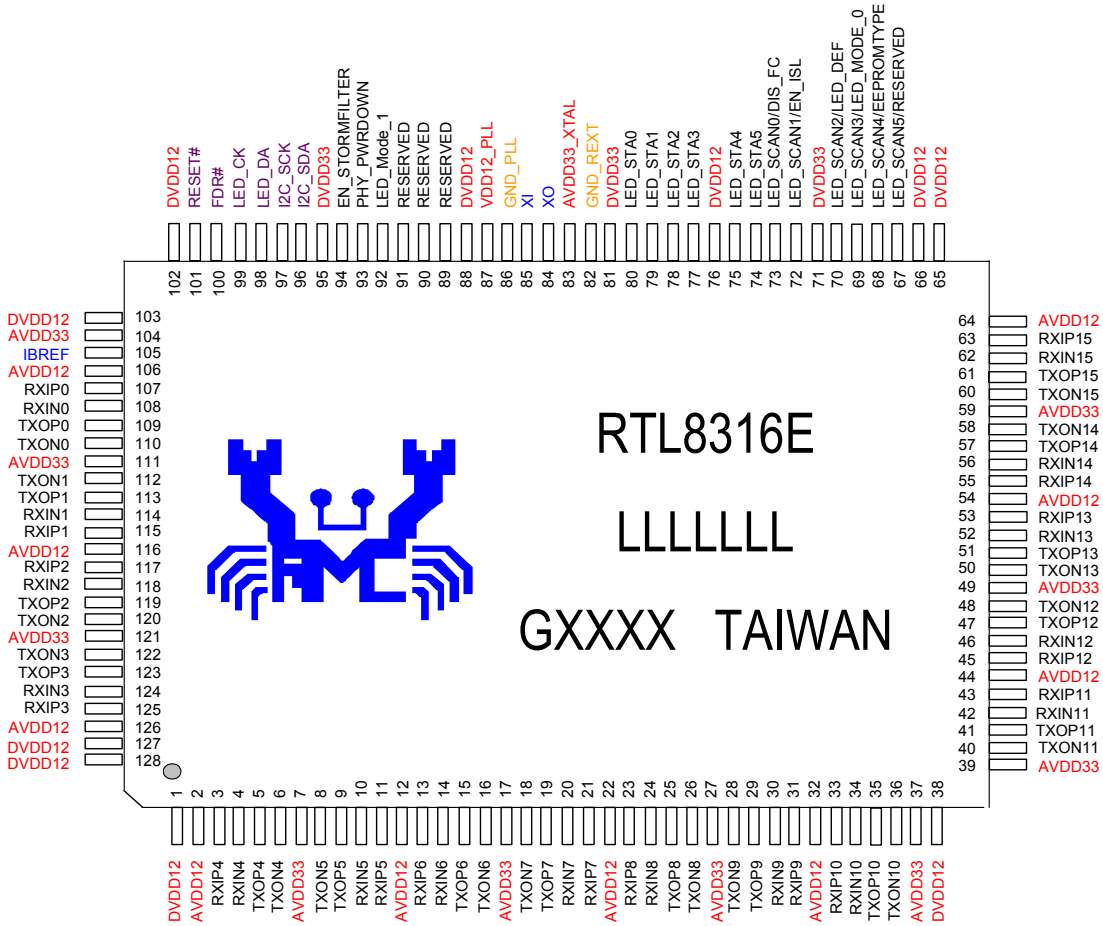


Figure 5. Pin Assignments (RTL8316E)

5.2. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 5).

5.3. Pin Assignments Table Definitions (RTL8316E)

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value is 75KΩ)

I_{PD}: Input Pin With Pull-Down Resistor; (Typical Value is 75KΩ)

I/O_{PU}: I_{PU} and O_{PU}

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value is 75KΩ)

O_{PD}: Output Pin With Pull-Down Resistor; (Typical Value is 75KΩ)

I/O_{PD}: I_{PD} and O_{PD}

5.4. Pin Assignments Table (RTL8316E)

Table 1. Pin Assignments Table (RTL8316E)

Name	Pin No.	Type
DVDD12	1	P
AVDD12	2	AP
RXIP4	3	AI/O
RXIN4	4	AI/O
TXOP4	5	AI/O
TXON4	6	AI/O
AVDD33	7	AP
TXON5	8	AI/O
TXOP5	9	AI/O
RXIN5	10	AI/O
RXIP5	11	AI/O
AVDD12	12	AP
RXIP6	13	AI/O
RXIN6	14	AI/O
TXOP6	15	AI/O
TXON6	16	AI/O
AVDD33	17	AP

Name	Pin No.	Type
TXON7	18	AI/O
TXOP7	19	AI/O
RXIN7	20	AI/O
RXIP7	21	AI/O
AVDD12	22	AP
RXIP8	23	AI/O
RXIN8	24	AI/O
TXOP8	25	AI/O
TXON8	26	AI/O
AVDD33	27	AP
TXON9	28	AI/O
TXOP9	29	AI/O
RXIN9	30	AI/O
RXIP9	31	AI/O
AVDD12	32	AP
RXIP10	33	AI/O
RXIN10	34	AI/O

Name	Pin No.	Type
TXOP10	35	AI/O
TXON10	36	AI/O
AVDD33	37	AP
DVDD12	38	P
AVDD33	39	AP
TXON11	40	AI/O
TXOP11	41	AI/O
RXIN11	42	AI/O
RXIP11	43	AI/O
AVDD12	44	AP
RXIP12	45	AI/O
RXIN12	46	AI/O
TXOP12	47	AI/O
TXON12	48	AI/O
AVDD33	49	AP
TXON13	50	AI/O
TXOP13	51	AI/O
RXIN13	52	AI/O
RXIP13	53	AI/O
AVDD12	54	AP
RXIP14	55	AI/O
RXIN14	56	AI/O
TXOP14	57	AI/O
TXON14	58	AI/O
AVDD33	59	AP
TXON15	60	AI/O
TXOP15	61	AI/O
RXIN15	62	AI/O
RXIP15	63	AI/O
AVDD12	64	AP
DVDD12	65	P
DVDD12	66	P
LED_SCAN5/RESERVED	67	I/O_{PD}
LED_SCAN4/EEPROMTYPE	68	I/O_{PD}
LED_SCAN3/LED_MODE_0	69	I/O_{PD}
LED_SCAN2/LED_DEF	70	I/O_{PD}
DVDD33	71	P
LED_SCAN1/EN_ISL	72	I/O_{PD}
LED_SCAN0/DIS_FC	73	I/O_{PD}
LED_STA5	74	O_{PD}
LED_STA4	75	O_{PD}
DVDD12	76	P
LED_STA3	77	O_{PD}
LED_STA2	78	O_{PD}

Name	Pin No.	Type
LED_STA1	79	O_{PD}
LED_STA0	80	O_{PD}
DVDD33	81	P
GND_REXT	82	AG
AVDD33_XTAL	83	AP
XO	84	AO
XI	85	AI
GND_PLL	86	AG
VDD12_PLL	87	AP
DVDD12	88	P
RESERVED	89	I/O_{PD}
RESERVED	90	I/O_{PD}
RESERVED	91	I/O_{PD}
LED_MODE_1	92	I_{PD}
PHY_PWRDOWN	93	I_{PD}
EN_STORMFILTER	94	I_{PD}
DVDD33	95	P
I2C_SDA	96	I/O_{PU}
I2C_SCK	97	I/O_{PU}
LED_DA	98	I/O_{PU}
LED_CK	99	O_{PU}
FDR#	100	I_{PU}
RESET#	101	AI_{PU}
DVDD12	102	P
DVDD12	103	P
AVDD33	104	AP
IBREF	105	AO
AVDD12	106	AP
RXIP0	107	AI/O
RXIN0	108	AI/O
TXOP0	109	AI/O
TXON0	110	AI/O
AVDD33	111	AP
TXON1	112	AI/O
TXOP1	113	AI/O
RXIN1	114	AI/O
RXIP1	115	AI/O
AVDD12	116	AP
RXIP2	117	AI/O
RXIN2	118	AI/O
TXOP2	119	AI/O
TXON2	120	AI/O
AVDD33	121	AP
TXON3	122	AI/O

Name	Pin No.	Type
TXOP3	123	AI/O
RXIN3	124	AI/O
RXIP3	125	AI/O
AVDD12	126	AP

Name	Pin No.	Type
DVDD12	127	P
DVDD12	128	P
DGND	EPAD	G

5.5. Pin Descriptions (RTL8316E)

5.5.1. Media Connection Pins (RTL8316E)

Table 2. Media Connection Pins (RTL8316E)

Pin Name	Pin No.	Type	Drive (mA)	Description
RXIP15/RXIN15 RXIP14/RXIN14 RXIP13/RXIN13 RXIP12/RXIN12 RXIP11/RXIN11 RXIP10/RXIN10 RXIP9/RXIN9 RXIP8/RXIN8 RXIP7/RXIN7 RXIP6/RXIN6 RXIP5/RXIN5 RXIP4/RXIN4 RXIP3/RXIN3 RXIP2/RXIN2 RXIP1/RXIN1 RXIP0/RXIN0	63, 62 55, 56 53, 52 45, 46 43, 42 33, 34 31, 30 23, 24 21, 20 13, 14 11, 10 3, 4 125, 124 117, 118 115, 114 107, 108	AI/O	-	Differential Receive Data Input: Port0~15 support 100Base-TX, 10Base-T
TXOP15/TXON15 TXOP14/TXON14 TXOP13/TXON13 TXOP12/TXON12 TXOP11/TXON11 TXOP10/TXON10 TXOP9/TXON9 TXOP8/TXON8 TXOP7/TXON7 TXOP6/TXON6 TXOP5/TXON5 TXOP4/TXON4 TXOP3/TXON3 TXOP2/TXON2 TXOP1/TXON1 TXOP0/TXON0	61, 60 57, 58 51, 50 47, 48 41, 40 35, 36 29, 28 25, 26 19, 18 15, 16 9, 8 5, 6 123, 122 119, 120 113, 112 109, 110	AI/O	-	Differential Transmit Data Output: Port0~15 support 100Base-TX, 10Base-T

5.5.2. Serial LED/LED IC Interface Pins (RTL8316E)

Table 3. Serial LED/LED IC Interface Pins (RTL8316E)

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_CK	99	O_{PU}	4	In Serial LED mode: Reference output clock for serial LED interface and Data is latched on the rising of LEDCK. In I2C-like LED mode: Reference output clock for I2C-like interface.
LED_DA	98	I/O_{PU}	4	Serial LED Data Output. In Serial LED mode: Serial bit stream of link status info. In I2C-like LED mode: The data written to LED IC.

5.5.3. SCAN LED Interface Pins (RTL8316E)

Table 4. SCAN LED Interface Pins (RTL8316E)

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_STA[5:0]	74, 75, 77, 78, 79, 80	O_{PD}	8	Scan LED Mode Status Pins.
LED_SCAN5/ RESERVED	67	I/O_{PD}	8	Scan LED Mode Scan Pins.
LED_SCAN4/ EEPROMTYPE	68			
LED_SCAN3/ LED_MODE_0	69			
LED_SCAN2/ LED_DEF	70			
LED_SCAN1/ EN_ISL	72			
LED_SCAN0/ DIS_FC	73			

5.5.4. Miscellaneous Interface Pins (RTL8316E)

Table 5. Miscellaneous Interface Pins (RTL8316E)

Pin Name	Pin No.	Type	Drive (mA)	Description
I2C_SCK	97	I/O_{PU}	4	I2C Interface Clock. For normal mode (100KHz), a cycle time is 10µs. For fast mode (400KHz), it is 2.5µs.
I2C_SDA	96	I/O_{PU}	4	I2C Interface Data Input/Output.
FDR#	100	I_{PU}	-	Factory default recovery input pin. Takes effect when asserted low for at least 3 seconds.
XI	85	AI	-	25MHz Crystal Clock Input and Feedback Pin.

Pin Name	Pin No.	Type	Drive (mA)	Description
XO	84	AO	-	25MHz Crystal Clock Output Pin.
RESET#	101	AI_{PU}	-	System Pin Reset Input.
IBREF	105	AO	-	Reference Resistor for PHY Bandgap. A 2.49KΩ (1%) resistor should be connected between IBREF and GND.
RESERVED	91, 90, 89	I/O_{PD}	-	Reserved for internal use.
RESERVED / LED_SCAN5	67	I/O_{PD}	-	Reserved for internal use.

5.5.5. Configuration Strapping Pins (RTL8316E)

Table 6. Configuration Strapping Pins (RTL8316E)

Pin Name	Pin No.	Type	Default	Description
EEPROMTYPE/ LED_SCAN4	68	I/O_{PD}	-	Select EEPROM Auto-Load Address Byte Size. 0: 2-Byte (default) 1: 1-Byte
LED_MODE_1 LED_MODE_0/ LED_SCAN3	92 69	I_{PD}	-	LED Mode Select. 00: Serial LED mode (default) 01: I2C-like LED mode 10: SCAN LED mode 11: Reserved
LED_DEF/ LED_SCAN2	70	I/O_{PD}	-	LED Status Default Mode Select. 0: Select mode0 (default) 1: Select mode1
EN_ISL/ LED_SCAN1	72	I/O_{PD}	-	Enable Port Isolation. 0: Disable port isolation (default) 1: Enable port isolation
DIS_FC/ LED_SCAN0	73	I/O_{PD}	-	Enable All Port Flow Control. 0: Enable (default) 1: Disable
PHY_PWRDOWN	93	I_{PD}	-	Enable PHY Power Down When Power On. 0: Normal (default) 1: Enable PHY power down when power on
EN_STORMFILTER	94	I_{PD}	-	Enable Broadcast Storm Filter. 0: Disable traffic storm filter (default) 1: Enable traffic storm filter

LED Group	Mode0	Mode1
LED0	Link/Act	Spd_{100}Link/Act
LED1	$Speed_{100}$	Spd_{10}Link/Act
LED2	$Speed_{10}$	Full Duplex

5.5.6. Power and GND Pins (RTL8316E)

Table 7. Power and GND Pins (RTL8316E)

Pin Name	Pin No.	Type	Description
AVDD33	7, 17, 27, 37, 39, 49, 59, 104, 111, 121	AP	Analog Power 3.3V.
AVDD12	2, 12, 22, 32, 44, 54, 64, 106, 116, 126	AP	Analog Power 1.2V.
DVDD33	71, 81, 95	P	Digital Power 3.3V for IO Pad.
DVDD12	1, 38, 65, 66, 76, 88, 102, 103, 127, 128	P	Digital Power 1.2V for Core Voltage.
VDD12_PLL	87	AP	Power for PLL.
GND_PLL	86	AG	Ground for PLL.
AVDD33_XTAL	83	AP	Analog Power for Crystal.
GND_REXT	82	AG	Analog Ground.

6. Pin Assignments and Descriptions (RTL8324E)

For RTL8316E Pin Assignments and Descriptions, see section 5, page 7.

6.1. Pin Assignments Figure (RTL8324E)

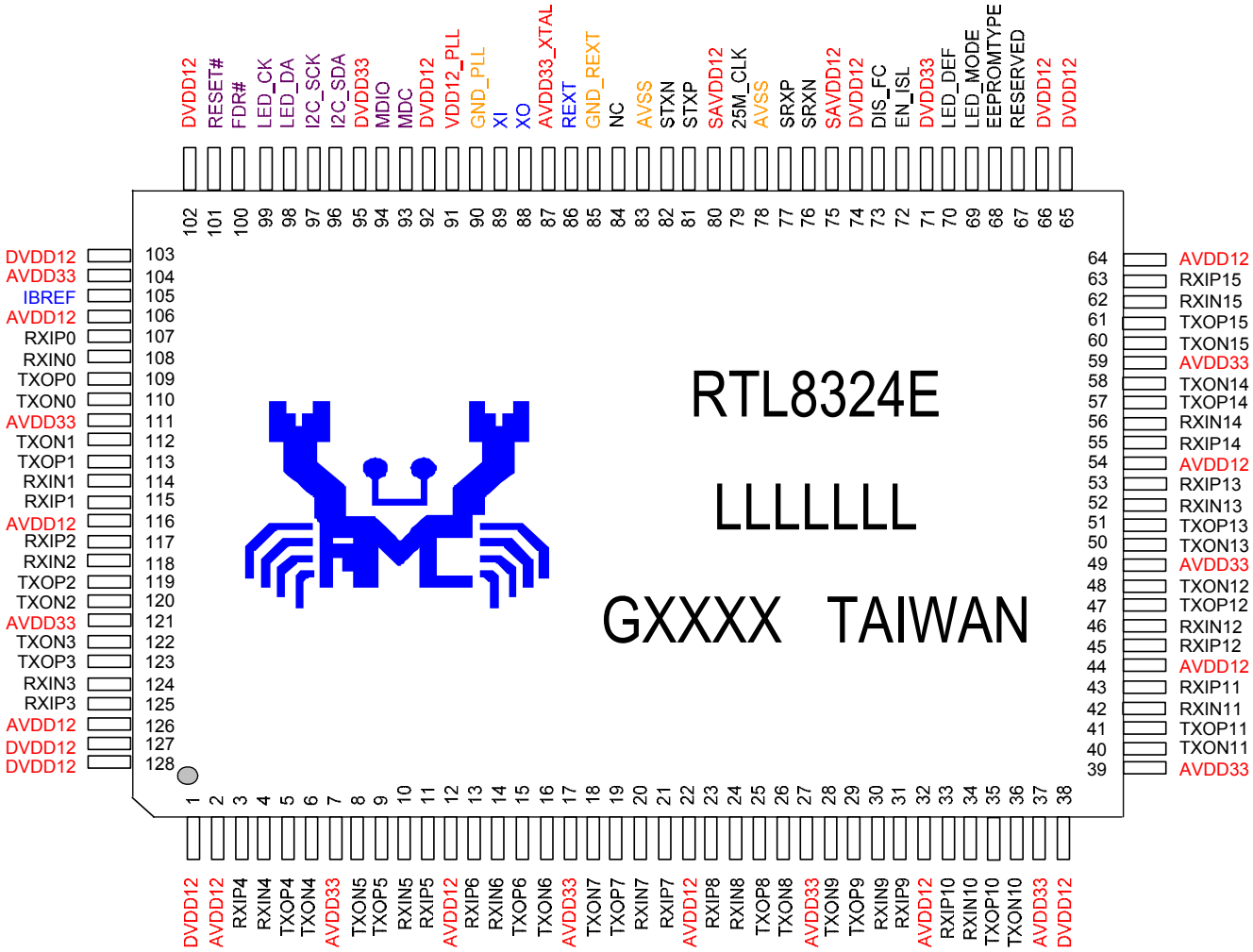


Figure 6. Pin Assignments (RTL8324E)

6.2. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 6).

6.3. Pin Assignments Table Definitions (RTL8324E)

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value approximately 75KΩ)

I_{PD}: Input Pin With Pull-Down Resistor; (Typical Value approximately 75KΩ)

I/O_{PU}: I_{PU} and O_{PU}

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value approximately 75KΩ)

O_{PD}: Output Pin With Pull-Down Resistor; (Typical Value approximately 75KΩ)

I/O_{PD}: I_{PD} and O_{PD}

6.4. Pin Assignments Table (RTL8324E)

Table 8. RTL8324E Pin Assignments Table (RTL8324E)

Name	Pin No.	Type
DVDD12	1	P
AVDD12	2	AP
RXIP4	3	AI/O
RXIN4	4	AI/O
TXOP4	5	AI/O
TXON4	6	AI/O
AVDD33	7	AP
TXON5	8	AI/O
TXOP5	9	AI/O
RXIN5	10	AI/O
RXIP5	11	AI/O
AVDD12	12	AP
RXIP6	13	AI/O
RXIN6	14	AI/O
TXOP6	15	AI/O
TXON6	16	AI/O
AVDD33	17	AP

Name	Pin No.	Type
TXON7	18	AI/O
TXOP7	19	AI/O
RXIN7	20	AI/O
RXIP7	21	AI/O
AVDD12	22	AP
RXIP8	23	AI/O
RXIN8	24	AI/O
TXOP8	25	AI/O
TXON8	26	AI/O
AVDD33	27	AP
TXON9	28	AI/O
TXOP9	29	AI/O
RXIN9	30	AI/O
RXIP9	31	AI/O
AVDD12	32	AP
RXIP10	33	AI/O
RXIN10	34	AI/O

Name	Pin No.	Type
TXOP10	35	AI/O
TXON10	36	AI/O
AVDD33	37	AP
DVDD12	38	P
AVDD33	39	AP
TXON11	40	AI/O
TXOP11	41	AI/O
RXIN11	42	AI/O
RXIP11	43	AI/O
AVDD12	44	AP
RXIP12	45	AI/O
RXIN12	46	AI/O
TXOP12	47	AI/O
TXON12	48	AI/O
AVDD33	49	AP
TXON13	50	AI/O
TXOP13	51	AI/O
RXIN13	52	AI/O
RXIP13	53	AI/O
AVDD12	54	AP
RXIP14	55	AI/O
RXIN14	56	AI/O
TXOP14	57	AI/O
TXON14	58	AI/O
AVDD33	59	AP
TXON15	60	AI/O
TXOP15	61	AI/O
RXIN15	62	AI/O
RXIP15	63	AI/O
AVDD12	64	AP
DVDD12	65	P
DVDD12	66	P
RESERVED	67	I/O_{PD}
EEPROMTYPE	68	I_{PD}
LED_MODE	69	I_{PD}
LED_DEF	70	I_{PD}
DVDD33	71	P
EN_ISL	72	I_{PD}
DIS_FC	73	I_{PD}
DVDD12	74	P
SAVDD12	75	AP
SRXN	76	AI
SRXP	77	AI
AVSS	78	AG

Name	Pin No.	Type
25M_CLKO	79	O
SAVDD12	80	AP
STXP	81	AO
STXN	82	AO
AVSS	83	AG
NC	84	
GND_REXT	85	AG
REXT	86	AO
AVDD33_XTAL	87	AP
XO	88	AO
XI	89	AI
GND_PLL	90	AG
VDD12_PLL	91	AP
DVDD12	92	P
MDC	93	O_{PU}
MDIO	94	I/O_{PU}
DVDD33	95	P
I2C_SDA	96	I/O_{PU}
I2C_SCK	97	I/O_{PU}
LED_DA	98	I/O_{PU}
LED_CK	99	O_{PU}
FDR#	100	I_{PU}
RESET#	101	AI_{PU}
DVDD12	102	P
DVDD12	103	P
AVDD33	104	AP
IBREF	105	AO
AVDD12	106	AP
RXIP0	107	AI/O
RXIN0	108	AI/O
TXOP0	109	AI/O
TXON0	110	AI/O
AVDD33	111	AP
TXON1	112	AI/O
TXOP1	113	AI/O
RXIN1	114	AI/O
RXIP1	115	AI/O
AVDD12	116	AP
RXIP2	117	AI/O
RXIN2	118	AI/O
TXOP2	119	AI/O
TXON2	120	AI/O
AVDD33	121	AP
TXON3	122	AI/O

Name	Pin No.	Type
TXOP3	123	AI/O
RXIN3	124	AI/O
RXIP3	125	AI/O
AVDD12	126	AP

Name	Pin No.	Type
DVDD12	127	P
DVDD12	128	P
DGND	EPAD	G

6.5. Pin Descriptions (RTL8324E)

6.5.1. Media Connection Pins (RTL8324E)

Table 9. Media Connection Pins (RTL8324E)

Pin Name	Pin No.	Type	Drive (mA)	Description
RXIP15/RXIN15 RXIP14/RXIN14 RXIP13/RXIN13 RXIP12/RXIN12 RXIP11/RXIN11 RXIP10/RXIN10 RXIP9/RXIN9 RXIP8/RXIN8 RXIP7/RXIN7 RXIP6/RXIN6 RXIP5/RXIN5 RXIP4/RXIN4 RXIP3/RXIN3 RXIP2/RXIN2 RXIP1/RXIN1 RXIP0/RXIN0	63, 62 55, 56 53, 52 45, 46 43, 42 33, 34 31, 30 23, 24 21, 20 13, 14 11, 10 3, 4 125, 124 117, 118 115, 114 107, 108	AI/O	-	Differential Receive Data Input: Port0~15 supports 100Base-TX, 10Base-T
TXOP15/TXON15 TXOP14/TXON14 TXOP13/TXON13 TXOP12/TXON12 TXOP11/TXON11 TXOP10/TXON10 TXOP9/TXON9 TXOP8/TXON8 TXOP7/TXON7 TXOP6/TXON6 TXOP5/TXON5 TXOP4/TXON4 TXOP3/TXON3 TXOP2/TXON2 TXOP1/TXON1 TXOP0/TXON0	61, 60 57, 58 51, 50 47, 48 41, 40 35, 36 29, 28 25, 26 19, 18 15, 16 9, 8 5, 6 123, 122 119, 120 113, 112 109, 110	AI/O	-	Differential Transmit Data Output: Port0~15 supports 100Base-TX, 10Base-T

6.5.2. Serial LED Interface Pins (RTL8324E)

Table 10. LED Interface Pins (RTL8324E)

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_CK	99	O_{PU}	4	In Serial LED Mode: Reference output clock for serial LED interface and Data is latched on the rising of LEDCK. In I2C-like LED Mode: Reference output clock for I2C-like interface.
LED_DA	98	I/O_{PU}	4	Serial LED Data Output. In Serial LED Mode: Serial bit stream of link status info. In I2C-like LED mode: The data written to LED IC.

6.5.3. Miscellaneous Interface Pins (RTL8324E)

Table 11. Miscellaneous Interface Pins (RTL8324E)

Pin Name	Pin No.	Type	Drive (mA)	Description
I2C_SCK	97	I/O_{PU}	4	I2C Interface Clock. For normal mode (100KHz), one cycle time is 10µs. For fast mode (400KHz), it is 2.5µs.
I2C_SDA	96	I/O_{PU}	4	I2C Interface Data Input/Output.
MDC	94	O_{PU}	8	MII Management Interface Clock Pin.
MDIO	93	I/O_{PU}	8	MII Management Interface Data Pin.
FDR#	100	I_{PU}	-	Factory Default Recovery Input Pin. Takes effect when pulled down for at least 3 seconds.
XI	89	AI	-	25MHz Crystal Clock Input and Feedback Pin.
XO	88	AO	-	25MHz Crystal Clock Output Pin.
RESET	101	AI_{PU}	-	System Pin Reset Input.
IBREF	105	AO	-	Reference Resistor for the Chip. A 2.49KΩ (1%) resistor should be connected between IBREF and GND.
RESERVED	67	I/O_{PD}	-	Reserved for internal use.

6.5.4. Configuration Strapping Pins (RTL8324E)

Table 12. Configuration Strapping Pins (RTL8324E)

Pin Name	Pin No.	Type	Drive (mA)	Description
EEPROMTYPE	68	I_{PD}	-	Select EEPROM Auto-Load Address Byte Size. 0: 2-Byte (default) 1: 1-Byte
LED_MODE	69	I_{PD}	-	LED Mode Select. 0: Serial LED mode (default) 1: I2C-like LED mode

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_DEF	70	I_{PD}	-	LED Status Default Mode Select. 0: Select mode0 (default) 1: Select mode1 LED Group / Mode0 / Mode1: LED0 / Link/Act / Spd_{100}Link/Act LED1 / $Speed_{100}$ / Spd_{10}Link/Act LED2 / $Speed_{10}$ / Full Duplex
EN_ISL	72	I_{PD}	-	Enable Port Isolation. 0: Disable port isolation (default) 1: Enable port isolation
DIS_FC	73	I_{PD}	-	Enable All Port Flow Control. 0: Enable (default) 1: Disable

6.5.5. XSMII Interface Pins (RTL8324E)

Table 13. XSMII Interface Pins (RTL8324E)

Pin Name	Pin No.	Type	Drive (mA)	Description
STXP/STXN	81, 82	AO	-	XSMII Interface Transmit Data Differential Output Pair.
SRXP/SRXN	77, 76	AI	-	XSMII Interface Receive Data Differential Input Pair.
25M_CLKO	79	O	4	25MHz Clock Output.
REXT	86	AO	-	Reference Resistor for XSMII Bandgap. A 12KΩ (1%) resistor should be connected between REXT and GND.
GND_REXT	85	AG	-	Ground for XSMII Bandgap.

6.5.6. Power and GND Pins (RTL8324E)

Table 14. Power and GND Pins (RTL8324E)

Pin Name	Pin No.	Type	Description
AVDD33	7, 17, 27, 37, 39, 49, 59, 104, 111, 121	AP	Analog Power 3.3V.
AVDD12	2, 12, 22, 32, 44, 54, 64, 106, 116, 126	AP	Analog Power 1.2V.
DVDD33	71, 95	P	Digital Power 3.3V for IO Pad.
DVDD12	1, 38, 65, 66, 74, 92, 102, 103, 127, 128	P	Digital Power 1.2V for Core Voltage.
VDD12_PLL	91	AP	Power for PLL.
GND_PLL	90	AG	Ground for PLL.
AVDD33_XTAL	87	AP	Analog Power for Crystal.
SAVDD12	75, 80	AP	Analog Power for XSMII.
AVSS	78	AG	Analog Ground for XSMII.

7. Physical Layer Functional Overview

7.1. MDI Interface

The RTL8316E/RTL8324E embeds 16 Fast Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 100Base-TX and 10Base-T. This interface consists of two signal pairs RXIP/RXIN, and TXOP/TXON. The MDI interface has internal termination resistors for reduced BOM cost and PCB complexity.

7.2. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.3. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.4. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.5. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.6. Auto-Negotiation for UTP

The RTL8316E/RTL8324E obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8316E/RTL8324E advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.7. Crossover Detection and Auto Correction

During the link setup phase, the RTL8316E/RTL8324E checks whether it receives active signals on every port in order to determine if a connection can be established. The RTL8316E/RTL8324E can identify the type of connected cable and sets the port to MDI or MDIX. When in MDI mode, the RTL8316E/RTL8324E uses TXOP/N as transmit pair; when in MDIX mode, the RTL8316E/RTL8324E uses RXIP/N as transmit pair.

7.8. Polarity Correction

The RTL8316E/RTL8324E automatically corrects polarity errors on the receiver pairs in 10Base-T mode. In 100Base-TX mode, the polarity does not matter.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

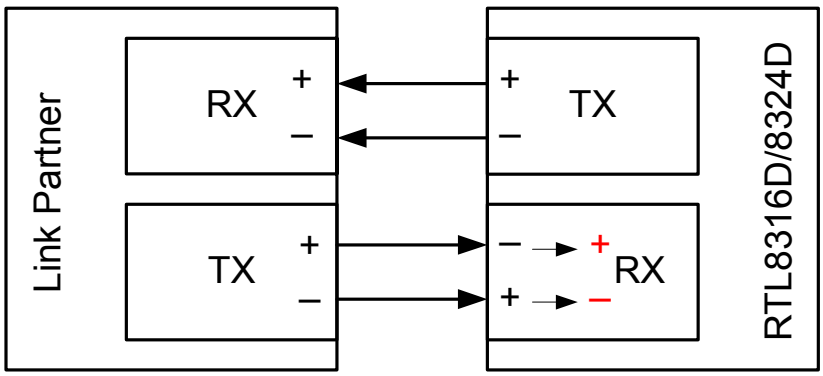


Figure 7. Conceptual Example of Polarity Correction

8. Switch Function Description

8.1. Hardware Reset and Software Reset

8.1.1. Hardware Reset

A hardware reset forces the RTL8316E/RTL8324E to start the initial power-on sequence. First hardware will strap pins to give all default values when the 'RESET' signal terminates. Next the configuration is auto-loaded from EEPROM (if EEPROM is detected), and then the complete SRAM BIST (Built-In Self Test) process is run.

8.1.2. Software Reset

The RTL8316E/RTL8324E supports a Switch Soft reset to reset the Switch packet buffer. All reset signals are low active.

8.2. Layer 2 Learning and Forwarding

The RTL8316E/RTL8324E supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning).

8.2.1. Learning

The RTL8316E/RTL8324E features a Layer 2 hash table (8K-entry). It uses a 4-way hash structure to store L2 entries. The L2 Unicast hash key is {MAC, FID/VID}.

8.2.2. Forwarding

When the VLAN egress filtering option is enabled, a received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded.

By default the received broadcast/multicast frame will flood to VLAN member ports only, except for the source port.

8.2.3. Address Table Aging

In a dynamic network topology, address aging allows the contents of the address table to always be the most recent and correct. A learned source address entry will be cleared (aged out) if it is not updated by the address learning process within an aging time period. The aging timer of the MAC address lookup table can be configured to between 1~65535 seconds (default value is approximately 300s).

8.3. Reserved Multicast Address Handling

The RTL8316E/RTL8324E supports Reserved Multicast Address (RMA) as defined in the IEEE 802.1 standard. For each RMA, the actions include Forward and Drop. The action priority is higher than the results of a L2 Table lookup. Default actions are shown in Table 15.

Table 15. Reserved Multicast Address Default Actions

Name	Address	Default
Bridge Group Address	01-80-C2-00-00-00	Forward
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01	Drop
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02	Drop
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03	Forward
Reserved for future protocol standards	01-80-C2-00-00-04~01-80-C2-00-00-0D, 01-80-C2-00-00-0F	Drop
LLDP IEEE Std 802.1AB Link Layer Discovery Protocol Multicast Address	01-80-C2-00-00-0E	Forward
All LANs Bridge Management Group Address	01-80-C2-00-00-10	Drop
GMRP	01-80-C2-00-00-20	Drop
GVRP	01-80-C2-00-00-21	Forward
Reserved for use by Multiple Registration Protocol (MRP) applications	01-80-C2-00-00-22~01-80-C2-00-00-2F	Drop
IEEE 802.1ag PDU CCM/LTM	01-80-C2-00-00-31~01-80-C2-00-00-3F	Forward

8.4. IEEE 802.3x Flow Control

The RTL8316E/RTL8324E supports IEEE 802.3x full duplex flow control. If one port's receive buffer is over the pause-on threshold, a pause-on frame is sent to the link partner to stop the transmission. When the port's receive buffer drops below the pause-off threshold, it sends a pause-off frame. The pause frame format is shown in Figure 8.

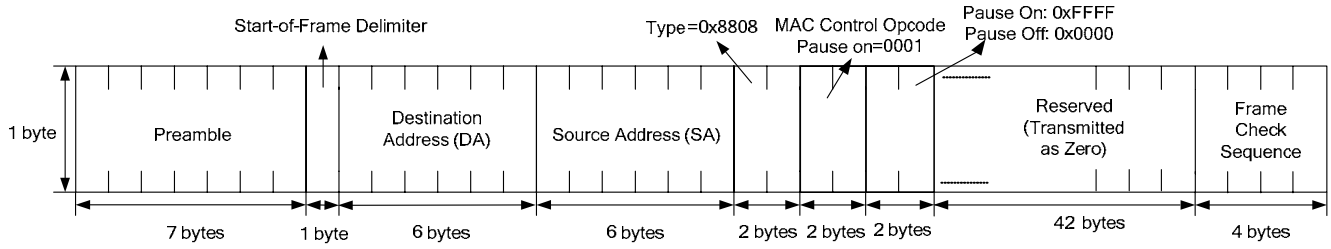


Figure 8. TX Pause Frame Format

The flow control mechanism of the RTL8316E/RTL8324E is implemented on the RX side. It counts the received pages on the RX side in order to determine on which port it should send out Pause On/Off packets.

When RTL8316E/RTL8324E flow control is enabled, the initial state is 'Non_Congest'. The state is monitored continuously. If a pause-on trigger condition occurs, it enters the 'Congest' state. When in the

'congest' state, it is also continuously monitored. When a pause-off trigger condition occurs it re-enters the 'Non_Congest' state. Figure 9 shows the flow control state machine.

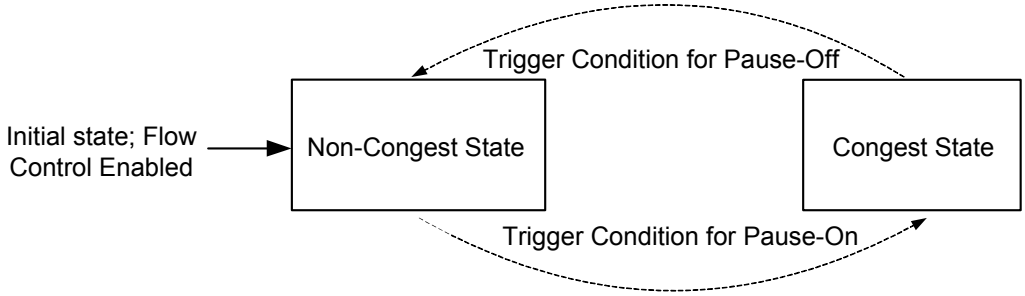


Figure 9. Flow Control State Machine

8.5. Half Duplex Backpressure

There are two mechanisms for half-duplex backpressure: collision-based or carrier-based.

8.5.1. Collision-Based Backpressure (Jam Mode)

If the input buffer is ready to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- The RTL8316E/RTL8324E will drive TXEN to high and send a 4-byte Jam signal (pattern is 0x55). The RTL8316E/RTL8324E will then drive TXEN to low.
- When the link partner receives the Jam signal, it will feedback a 4-byte signal (pattern is 0xFF), then it will drive RXDV to low.
- The link partner waits for a random back-off time then re-sends the packet. The timing is shown in Figure 10.

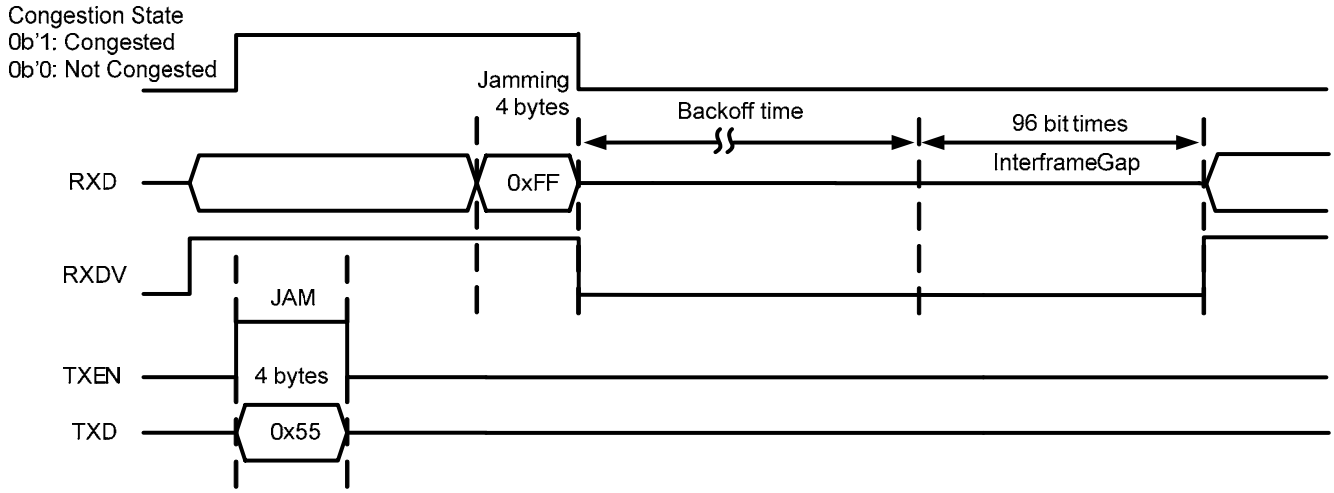


Figure 10. Collision-Based Backpressure Signal Timing

8.5.2. Carrier-Based Backpressure (Defer Mode)

If the input buffer is about to overflow, this mechanism will send a 0x55 pattern to defer the other station's transmission. The RTL8316E/RTL8324E will continuously send the defer signal until the input buffer overflow is resolved.

8.6. IEEE 802.3az Energy Efficient Ethernet (EEE)

The RTL8316E/RTL8324E supports IEEE 802.3az Energy Efficient Ethernet (EEE) ability for 100Base-TX in full duplex operation, and supports 10Base-Te for 10Base-T in full/half duplex .The Energy Efficient Ethernet (EEE) operational mode combines the IEEE 802.3 Media Access Control (MAC) Sub-layer with a family of Physical Layers defined to support operation in Low Power Idle (LPI) Mode. When the port is in LPI Mode, link partners of both sides can turn off the unnecessary TX/RX circuits to save power consumption during periods of low link utilization.

The RTL8316E/RTL8324E EEE operational mode supports the IEEE 802.3 MAC operation at 100Mbps. In addition, the RTL8316E/RTL8324E supports 10Mbps PHY with reduced transmit amplitude requirements in EEE operational mode. This new PHY is fully interoperable with legacy 10Base-T PHY over 100m of Class-D (Category 5) or better cabling.

8.7. Green Ethernet

8.7.1. Link Down Power Saving

The RTL8316E/RTL8324E implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. A port automatically enters link down power saving mode ten seconds after the cable is disconnected from it. Once a port enters link down power saving mode, it transmits normal link pulses on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect incoming signals, which might be 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

8.8. IEEE 802.1p and IEEE 802.1Q (VLAN)

The RTL8316E/RTL8324E supports IEEE 802.1p and 802.1Q tag-based, port-based VLAN. It provides a 512-entry VLAN table and 16-entry VLAN CAM table. VLAN table lookup applies a 4-Way hash algorithm, and the CAM table is used to resolve hash collisions.

The RTL8316E/RTL8324E uses VID[0:6] as an index to the VLAN table. If the remaining 5-bit VID[7:11] is matched in the entry, it means this entry lookup is a hit. If the VLAN table lookup fails, the chip will perform a lookup in the 16-entry VLAN CAM table.

The RTL8316E/RTL8324E features an ingress filter function; packets from an input port that is not in the member set will be dropped. This function can be enabled or disabled via register configuration.

8.9. Loop Detection

The RTL8316E/RTL8324E periodically transmits a Realtek protocol frame to detect network loop faults. If a port detects a loop, the LED corresponding to the looped port will blink until the loop is resolved. At the same time, the loop event flag will be set.

8.10. Layer 2 Traffic Suppression (Storm Control)

The RTL8316E/RTL8324E supports the storm filter function for each port. The storm types are broadcast storm, known multicast storm, unknown multicast storm, and unknown DA unicast storm. The RTL8316E/RTL8324E can control the four storm types via one leaky bucket per port.

8.11. IEEE 802.3ad Link Aggregation Protocol

The RTL8316E/RTL8324E supports 802.3ad (Link Aggregation) for 4 groups of link aggregators with up to 8 ports per-group. The chosen ports must be in full duplex mode and they must have the same attributes (for example: All 100Mbps or all 10Mbps). The link aggregation group is regarded as one logical port and has an ID (the lowest port number of the physically aggregated port members is used as its ID).

8.12. Bandwidth Control

8.12.1. Input Bandwidth Control

The RTL8316E/RTL8324E has input bandwidth control per port. If the speed of received packets is faster than the bandwidth setting of this port, the switch will send a pause frame to the link partner or drop packets, according to its flow control setting.

8.12.2. Output Bandwidth Control

The RTL8316E/RTL8324E has output bandwidth control per port, and has output bandwidth control per queue in WRR mode. The bandwidth granularity is 16Kbps.

8.13. Quality of Service (QoS)

The RTL8316E/RTL8324E identifies the priority of packets based on three types of QOS priority information:

- Port-based
- IEEE 802.1Q-based
- DSCP-based

8.13.1. Priority Arbitration

The RTL8316E/RTL8324E has two priority arbitration weight tables to decide which type of priority should be accepted when multiple types of priority exist. Each port can be set to its own Priority arbitration weight.

8.13.2. Port-Based Priority Assignment

Port-based priority assignment specifies a 3-bit priority for each physical port. When a packet is received from a physical port, it is assigned the 3-bit priority of that physical port.

8.13.3. IEEE 802.1Q-Based Priority Assignment

In IEEE 802.1Q-based priority assignment, when a packet is VLAN-tagged or priority-tagged, the 3-bit priority is specified by tag. When a packet is untagged, the 802.1Q-based priority is assigned to the default 3-bit priority information of a physical port. Each port must provide a default 3-bit priority (every received packet must be assigned a 3-bit 1Q-Based Priority). When the priority comes from a packet, the 1Q-based priority is acquired by mapping 3-bit tag priority to 3-bit priority though a RTL8316E/RTL8324E 1Q-based Priority Mapping Table. The 1Q-based priority can be disabled.

8.13.4. DSCP-Based Priority Assignment

The RTL8316E/RTL8324E has 2 tables to map 6-bit DSCP values to 3-bit internal priorities. Each table has 64 entries. Each port can decide which table to use. The DSCP-based priority assignment can be disabled by setting its weight to 0 in the Priority arbitration weight table.

8.13.5. Internal Priority to Queue ID Table

The RTL8316E/RTL8324E can transfer its internal priority to the output queue ID. Each port has a table with 8 entries to map the 3-bit internal priority to 2-bit queue ID.

8.14. Packet Scheduling (WRR and WFQ)

The RTL8316E/RTL8324E has four queues per port. The Packet Scheduler controls the multiple traffic classes (i.e., controls the packet sending sequence of the priority queue). The RTL8316E/RTL8324E has two scheduling algorithms: Weighted Round-Robin (WRR) and Weighted Fair-Queuing (WFQ). Note that the Strict Priority queue is the highest priority of all queues, and overrides WFQ & WRR. A larger strict priority queue ID indicates the priority is higher.

The Scheduler operates as follows:

- Weighted Fair-Queuing (WFQ): Byte-count
- Weighted Round-Robin (WRR): Packet-count

Note that WFQ and WRR cannot exist at the same time.

8.15. Egress Packet Remarking

RTL8316E/RTL8324E Remarking can be divided into 1p remarking and DSCP remarking. For 1p remarking, there is an internal priority to user priority table that is used to configure the final user priority value for the whole system. DSCP remarking also has an internal priority to DSCP priority table.

8.16. Ingress and Egress Port Mirror

If a frame meets the Ingress and Egress mirroring port conditions, the RTL8316E/RTL8324E duplicates the packet to the mirroring port. The RTL8316E/RTL8324E has one mirror set, and the mirroring port can monitor several mirrored ports simultaneously. For flow control, the mirroring port will send PAUSE frames or backpressure signals to the mirrored port. The QoS output port drop function can be enabled by software on the mirroring port.

8.17. Management Information Base (MIB)

The RTL8316E/RTL8324E MIB (Management Information Base) counters include:

- RFC2819 – RMON MIB Group 1, 2, 3, 9
- RFC3635 – Ethernet-like MIB
- RFC2863 – Interface Group MIB
- RFC1213 – MIB II
- RFC4188 – Bridge MIB
- RFC4363 – Bridge MIB Extension

8.18. Realtek Cable Tester

The RTL8316E/RTL8324E features the Realtek Cable Tester (RTCT). The Cable Tester function can be used to detect a short (two conductors of a pair have short-circuited) or open (a lack of continuity between the pins at each end of the Ethernet cable, or a disconnected cable) in each differential pair, and report the result in corresponding registers. The RTL8316E/RTL8324E also has an LED to indicate test status and results.

8.19. EEPROM Configuration

The EEPROM can be divided into two sizes: 4Kb~8Kb and 32Kb~512Kb. Using the small size EEPROM will reduce the time required to load code, as well as the cost. The address size of the small size EEPROM is 8 bits, while the larger EEPROM size is 16 bits (addressable space up to 64K). The small and large size EEPROM address timing waveform is different, and the auto-load size is shown in the register.

- Small Size EEPROM: Uses a control byte to define the EEPROM device address. Each block is 8-bit addressable, and its size is 256*8-bits. A 4Kb EEPROM supports two blocks, and an 8Kb EEPROM supports four blocks.
- Large Size EEPROM: Uses a control byte to define a one-block EEPROM device address. This block is addressable by 12~16 bits (i.e., 4K~64K range), and its size is 4K*8-bits =32Kb, to 64K*8-bits =512Kb). 32Kb supports 12-bit addresses, and 512Kb supports 16-bit addresses.

The RTL8316E/RTL8324E supports an EEPROM Factory Default Reset function. This function can be triggered by an input pin or FDR register. In order to prevent mis-operation, the FDR pin reset duration should be longer than 3 seconds.

9. Interface Descriptions

9.1. XSMII Interconnection

XSMII (Eight Serial Media Independent Interface) reduces PCB complexity and IC pin count. This innovative serial interface provides an up to 5 inch MAC to PHY communication path. XSMII can carry the half/full duplex Megabit Ethernet data streams of eight ports simultaneously, using only 4 pins.

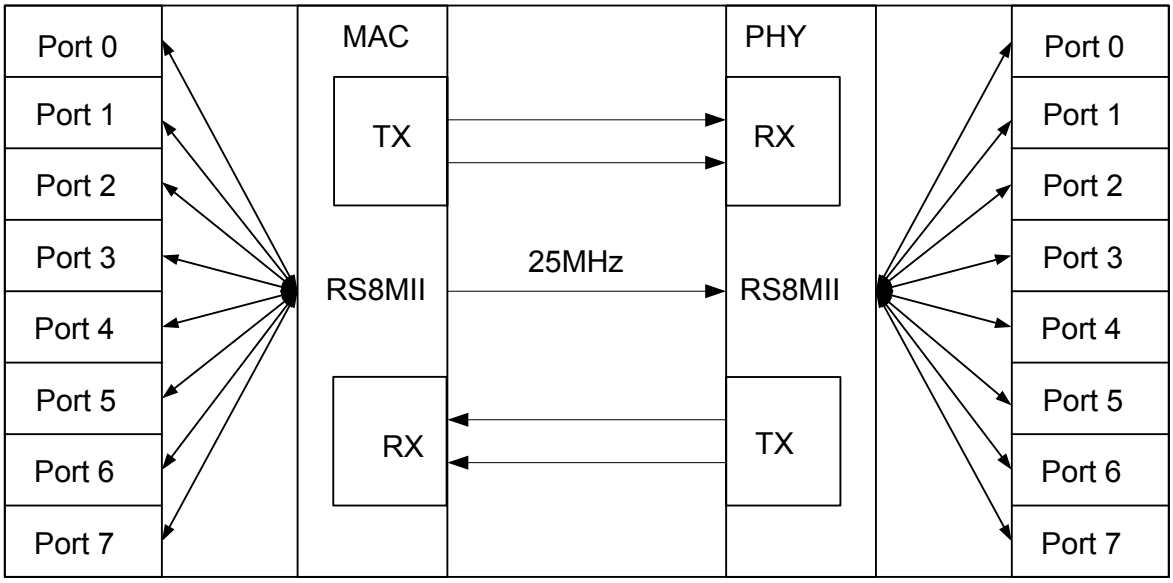


Figure 11. XSMII Interconnection

9.2. I2C-Like LED

The RTL8316E/RTL8324E supports I2C-like LED by connecting with an LED of the RTL8231, which provides single-color and Bi-color scan LED and extended GPIOs.

When powered on or hardware reset, the RTL8316E/RTL8324E initializes the RTL8231, and then writes the LED status to it to turn on/off LEDs. The external CPU can also access the RTL8231 to extend GPIOs via indirect mode.

9.3. Serial LED Connection

The RTL8316E/RTL8324E has 16/24 MAC ports and supports a serial LED interface to display the link status. The serial LED interface, LED_SCK and LED_DATA provide clock and data to enable/disable the external shift registers. A 74HC164 8-Bit Serial-In, Parallel-Out Shift Register captures the per-port link status and diagnostic information.

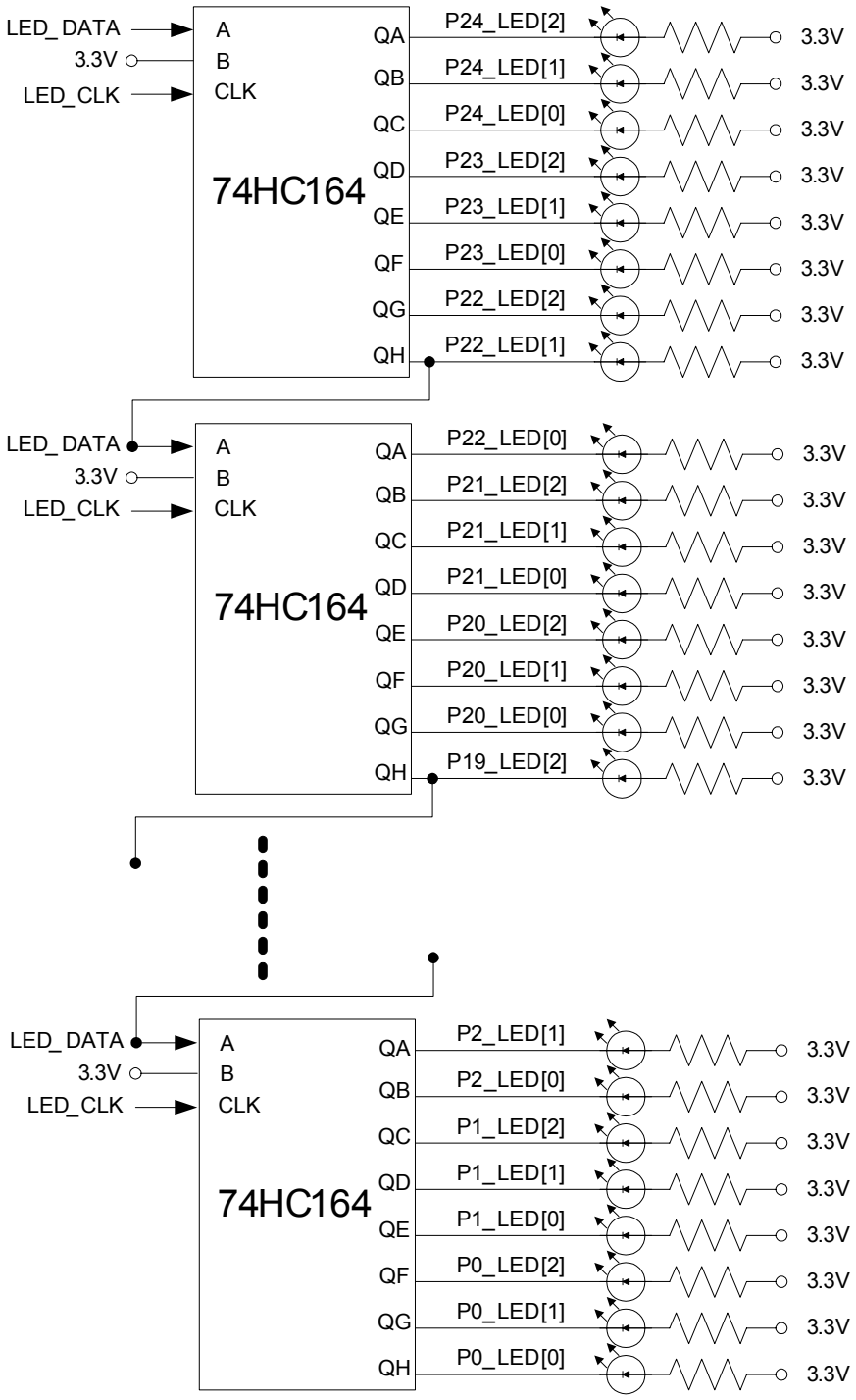


Figure 12. Serial LED Connection

9.4. Scan LED for RTL8316E (Not Supported in the RTL8324E)

In order to reduce the external LED circuits, the RTL8316E supports scan LED mode. It covers 16 port's link status with two LEDs, and provides six scan pins and six status pins to display the link status.

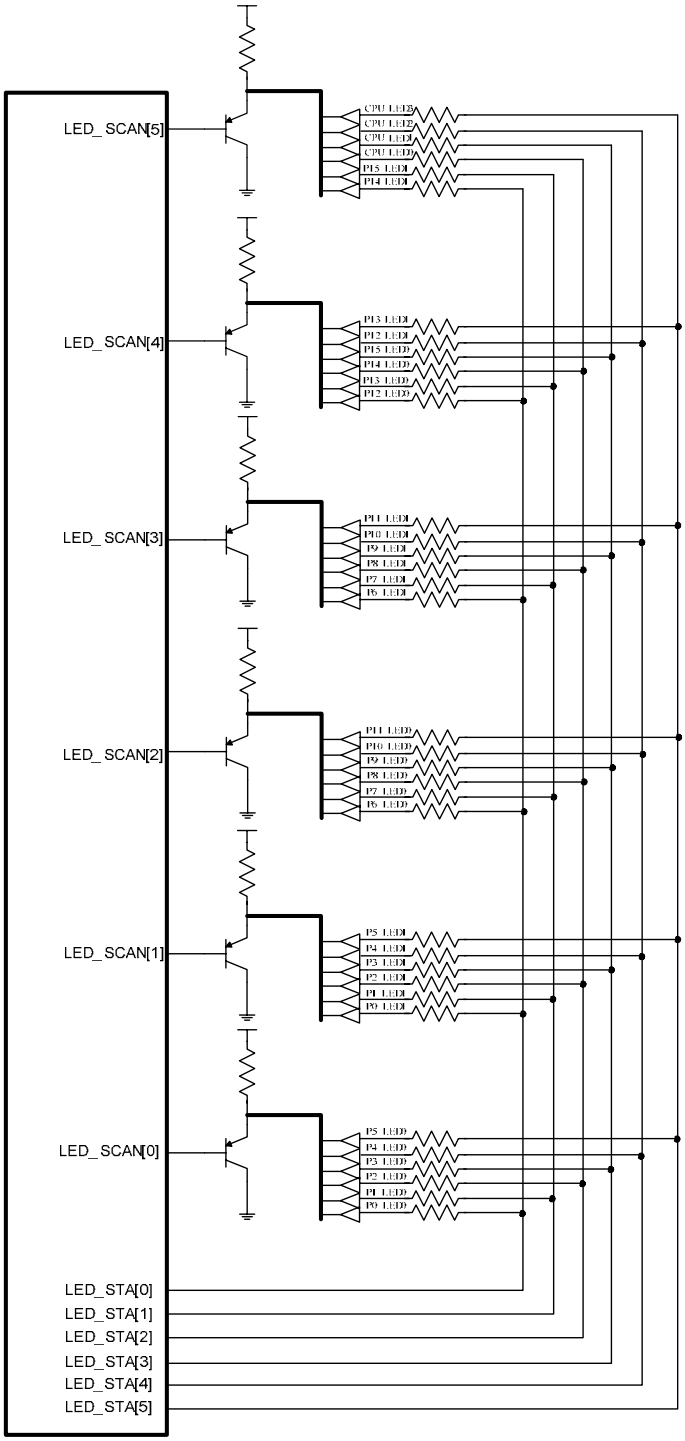


Figure 13. Scan LED Mode Connection

9.5. I2C Master for EEPROM

The EEPROM can be divided into two sizes: 2Kb~8Kb and 32Kb~512Kb. The address of the small size EEPROM is 8-bits, however the larger EEPROM has word-high addressing and word-low addressing, and it is 16-bits (two bytes).

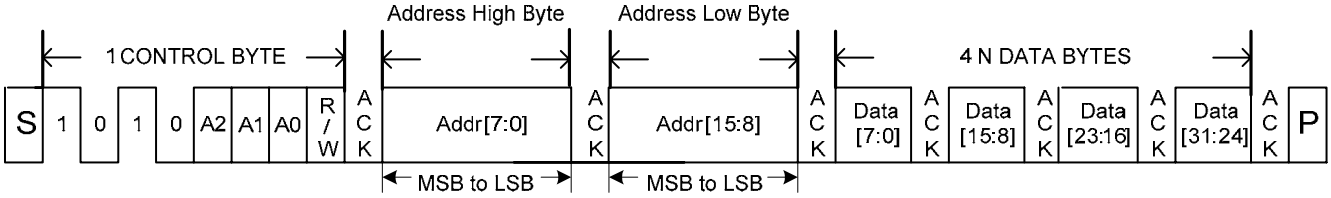


Figure 14. Large Size (32Kb~512Kb) EEPROM Read/Write Timing

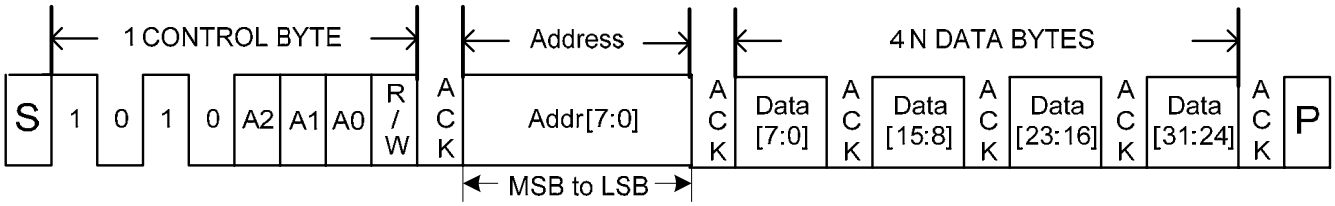


Figure 15. Small Size (4Kb~8Kb) EEPROM Read/Write Timing

9.6. Serial CPU Interface

The RTL8316E/RTL8324E supports a serial CPU interface (Slave mode) to access the internal register. It has two I/O pins (i.e., SDA and SCL). SDA is the access data signal, and SCL is the clock signal (typical clock is 1~2MHz). The read/write data sequence is shown in Figure 16. It consists of a control byte (1 byte) + address bytes (2 bytes) + data bytes (4N pieces, N: integer, N≠0).

When the external CPU wants to read/write data to the RTL8316E/RTL8324E, it must set the read/write bit (read is 1, and write is 0).

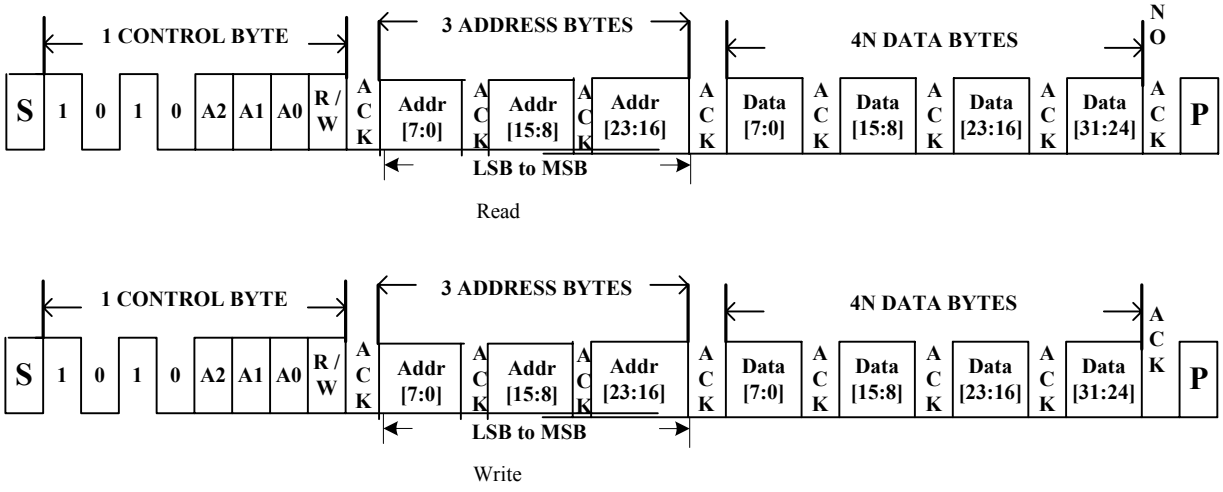


Figure 16. Serial CPU Interface Access Data Sequence

10. Electrical AC/DC Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 16. Absolute Maximum Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
DVDD33, AVDD33, AVDD33_XTAL Supply Referenced to GND	GND-0.3	+3.63	V
DVDD12, AVDD12, VDD12_PLL, SAVDD12 Supply Referenced to GND, GND_PLL, AVSS	GND-0.3	+1.32	V

10.2. Operating Range

Table 17. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
DVDD33, AVDD33, AVDD33_XTAL Supply Voltage Range	3.135	3.3	3.465	V
DVDD12, AVDD12, VDD12_PLL, SAVDD12 Supply Voltage Range	1.14	1.2	1.26	V

10.3. DC Characteristics

Table 18. DC Characteristics

Symbol	Parameter (VDDIO=3.3V)	Min	Typical	Max	Units
V_{IH}	TTL Input High Voltage	2.0	-	-	V
V_{IL}	TTL Input Low Voltage	-	-	0.8	V
V_{OH}	Output High Voltage	2.4	-	-	V
V_{OL}	Output Low Voltage	-	-	0.4	V

10.4. AC Characteristics

10.4.1. XSMII Transmitter Signal Electrical Characteristics

Table 19. XSMII Transmitter Signal Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Units
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.35	0.4	0.8	V
C_{TX}	AC Coupling Capacitor	75	100	200	nF
L_{TX}	Transmit Length in PCB	-	-	5	Inch

10.4.2. XSMII Receiver Signal Electrical Characteristics

Table 20. XSMII Receiver Signal Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Units
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Input Voltage	0.3	-	1.0	V
C_{RX}	AC Coupling Capacitor	75	100	200	nF

10.4.3. Serial LED Signal Timing

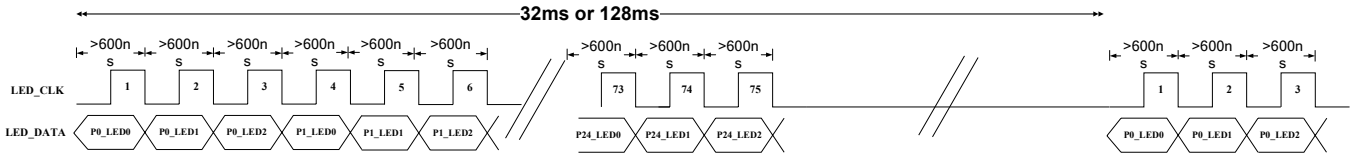


Figure 17. Serial LED Signal Timing

10.4.4. Scan LED Mode Signal Timing (RTL8316E)

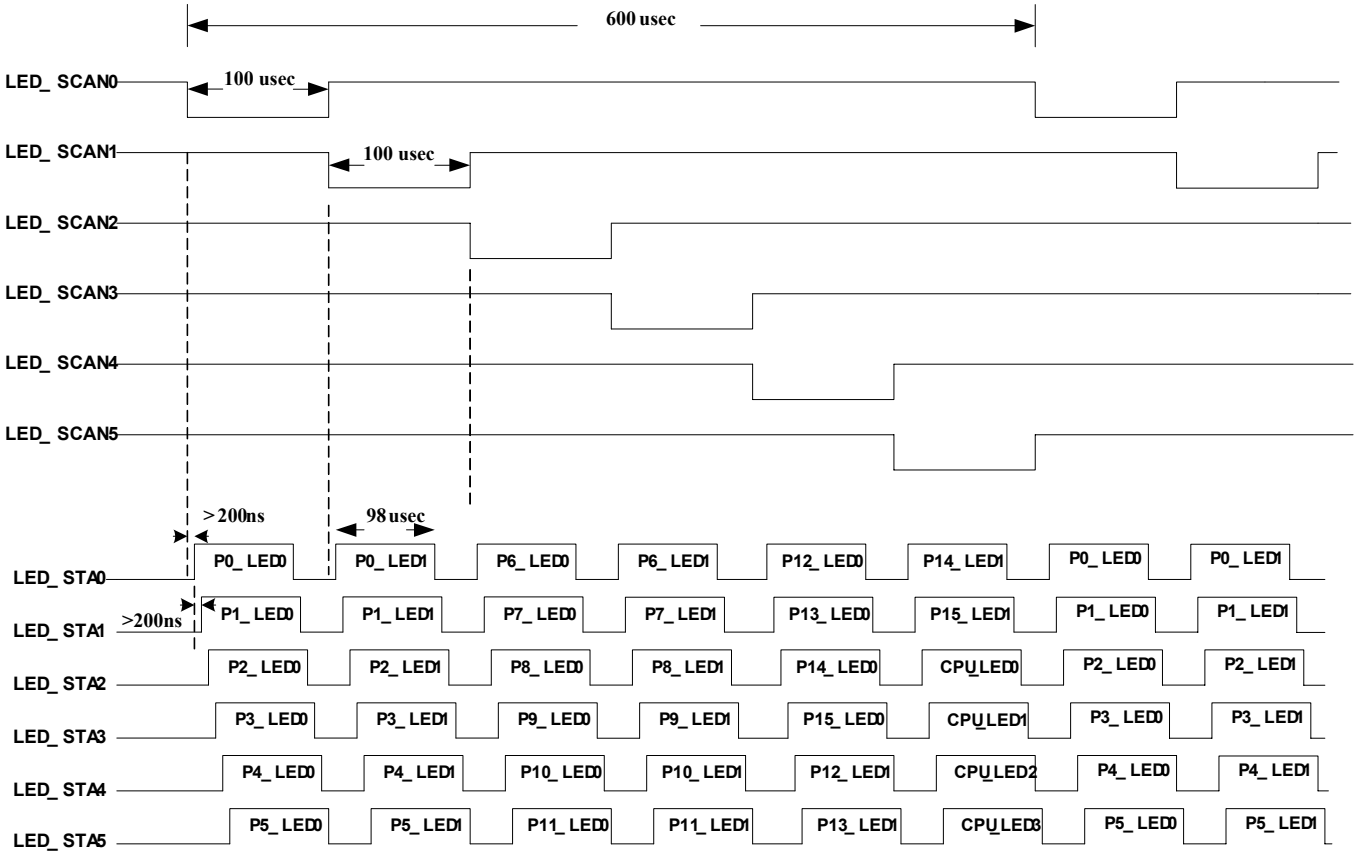


Figure 18. Scan LED Mode Signal Timing (RTL8316E)

10.4.5. I2C Master for EEPROM Timing

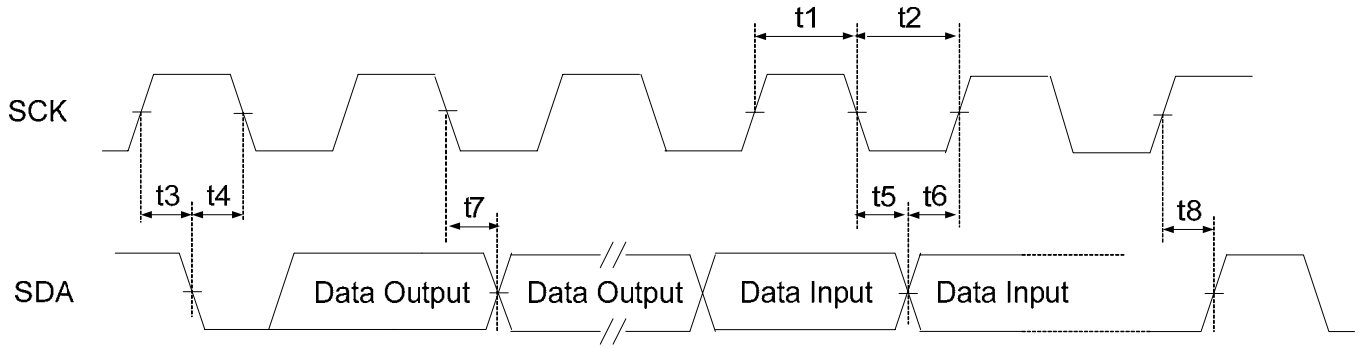


Figure 19. I2C Master Mode Timing

10.4.6. SCK/SDA Power on Timing

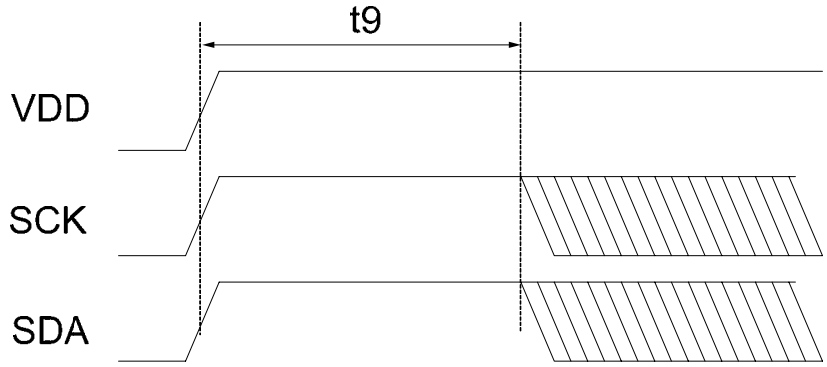


Figure 20. SCK/SDA Power on Timing

10.4.7. EEPROM Auto-Load Timing

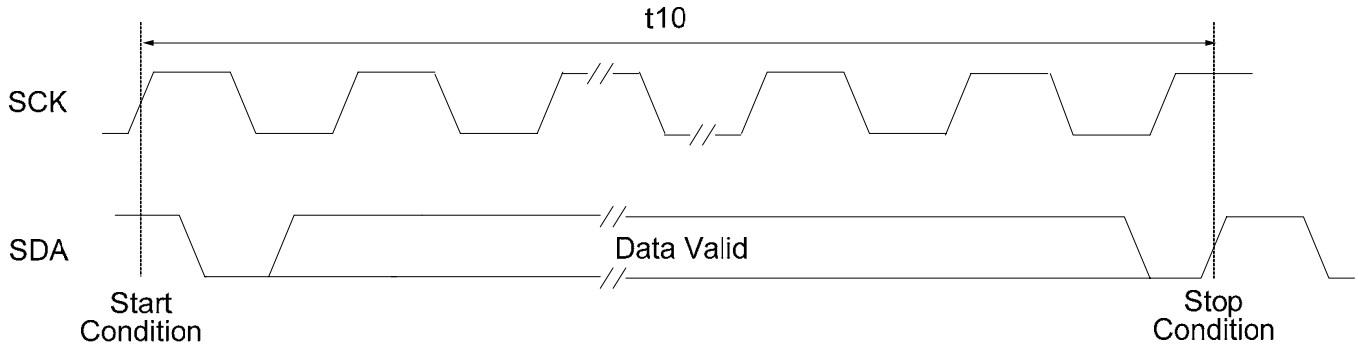


Figure 21. EEPROM Auto-Load Timing

10.4.8. I2C Master Mode Timing Characteristics

Table 21. I2C Master Mode Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
t1	SCK High Time	4.9	5	-	µs
t2	SCK Low Time	4.9	5	-	µs
t3	START Condition Setup Time	4.9	5	-	µs
t4	START Condition Hold Time	4.9	5	-	µs
t5	Data In Hold Time	0	-	-	µs
t6	Data In Setup Time	250	-	-	ns
t7	Data Output Hold Time	2.4	2.5	2.6	
t8	STOP Condition Setup Time	4.9	5	-	µs
t9	SCK/SDA Active From Power On	97	100	185	ms
t10	EEPROM Auto-Load Time (8K bit)	97	100	185	ms

10.4.9. Serial CPU Interface Timing

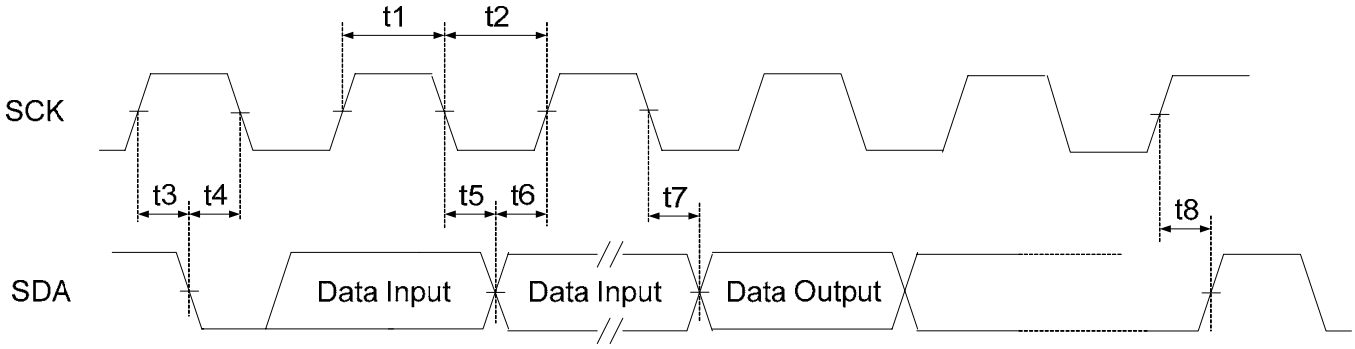


Figure 22. Serial CPU Interface Timing

10.4.10. Serial CPU Interface Timing Characteristics

Table 22. Serial CPU Interface Timing Characteristics

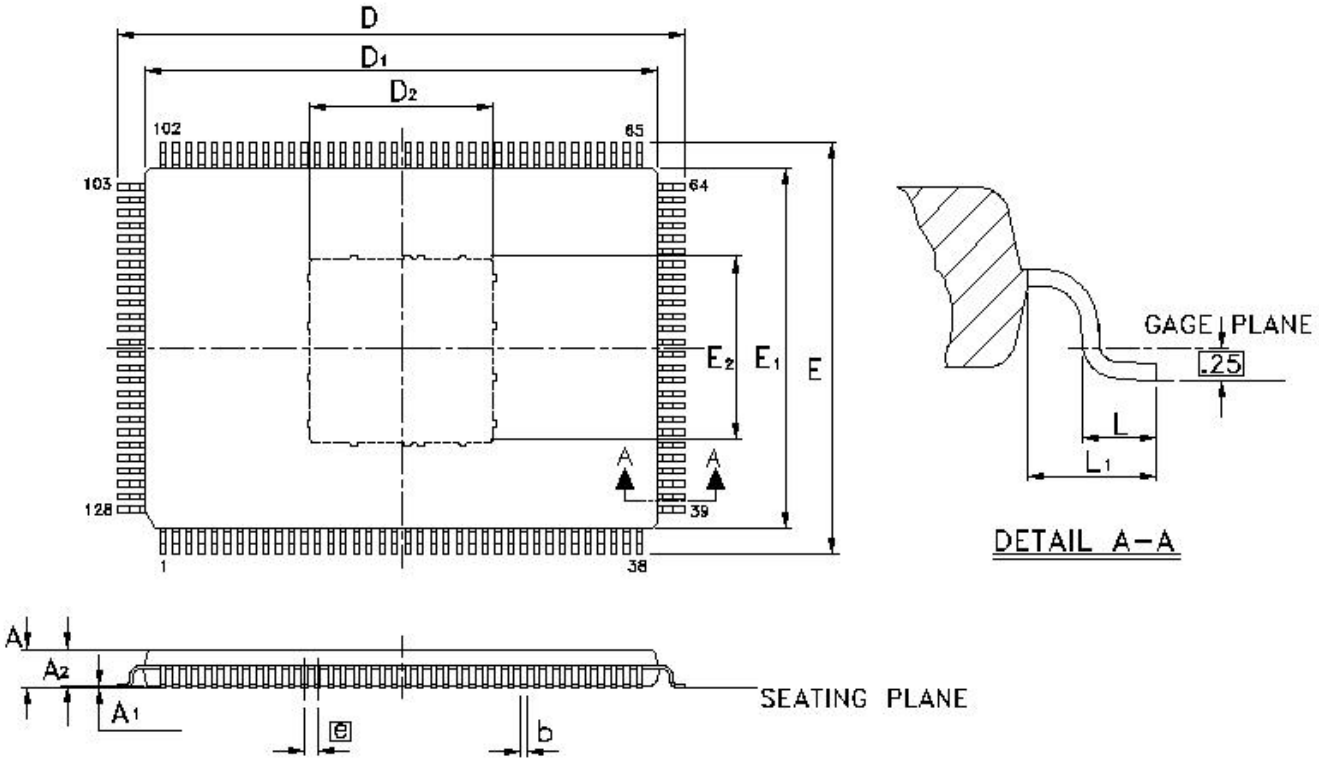
Symbol	Description	Min	Typical	Max	Units
t1	SCK High Time	4.0	-	-	µs
t2	SCK Low Time	4.0	-	-	µs
t3	START Condition Setup Time	4.0	-	-	µs
t4	START Condition Hold Time	4.0	-	-	µs
t5	Data Hold Time	0	-	-	µs
t6	Data Setup Time	250	-	-	ns
t7	Clock to Data Output Delay	-	9	-	ns
t8	STOP Condition Setup Time	4.0	-	-	µs

10.5. SMI Timing Characteristics (RTL8324E Only)

Table 23. SMI Timing Characteristics (RTL8324E Only)

Symbol	Parameter	Min	Typical	Max	Units
MDC	MDC Clock Rate	-	548	-	ns
MDIO Setup Time	Write Cycle	10	-	-	ns
MDIO Hold Time	Write Cycle	10	-	-	ns

11. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.2	0.27	0.007	0.009	0.011
D	22.00BSC			0.866BSC		
D_1	20.00BSC			0.787BSC		
D_2 / E_2	5.60	6.85	7.50	0.220	0.270	0.295
E	16.00BSC			0.630BSC		
E_1	14.00BSC			0.551BSC		
e	0.50BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes:

1. CONTROLLING DIMENSION: MILLIMETER (mm).
2. REFERENCE DOCUMENT: JEDEC MS-26.

12. Ordering Information

Table 24. Ordering Information

Part Number	Package	Status
RTL8316E-CG	LQFP 128-Pin E-PAD 'Green' Package	Production
RTL8324E-CG	LQFP 128-Pin E-PAD 'Green' Package	Production

Note: See page 7 (RTL8316E-CG) and page 14 (RTL8324E-CG) for package identification.

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