High-Side Power Distribution Controller

Features

- **High-Side Driver for an External N-Channel MOSFET**
- **Under-Voltage Lockout (UVLO)**
- **Wrong VIN Input Voltage Protection**
- **Output Under-Voltage Protection (UVP)**
- **Short-Circuit Protection During Power-up (SCP)**
- **Over-Current Protection (OCP)**
- **Selectable VIN Monitor Voltage**
- **Shutdown Function**
- **Power Okay (POK) Function**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

APL3542A is a high-side power distribution controller for an external N-channel MOSFET, allow for +12V, +19V or +5V power-supply rail. The wrong input voltage protection function protects a wrong input adapter insertion, when input voltage is out of the target input voltage range the IC is off.

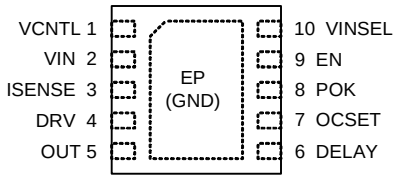
The over-current protection monitors the output current by using the voltage drop across the external sensing resistor, when output current reaches the trip point the IC will be shut down. The APL3542A also provides a short-circuit protection during power-up. The device monitors VOUT voltages for a short-circuit detection, if a short-circuit condition is detected the IC will be shut down.

Other features include a POK output to indicate the output voltage is ready, and a logic-controlled shutdown mode.

Applications

- **AIO Computers**
- **Notebooks**

Pin Configuration



TDFN3x3-10
(Top View)

=Exposed Pad. Power's and signal's return path. Connect this pad to large copper area for better heat dissipation.

Ordering and Marking Information

APL3542A □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN 3x3-10 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3542A QB : APL 3542A XXXXX	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN} V_{VCNTL}	VIN, VCNTL Input Voltage (VIN to GND)	-0.3 to 40	V
V_{OUT}, V_{DRV}, V_{VINSEL}	VOUT, DRV, and VINSEL to GND Voltage	-0.3 to 40	V
V_{EN}, V_{POK}, , V_{OCSET}, V_{DELAY}	EN, POK, OCSET, DELAY to GND Voltage	-0.3 to 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air	60	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN} V_{VCNTL}	VIN, VCNTL Input Voltage (VIN to GND)	5 to 26	V
V_{OUT}, V_{VINSEL}	VOUT, and VINSEL to GND Voltage	0 to 26	V
V_{EN}, V_{POK}, , V_{OCSET}, V_{DELAY}	EN, POK, OCSET, DELAY to GND Voltage	0 to 5	V
R_{OCSET}	OCSET Pull Low Resistance	2 to 30	kΩ
T_A	Ambient Temperature	-40 to 85	°C
T_J	Junction Temperature	-40 to 125	°C

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=19V, V_{EN} =5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3542A			Unit
			Min	Typ	Max	
UNDER-VOLTAGE LOCKOUT (UVLO) AND SUPPLY CURRENT						
V_{UVLO}	VCNTL UVLO Threshold Voltage	V_{CNTL} rising, T_A= 25 °C	4.0	4.3	4.5	V
	VCNTL UVLO Hysteresis		-	0.3	-	V
$T_{D(ON)}$	Power-On Delay Time	V_{CNTL} >V_{UVLO}, V_{EN}=5V, and $V_{VINSEL(H)}$>V_{VINSEL}> $V_{VINSEL(L)}$	-	30	-	ms
I_{VICNTL}	VCNTL Supply Current	No load, V_{EN} =5V,	-	500	750	µA
		No load, V_{EN} =0V	-	20	40	µA
WRONG VIN INPUT VOLTAGE PROTECTION						
$V_{VINSEL(L)}$	VINSEL Low Detection Rising Threshold	V_{INSEL} rising, IC is on, V_{IN}=5V to 26V	0.625	0.650	0.665	V
	VINSEL Low Detection Falling Threshold	V_{INSEL} falling, IC is off, V_{IN}=5V to 26V	0.575	0.600	0.615	V
$V_{VINSEL(H)}$	VINSEL High Detection Rsing Threshold	V_{INSEL} rising, IC is off, V_{IN}=5V to 26V	2.145	2.200	2.232	V
	VINSEL High Detection Falling Threshold	V_{INSEL} falling, IC is on, V_{IN}=5V to 26V	2.048	2.100	2.132	mV
	VINSEL Input Current	V_{VINSEL}=40V	-	-	1	µA
	VINSEL Voltage Detection Disable Threshold	By pulling VINSEL low to disable VINSEL voltage detection, V_{IN}=5V to 21V	-	-	0.3	V
GATE DRIVER						
$V_{DRV-OUT}$	DRV to VOUT Voltage	V_{DRV}-V_{OUT}	-	5	-	V
	DRV Source Current	V_{DRV}=10V, V_{DRV}-V_{OUT}=2.5V	-	450	-	µA
	DRV Discharge Resistance	Any fault condition and shutdown (connected from DRV to VOUT)	-	50	-	Ω
PROTECTIONS						
	Under-Voltage Protection Threshold	V_{OUT} falling, V_{OUT}/V_{IN} (UVP is enabled after POK asserted high)	80	85	90	%
	Under-Voltage Protection Debounce		-	1	-	ms
I_{OCP}	OCP Threshold	I_{OCP}=1000/R_{OCSET}/R_{SENSE} (please see Function Description)	-	-	-	

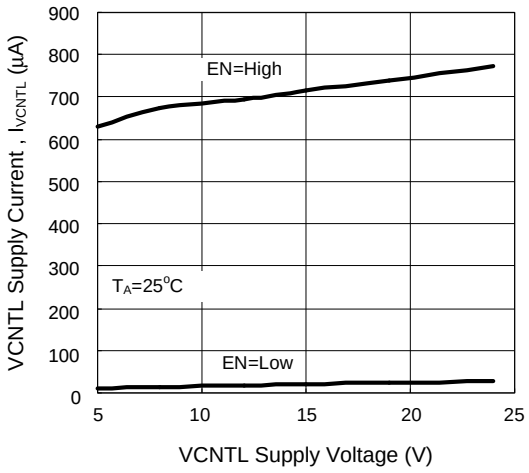
Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=19V, V_{EN} =5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

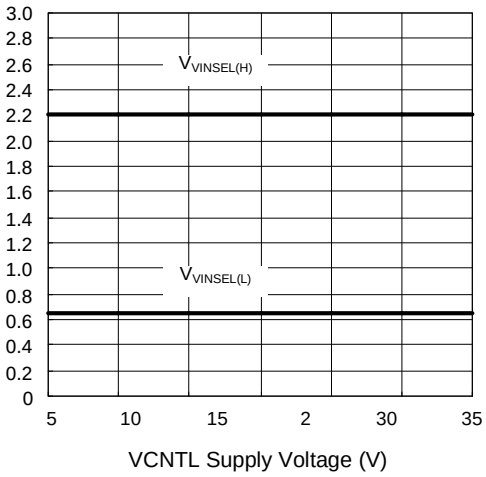
Symbol	Parameter	Test Conditions	APL3542A			Unit
			Min	Typ	Max	
PROTECTIONS						
V_{OCP}	OCP Offset Target Tolerance	VIN=19V, R_{OCSET}=2kΩ~30kΩ, OCP offset Target=1000/R_{OCSET} (assuming ROCSET tolerance is 0%) (OCP is tripped when the difference voltage V_{VIN} - V_{ISENSE} is equal to OCP Offset Target)	-20	-	20	%
T_{OCP}	OCP Debounce Time		-	10	-	ms
	OCP No Debounce Threshold		-	1.5*I_{OCP}	-	
	VOUT Input Current	V_{OUT}=19V	-	60	80	μA
	VOUT Discharge Resistance	Discharge during any fault condition or shutdown	-	50	-	Ω
	Over Temperature Protection		-	135	-	°C
	Over Temperature Protection Hysteresis		-	50	-	°C
EN Input						
	EN Logic Input Threshold		0.9	1.25	1.6	V
	EN Input Logic Hyteresis		-	0.2	-	V
	EN Pull-up Current		-	4	-	μA
POK Output						
V_{POK_TH}	POK Threshold	V_{OUT} rising, V_{IN}-V_{OUT}, V_{POK}=High	-	90	-	V
	POK Threshold Hysteresys	V_{OUT} falling from normal, V_{POK}=Low	-	5	-	%
	POK Low Voltage	I_{POK}=10mA	-	-	0.5	V
	POK Leakage Current	V_{POK}=40V	-	-	1	μA
$T_{D(POK)}$	POK Rising Delay Time	V_{OUT} rising, POK assertion	7	10	13	ms
Pre-Charge						
	Pre-charge Current	V_{IN}-V_{OUT}>1V	-	100	-	mA
	Pre-charge Reset Time	From the occurrence of SCP to the next pre-charge start	-	30	-	ms
	Pre-charge Re-try Times during Short-Circuit		-	4	-	time
	DELAY Source Current		-	2.4	-	μA
	DELAY pin Pre-SCP Threshold		-	1.8	-	V

Typical Operating Characteristics

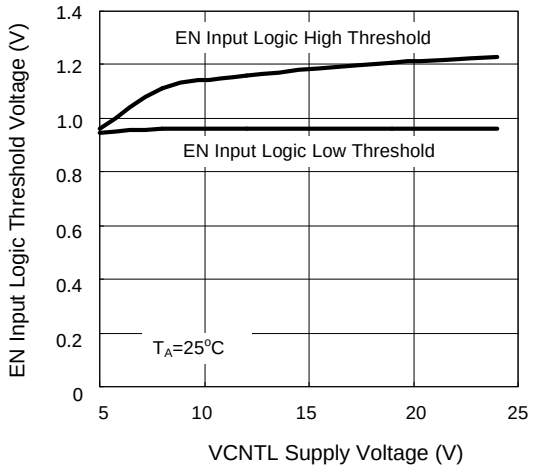
VCNTL Supply current vs. VCNTL Supply Voltage



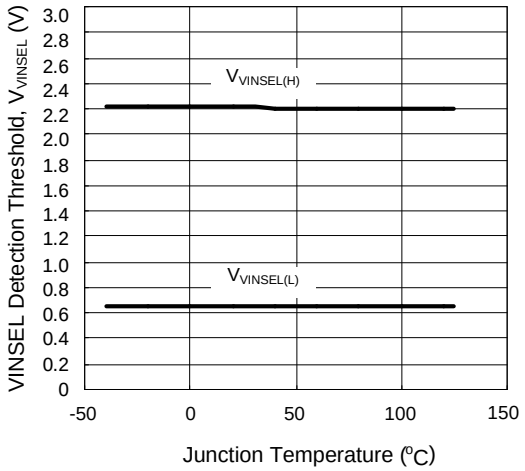
VINSEL Detection Threshold Voltage vs. VCNTL Supply Voltage



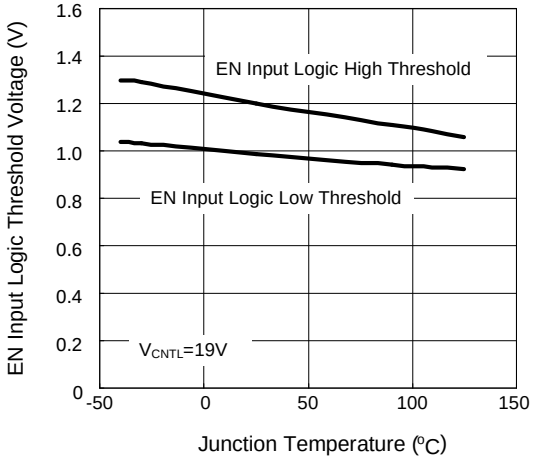
EN Logic Threshold Voltage vs. VCNTL Supply Voltage



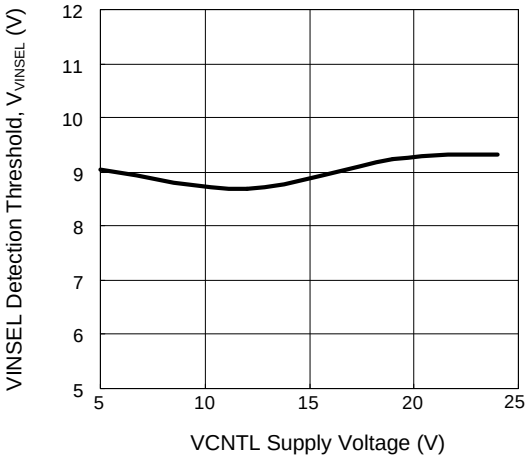
VINSEL Detection Threshold Voltage vs. Junction Temperature



EN Input Logic Threshold Voltage vs. Junction Temperature

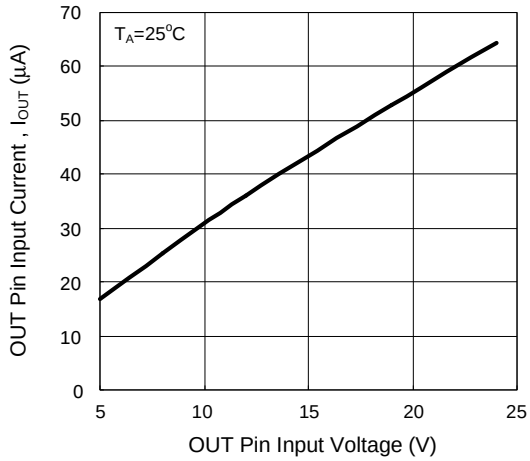


POK Rising Delay Time vs. VCNTL Supply Voltage

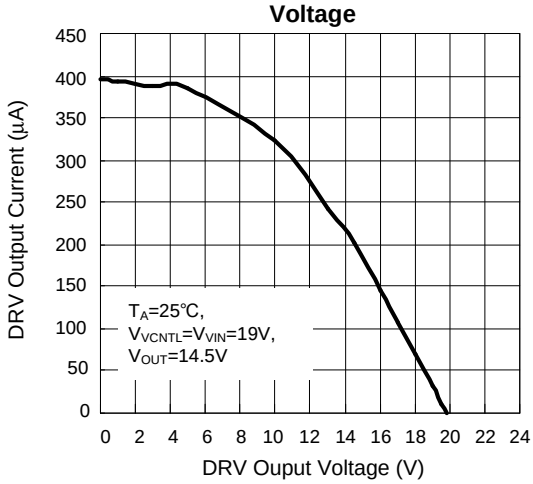


Typical Operating Characteristics

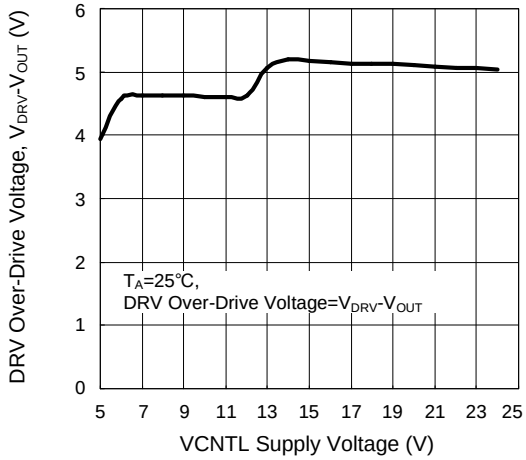
OUT Pin Input Current vs. OUT Input Voltage



DRV Output Current vs. DRV Output Voltage



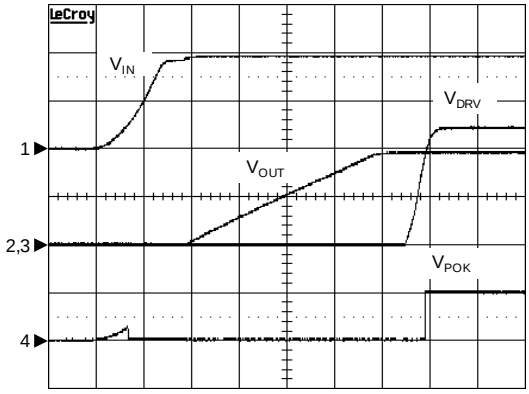
DRV Over-Drive Voltage vs. VCNTL Supply Voltage



Operating Waveforms

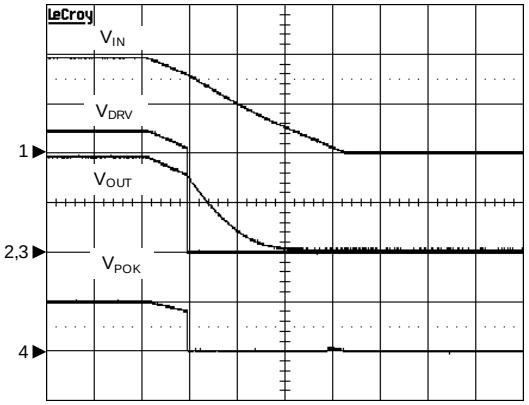
The test condition is T_A= 25°C unless otherwise specified.

Power On with POK Pulled High



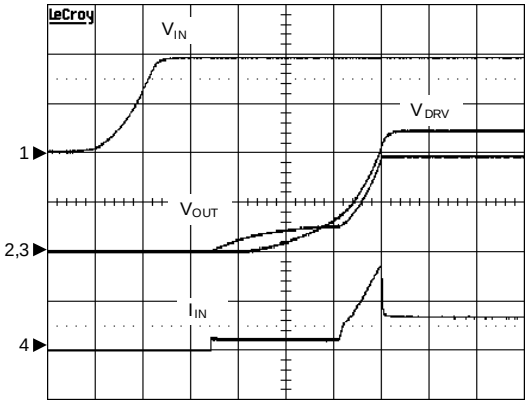
V_{IN} =19V, C_{DRV}=220nF, C_{OUT}=470µF, no load, EN open, POK tied to VIN via 100kΩ/36kΩ, VINSEL tied to VIN via 24kΩ/2kΩ.
CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: V_{DRV}, 10V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 20ms/Div

Power Off with POK Pulled High



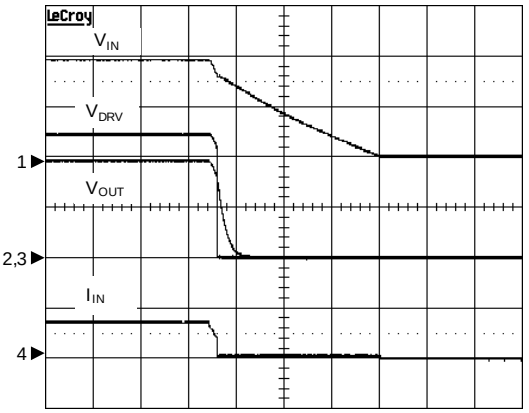
V_{IN} =19V, C_{DRV}=220nF, C_{OUT}=470µF, no load, EN open, POK tied to VIN via 100kΩ/36kΩ, VINSEL tied to VIN via 24kΩ/2kΩ.
CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: V_{DRV}, 10V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 100ms/Div

Power On with POK Open



V_{IN} =19V, C_{DRV}=220nF, C_{OUT}=470µF, no load, EN open, POK open, VINSEL tied to VIN via 24kΩ/2kΩ.
CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: V_{DRV}, 10V/Div, DC
CH4: I_{IN}, 0.5A/Div, DC
TIME: 20ms/Div

Power Off with POK Open

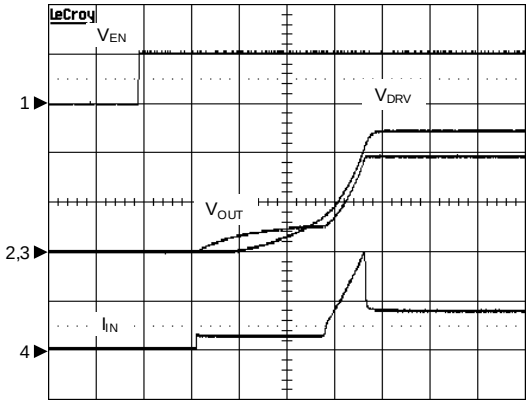


V_{IN} =19V, C_{DRV}=220nF, C_{OUT}=470µF, no load, EN open, POK open, VINSEL tied to VIN via 24kΩ/2kΩ.
CH1: V_{EN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: I_{IN}, 0.5A/Div, DC
TIME: 100ms/Div

Operating Waveforms

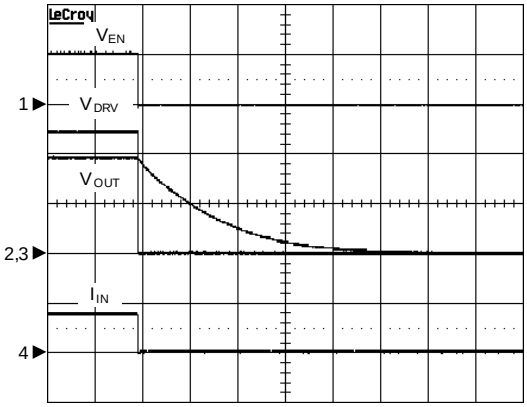
The test condition is T_A= 25°C unless otherwise specified.

Enable



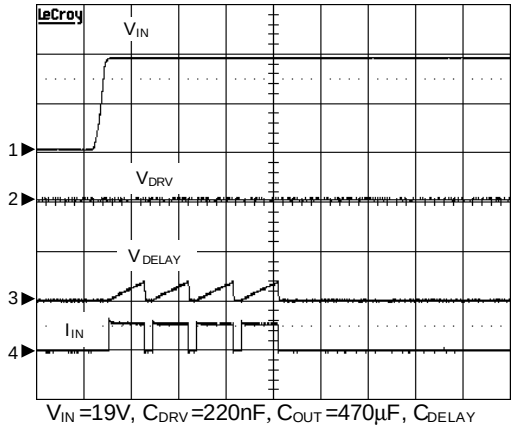
V_{IN} =19V, C_{DRV}=220nF, C_{OUT} =470µF, R_{LOAD}=47Ω, POK pin open,
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: V_{DRV}, 10V/Div, DC
CH4: I_{IN}, 0.5A/Div, DC
TIME: 20mA/Div

Disable



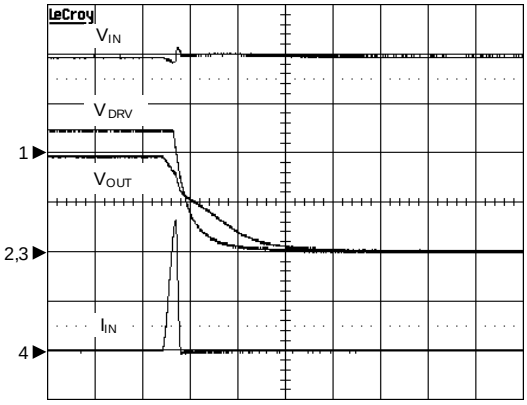
V_{IN} =19V, C_{DRV}=220nF, C_{OUT} =470µF, R_{LOAD}=47Ω, POK pin open,
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: V_{DRV}, 10V/Div, DC
CH4: I_{IN}, 0.5A/Div, DC
TIME: 10mA/Div

Short-Circuit Before Power On



V_{IN} =19V, C_{DRV}=220nF, C_{OUT} =470µF, C_{DELAY} =0.1µF, EN pin open, POK pin open, Output shorted to ground then VIN power on
CH1: V_{IN}, 10V/Div, DC
CH2: V_{DRV}, 2V/Div, DC
CH3: V_{DELAY}, 5V/Div, DC
CH4: I_{IN}, 200mA/Div, DC
TIME: 100ms/Div

Short Circuit After Power On

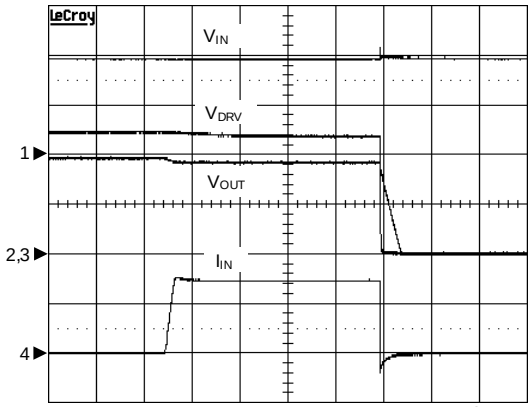


V_{IN} =19V, C_{DRV}=220nF, C_{OUT} =470µF, EN pin open, POK pin open, R_S=25mΩ, R_{OCSET}=5kΩ, Output shorted to ground
CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: V_{DRV}, 10V/Div, DC
CH4: I_{IN}, 10A/Div, DC
TIME: 50µA/Div

Operating Waveforms (Cont.)

The test condition is T_A= 25°C unless otherwise specified.

OCP and Its Debounce Time

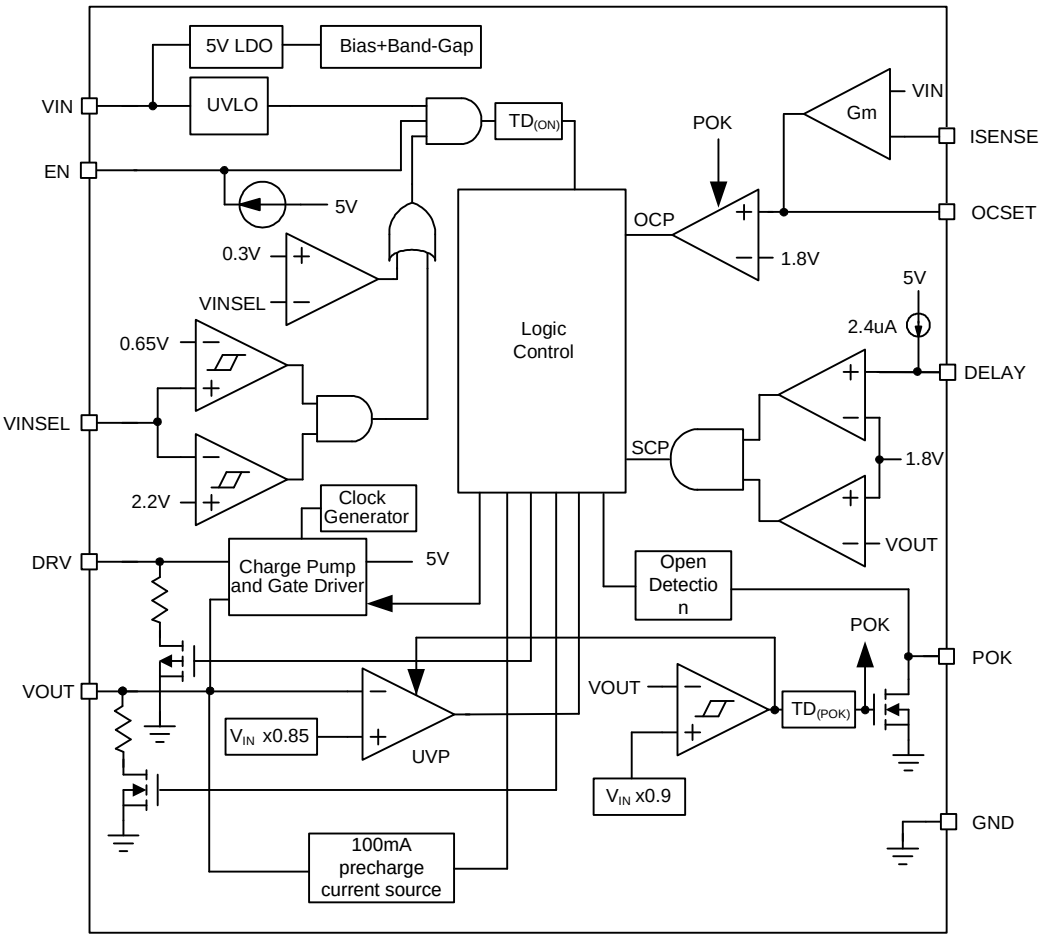


V_{IN}=19V, C_{DRV} =220nF, C_{OUT} =470µF, EN pin open, POK pin open, R_S=25mΩ, R_{OCSET}=5kΩ, ILOAD=8A
CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 10V/Div, DC
CH3: V_{DRV}, 10V/Div, DC
CH4: I_{IN}, 5A/Div, DC
TIME: 2ms/Div

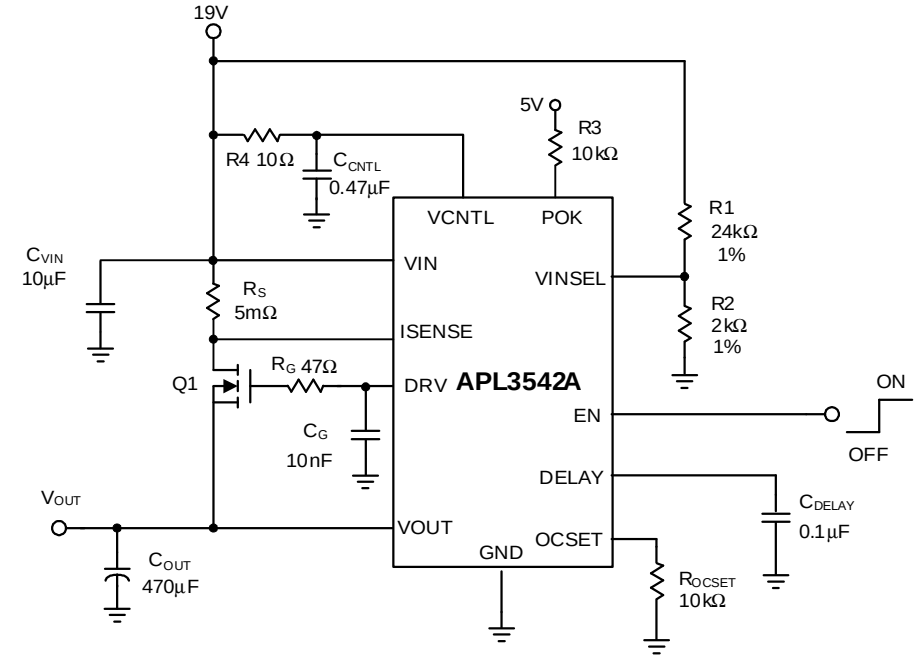
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VCNTL	Supply Voltage for internal circuits.
2	VIN	Provide power to the internal 100mA current source and gate driver.
3	ISENSE	This pin is used to sample the voltage drop between VIN and ISENSE for sensing load current.
4	DRV	Gate Driver Output. The gate driver for the external N-channel MOSFET.
5	VOUT	Output Voltage Sense Pin. Connect this pin to the source of external N-channel MOSFET to monitor the output voltage.
6	DELAY	Connecting a capacitor from this pin to ground sets the delay time which determines when SCP protection is activated.
7	OCSET	Over-Current Trip Point Adjustment Pin. A resistor (R_{OCSET}) from this pin to ground sets the OCP threshold.
8	POK	Power Okay Indicator Output. The POK is an open-drain pull-down device. When VOUT voltage is below the POK threshold, the POK output is pulled low; when VOUT voltage is above the POK threshold, the POK output is in high impedance.
9	EN	Enable Input. Pulling the V_{EN} above 2V will enable the IC; pulling V_{EN} below 0.6V will disable the IC. This pin is pulled high by an internal current source.
10	VINSEL	Input Voltage Sense Pin. Connect a resistive divider from VIN to VINSEL to GND to monitor the input voltage. Pulling V_{VINSEL} below 0.3V will disable this function.

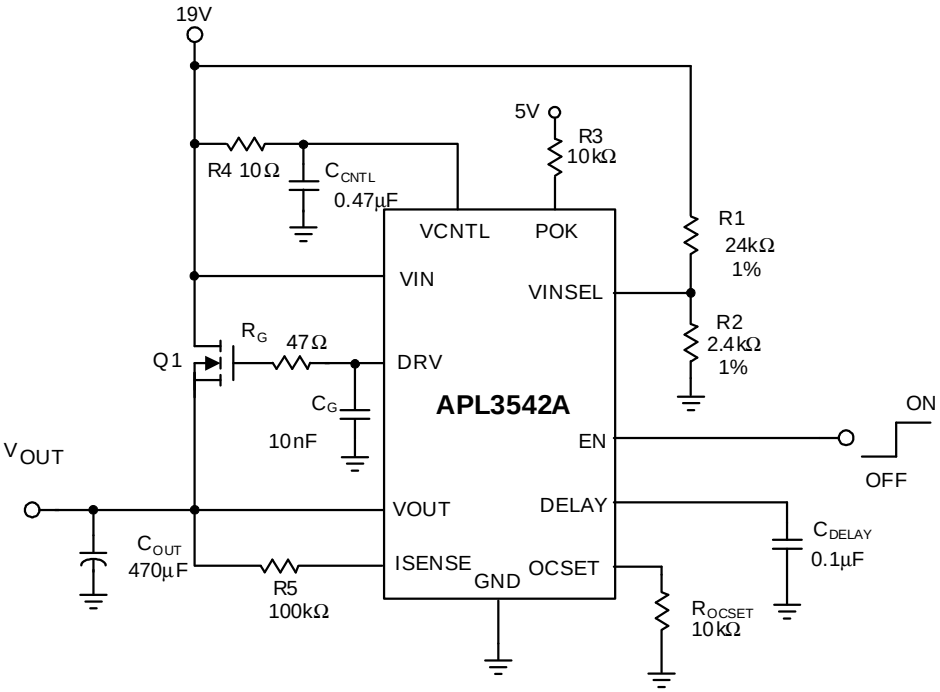
Block Diagram



Typical Application Circuit



Use R_S resistor to sense output current



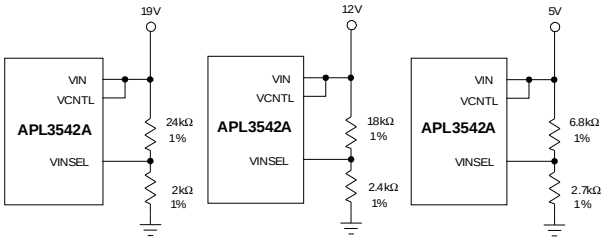
Use MOSFET's on-resistance to sense output current

Function Description

Wrong VIN Input Voltage Protection

The APL3542A provides an input voltage detection function to protect a wrong input adapter insertion by using VINSEL pin. Connect a resistive divider from VIN to VINSEL to GND to set the target input voltage. The VINSEL pin acquires the input voltage information from the divider. When the V_{VINSEL} is out of the range of $V_{VINSEL(L)}$ ~ $V_{VINSEL(H)}$, the APL3542A enters disable mode and shuts off DRV output. While the $V_{VINSEL(L)}$ is 0.65V and $V_{VINSEL(H)}$ is 2.2V typically, the VINSEL input voltage set by the external resistive divider is recommend at around1.425V. Below diagrams are some examples according to different VIN input voltage, for your reference.

For accurate setting, using high accurate resistors is recommended.



Power-Up

The APL3542A has a built-in under-voltage lockout circuitry to keep the DRV output shut off until internal circuitry is operating properly. The UVLO circuit has a hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold and after 10ms delay time.

Under-Voltage Protection (UVP)

The OUT pin monitors the output voltage. If the V_{OUT} is under 85% of VIN input voltage, because of the short circuit or other influences, it will cause the under voltage protection, and turn off IC, the V_{OUT} voltage is also discharged to GND by an internal resistor, requiring a VIN UVLO or EN re-enable again to restart IC. Note that the UVP is active after the power-up and POK is asserted.

Over-Current Protection (OCP)

The APL3542A provides OCP protection against over load or short circuit conditions after POK is asserted.

The OCP threshold can be adjusted by the resistor on OCSET pin, R_{OCSET}. When the load current flowing through the R_S (the sense resistor between VIN and ISENSE) or $R_{DS(ON)}$ (the on-resistance of external power MOSFET) exceeds the OCP threshold, I_{OCP}, the APL3542A will turn off its DRV by internal discharge circuit and latch whole chip in off state until EN or VCC is cycled. The I_{OCP} can be calculated according to R_{SENSE} and R_{OCSET} by the following equation:

$I_{OCP}(A)= 1000/ (R_S (m\Omega) x R_{OCSET}(k\Omega))$

-using R_S as current sensing

$I_{OCP}(A)= 1000/ (R_{DS(ON)} (m\Omega) x R_{OCSET}(k\Omega))$

-using $R_{DS(ON)}$ as current sensing

The OCP latch-off occurs when the load current exceeds I_{OCP} and period persists over OCP debounce time. This feature of debounce ignores transient current. When the load current exceeds 1.5 x I_{OCP}, the APL3542A latches off immediately.

Pre-SCP Protection

The APL3542A implements Pre-SCP function during power-on period by monitoring the voltage on both DELAY and OUT pins. If a short circuit is present before power on, the VOUT's voltage will be kept low and never reach 1.8V threshold while the DELAY's voltage will rise beyond 1.8V, the SCP will be engaged. The chip will latch off after 4 times of short circuit condition is detected, needing to toggle EN or VCC to release the latch off condition. Connecting a capacitor on DELAY pin can adjust the SCP timing, meaning that larger C_{DELAY} capacitor postpones the timing of SCP. If output soft start time is very long, the C_{DELAY} capacitor should be adjusted, accordingly. Approximately, the selection of C_{DELAY} should meet the following criterion to avoid wrongly SCP trigger: 42000 x C_{DELAY}>C_{OUT}

Function Description (Cont.)

Shutdown Control

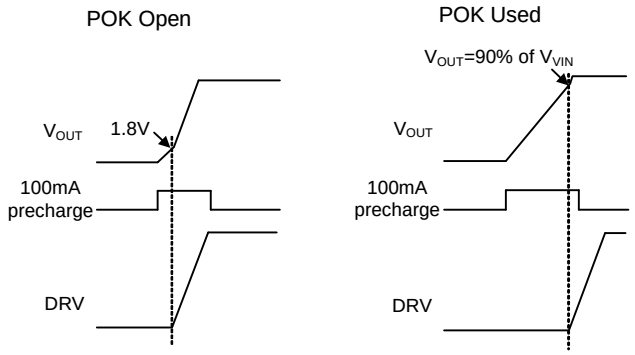
The APL3542A has an active-low shutdown function. Pulling the V_{EN} above 2V will enable the IC; pulling V_{EN} below 0.6V will disable the IC and the POK is pulled low immediately (ignore the $V_{POK(TH)}$ and $T_{D(POK)}$), the V_{OUT} voltage is also discharged to GND by an internal resistor . EN pin is pulled high by an internal current source and can be left floating.

POK Output and POK Open Detection

The power okay function monitors the output voltage and drives the POK low to indicate a fault. When a fault condition such as over-current, or under-voltage is occurred, and the V_{OUT} output voltage falls to 85% of VIN input voltage, the POK is pulled low. When the V_{OUT} output voltage reaches to 90% of V_{VIN}, and after 10ms delay time the POK is pulled high. Since the POK is an open-drain device, connecting a resistor to a pull high voltage is necessary.

POK Output and POK Open Detection(cont.)

If the POK is not used, it can be left open. We presume that the POK is a declaration of "power is ready" and used to allow system draws large current from V_{OUT}. Since the POK is opened, meaning that POK indication is not implemented by system designer, the larger power request shall come at any time. In POK open case, we advance the DRV timing to drive Q1 in case power request is around the corner. Please refer to the following timing diagram for both POK open and POK used conditions. If the POK is used, the range of POK externally pulled high resistor must be 2kΩ~200kΩ.



Application Information

Filtering of VIN and VCNTL

While hot plug-in an AC adapter, the inductive peak voltage seen in the VIN pin could be very high if there is no any filtering measure taken. It is recommended to place a 0.1 to 10μF ceramic bypass capacitor as close as possible to the VIN pin. An RC-filter on VCNTL pin, depicted in the application circuit, is preferable because better performance in filtering the peak voltage and noise. Note that the voltage rating of the input capacitor must be greater than the maximum V_{IN} voltage.

Gate and Output Capacitor

It is recommended to place a capacitor in the gate of external power MOSFET to control the soft-start rate of output voltage, especially when a high-value output capacitor is used. The gate capacitor can reduce the inrush current to the output capacitor during soft-start. If the power supply cannot support the inrush current, the C_{OUT} voltage will be clamped during soft-start and SCP will be falsely activated. The inrush current must be controlled within power supply current capability by using this gate capacitor. Note that the voltage rating of the gate capacitor must be greater than the maximum V_{DRV} voltage, where the V_{DRV} approximately equals V_{IN}+5V.

A bulk output capacitor, placed close to the load, is recommended to support load transient current. Precautions should be taken when a high-value output capacitor is used the gate capacitor C1 (shown in the application circuit) must be matched. A high-value output capacitor with a small-value C1 would probably lead to inrush current and end up SCP latched-off in the soft-start period. Please make sure that the gate capacitor C1 is matched with a high-value output capacitor. Note that the voltage rating of the output capacitor must be greater than the maximum V_{IN} voltage.

Gate Resistor

It is recommended to place a resistor R_G, as shown in the Typical Application Circuit, in the gate of external power MOSFET to prevent occurrence of oscillation during powering on. If the oscillation occurs, the SCP or VINSEL wrong voltage detection might be activated unexpectedly. The R_G literally could stabilize the external MOSFET to avoid oscillation. The R_G can be in the range of 10~100Ω. The recommended value is 47Ω.

Power MOSFETs

APL3542A requires an N-channel MOSFET that is utilized as an on/off switch. When a MOSEFT is selected, please make sure that the $R_{DS(ON)}$ of this MOSFET can meet your maximum voltage droop requirement in full load conditions. And also make sure that the MOSFET you select can satisfy the current delivering requirement, described in the paragraph of Short-Circuit Protection in Function Description. Another important criterion for selection of MOSFET is the MOSFET must be operated within its safe operation area in your application. The package type of the MOSFET must be chosen for efficient heat removal. Note that the V_{DS} rating of the MOSFET you selected must be greater than the V_{IN} voltage and the V_{GS} rating must be greater than 5V. The power dissipated in the MOSFET while on is shown in the following equation:

$$P_D = I_O^2 \times R_{DS(on)}$$

Select a package type and heatsink that maintains the junction temperature below the rating.

Layout Consideration

Figure 1 illustrates the layout, with bold lines indicating high current paths; and these traces must be short and wide. The layout guidelines are listed as below.

1. Place the input capacitors C_{IN} for VIN near pin as close as possible.
2. The trace from DRV to the gate of power MOSFETs should be wide and short.
3. Place output capacitor C_{OUT} near the load as close as possible.
4. Large current paths must have wide and thick traces, depicted as the bold lines.
5. The drain of the power MOSFETs should be a large plane for heatsinking.

Application Information (Cont.)

Layout Consideration (Cont.)

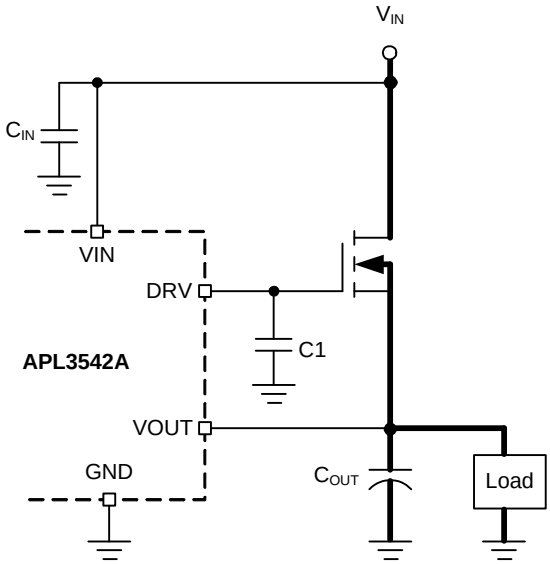
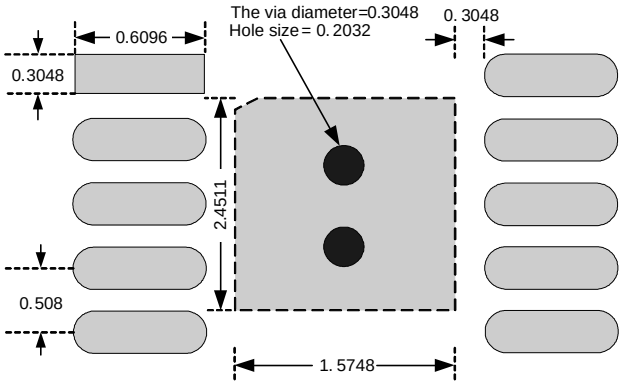


Figure 1. Layout Guidelines

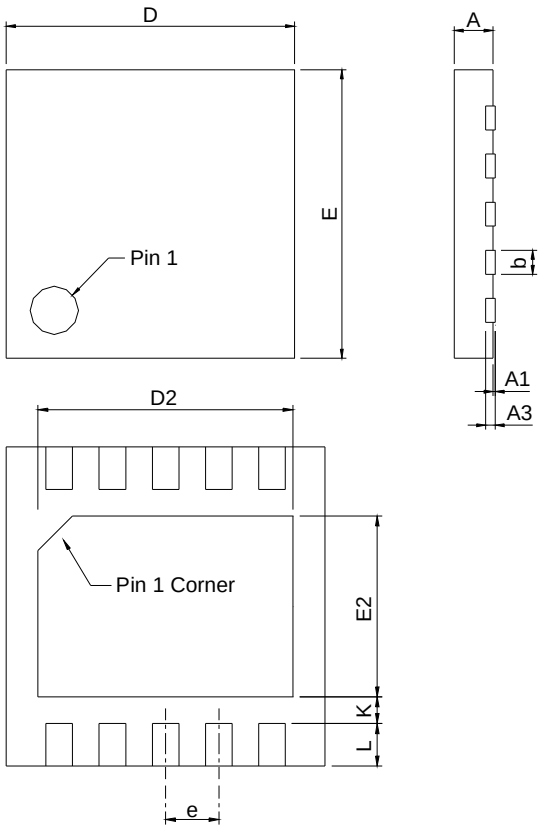
Recommended Minimum Footprint



TDFN3x3-10

Package Information

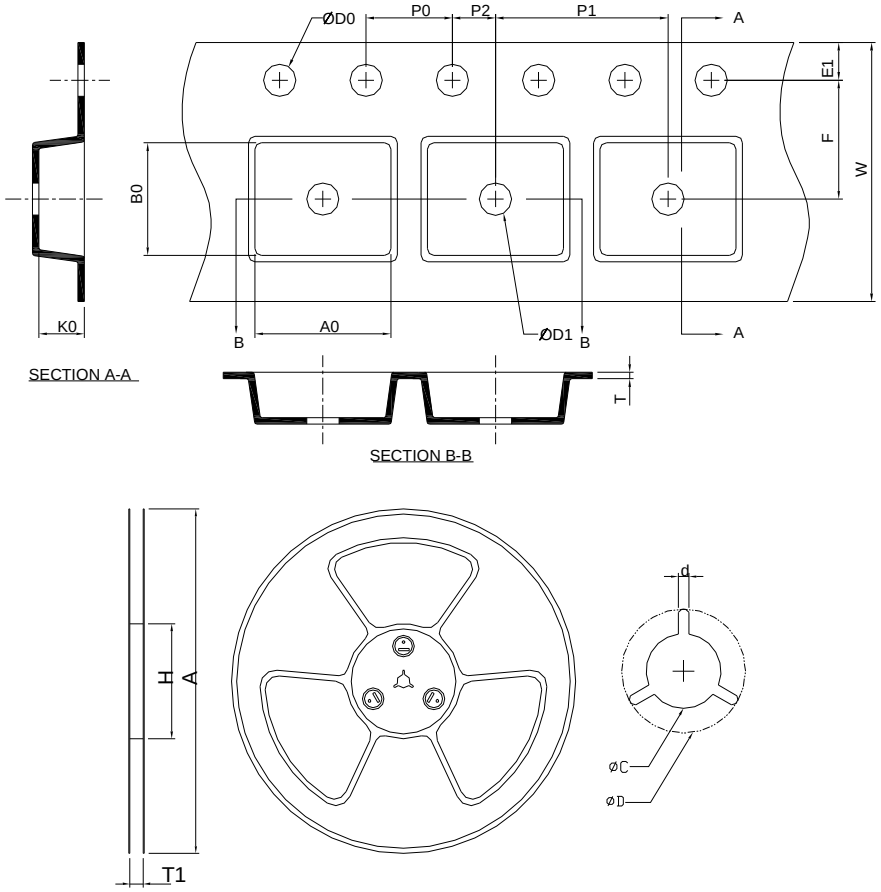
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

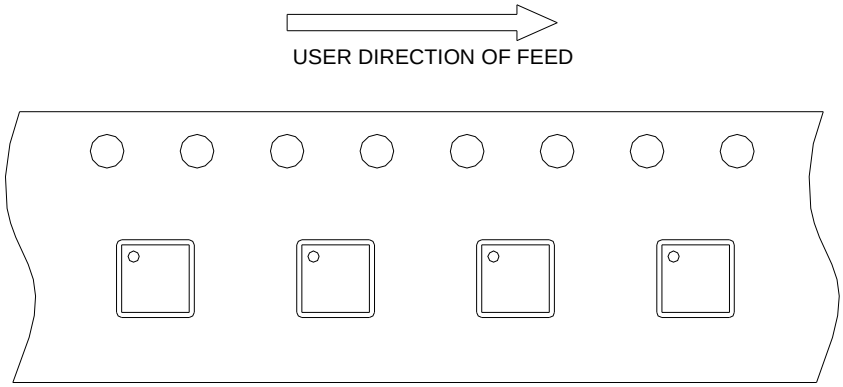
(mm)

Devices Per Unit

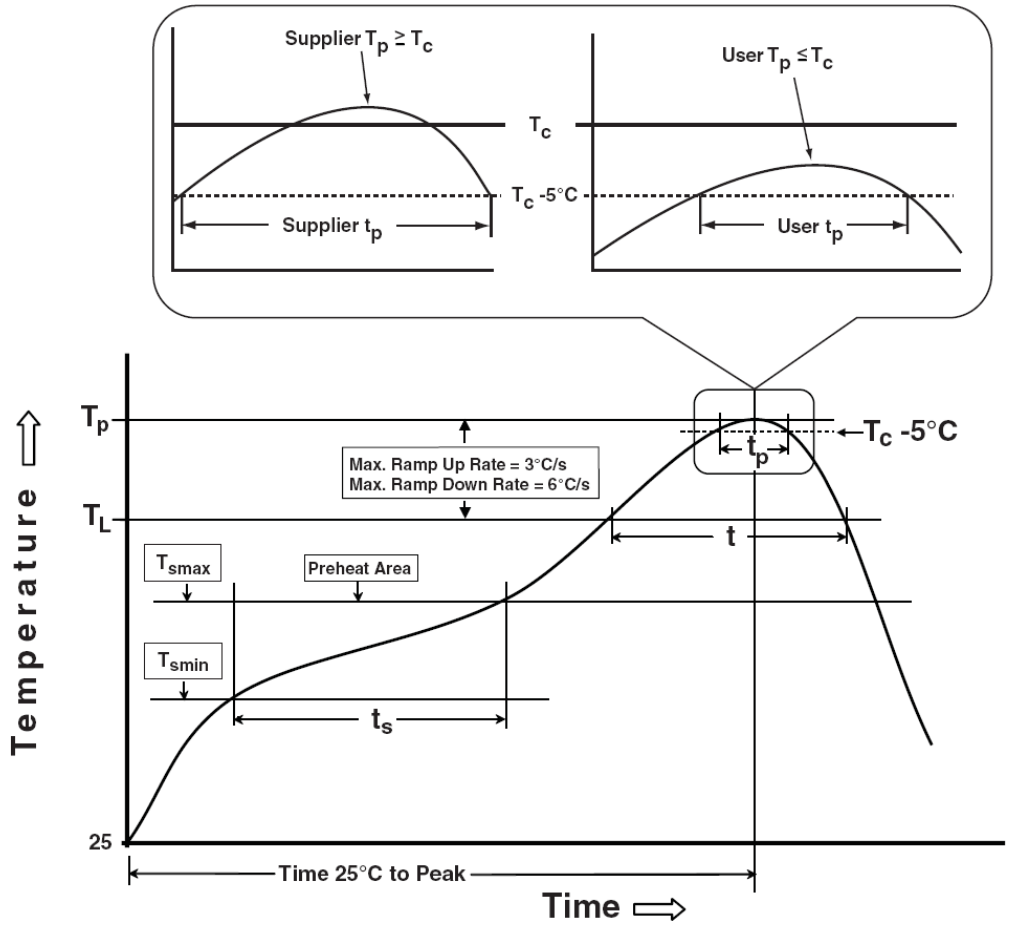
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

Taping Direction Information

TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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