

SE20N110

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

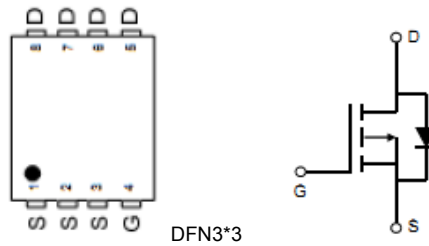
Features

For a single MOSFET

- $V_{DS} = 20V$
- $R_{DS(ON)} = 3.9m\Omega @ V_{GS}=4.5V$

Pin configurations

See Diagram below



Absolute Maximum Ratings

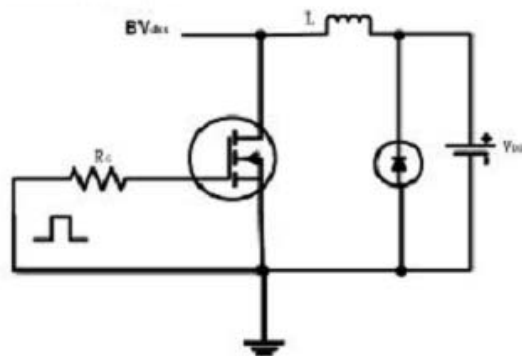
Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	110	A
	Pulsed		340	
Total Power Dissipation	@TA=25°C	P_D	90	W
Operating Junction Temperature Range		T_J	-55 to 150	°C

SE20N110

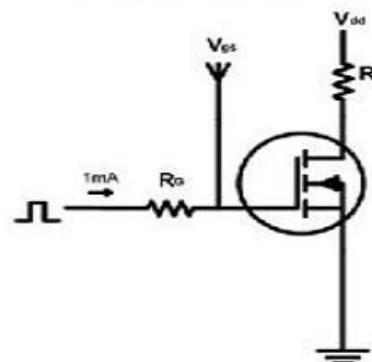
Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0 V	20			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 24V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =20 V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	0.5	0.7	1	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =20A	-	3.9	5.5	mΩ
		V _{GS} =2.5V, I _D =15A		6	9	
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		7032		pF
C _{oss}	Output Capacitance			898		pF
C _{rss}	Reverse Transfer Capacitance			743		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =10V, V _{DS} =15V, I _D =30A		80		nC
Q _{gs}	Gate Source Charge			19		nC
Q _{gd}	Gate Drain Charge			38		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =15V, R _{GEN} =1Ω I _D =1A		20		ns
t _{d(off)}	Turn-Off Delay Time			80		ns
t _{d(r)}	Turn-On Rise Time			36		ns
t _{d(f)}	Turn-Off Fall Time			33		ns
Thermal Resistance						
Symbol	Parameter		Typ	Max		Units
R _{θJC}	Junction to Case		-	2		°C/W
R _{θJA}	Junction to Ambient (t ≤ 10s)		-	50		°C/W

Test Circuits and Waveform

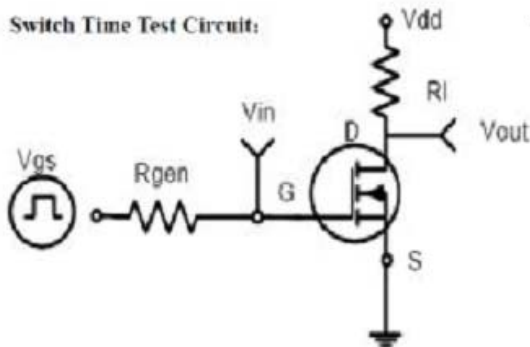
EAS test circuits:



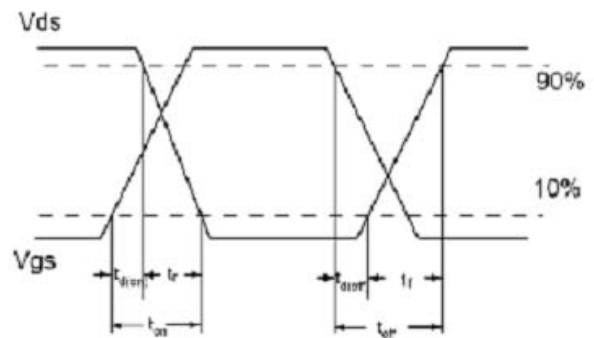
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Typical Characteristics

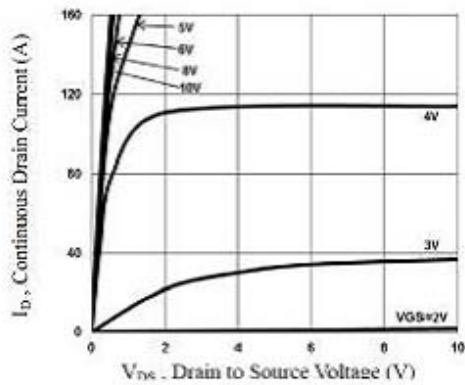


Figure 1: Typical Output Characteristics

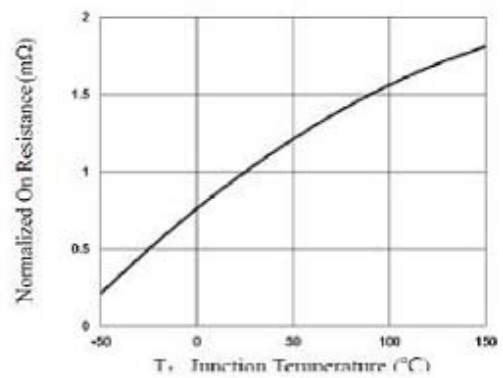


Figure 2: Normalized RDS(on) vs. TJ

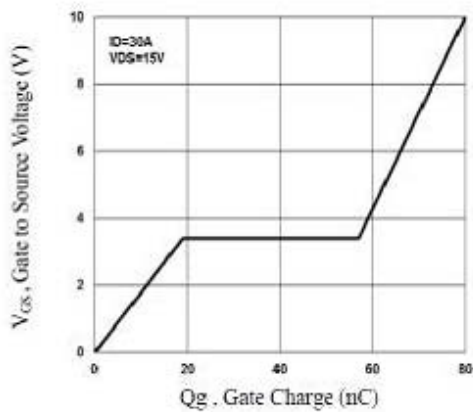


Figure 3: Gate-Charge Characteristics

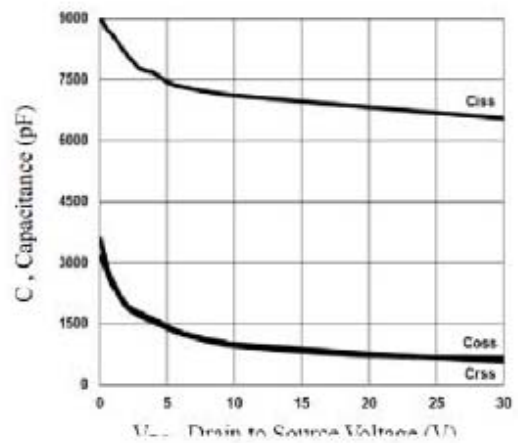


Figure 4: Capacitance Characteristics

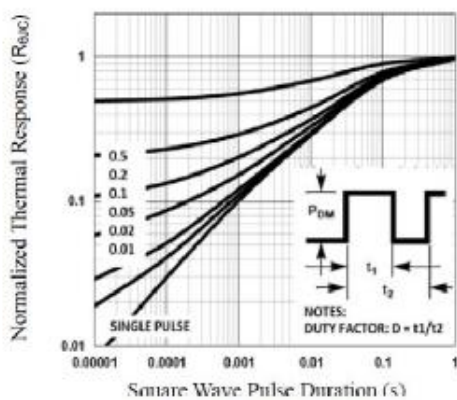


Figure 5: Normalized Thermal transient Impedance Curve

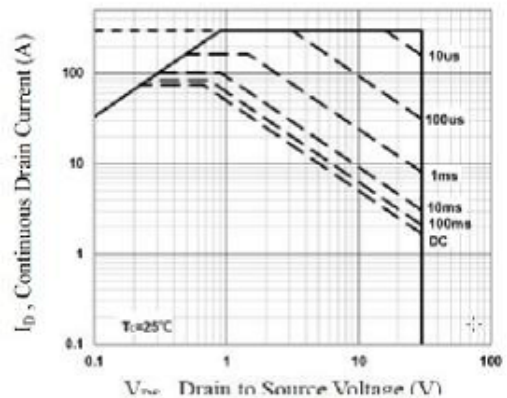
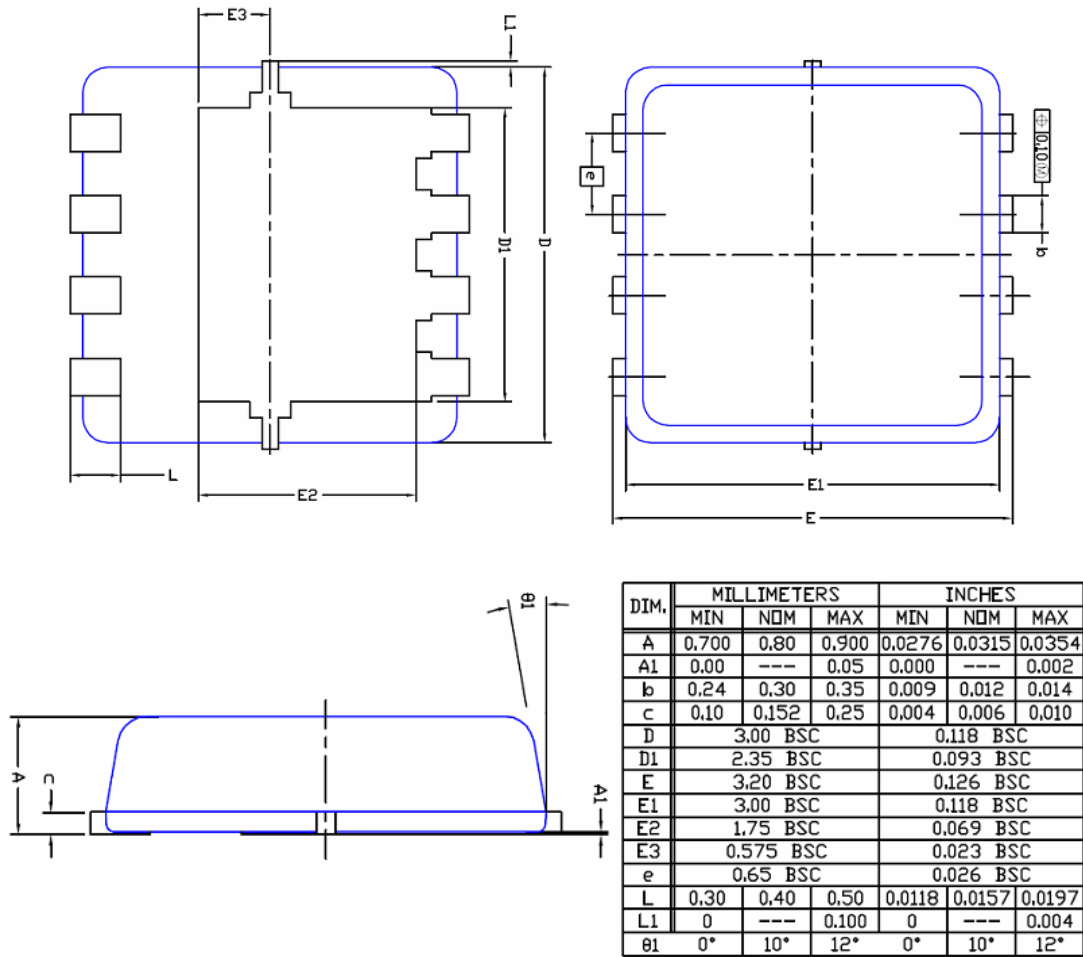


Figure 6: Maximum Safe Operation Area

SE20N110

Package Outline Dimension

DFN3 × 3



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SHANGHAI SINO-IC MICROELECTRONICS CO., LTD

Add: Building 3, Room 3401-03, No.200 Zhangheng Road,
ZhangJiang Hi-Tech Park, Pudong, Shanghai 201203, China

Phone: +86-21-33932402 33932403

33932405 33933508 33933608

Fax: +86-21-33932401

Email: szrxw002@126.com

Website: <http://www.sino-ic.net>