

SE100130GA

**N-Channel Enhancement-Mode MOSFET**

Revision: A

**General Description**

This type used advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge.

- High density cell design for ultra low  $R_{DS(ON)}$
- Excellent package for good heat dissipation

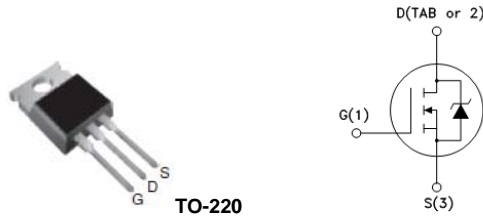
**Features**

For a single MOSFET

- $V_{DS} = 100V$
- $R_{DS(ON)} = 4m\Omega @ V_{GS}=10V$

**Pin configurations**

See Diagram below



**Absolute Maximum Ratings**

Parameter		Symbol	Rating	Units
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current <sup>1</sup>	Continuous	$I_D$	100	A
	Pulsed		390	
Total Power Dissipation	@TA=25°C	$P_D$	176	W
Operating Junction Temperature Range		$T_J$	-55 to 175	°C
Avalanche Energy, Single Pulsed		$E_{AS}$	400	mJ

**Thermal Resistance**

Symbol	Parameter	Min	Typ	Units
$R_{\theta JC}$	Junction to Case		0.85	°C/W

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Electrical Characteristics (T <sub>J</sub> =25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS (Note 2)</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0 V	100			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>DS</sub> = 100V, V <sub>GS</sub> =0V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	2	2.8	4.0	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		4	5	mΩ
g <sub>FS</sub>	Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		75		S
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz		3650		pF
C <sub>oss</sub>	Output Capacitance			290		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			88		pF
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =20A		56		nC
Q <sub>gs</sub>	Gate Source Charge			14		nC
Q <sub>gd</sub>	Gate Drain Charge			18		nC
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>GEN</sub> =10Ω		17		ns
t <sub>d(off)</sub>	Turn-Off Delay Time			57		ns
t <sub>d(r)</sub>	Turn-On Rise Time			40		ns
t <sub>d(f)</sub>	Turn-Off Fall Time			37		ns
<b>REVERSE DIODE</b>						
I <sub>S</sub>	Diode Continuous Forward Current	T <sub>C</sub> =25°C			20	A
V <sub>SD</sub>	Diode Forward Voltage	V <sub>DS</sub> =0V, I <sub>F</sub> =20V,		0.9	1.2	V
T <sub>rr</sub>	Reverse Recovery Time	V <sub>R</sub> =50V, I <sub>F</sub> =I <sub>S</sub>		50		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dT=500A/us		255		nC

Typical Characteristics

Fig 1. Typical Output Characteristics

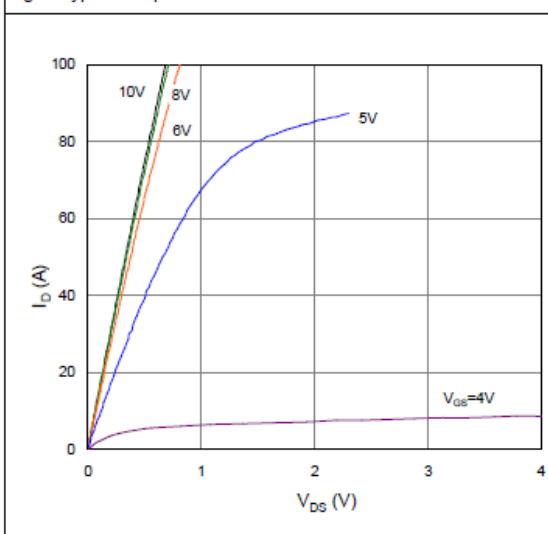


Figure 2. On-Resistance vs. Gate-Source Voltage

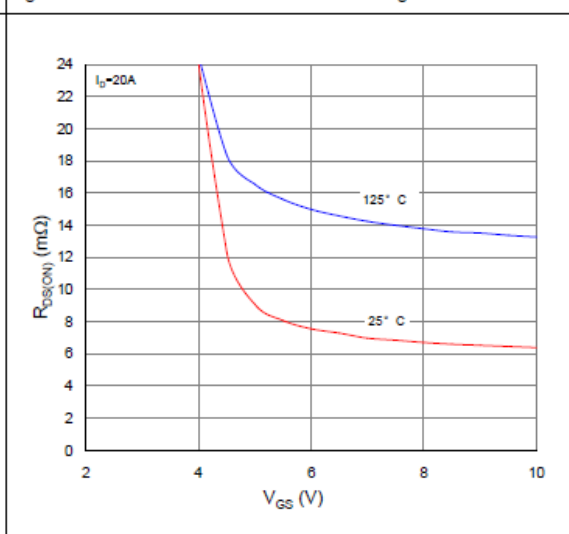


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

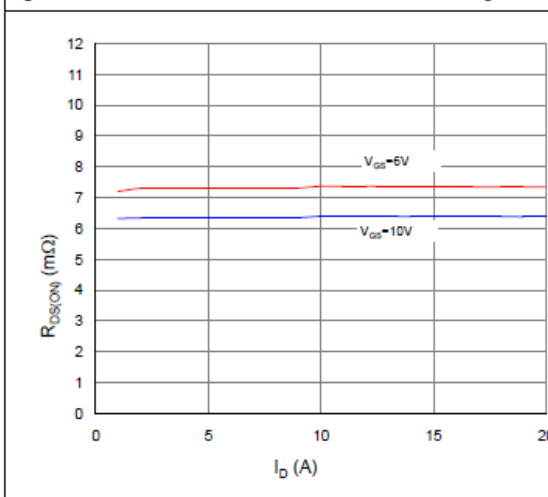


Figure 4. Normalized On-Resistance vs. Junction Temperature

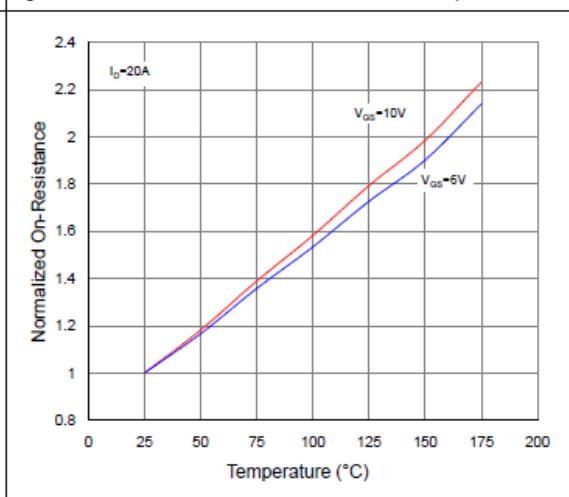


Figure 5. Typical Transfer Characteristics

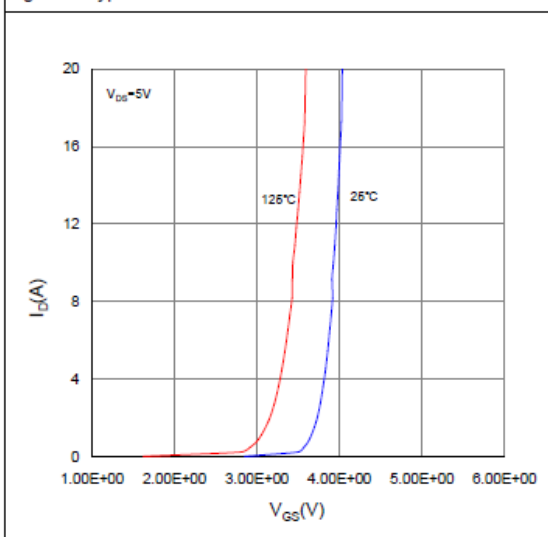
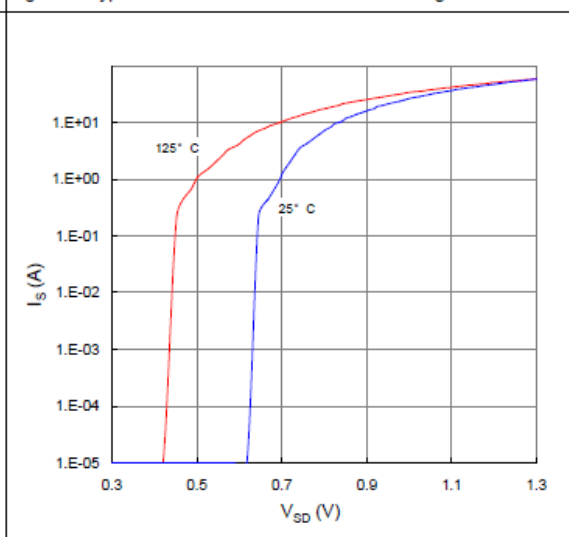


Figure 6. Typical Source-Drain Diode Forward Voltage



Typical Characteristics

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

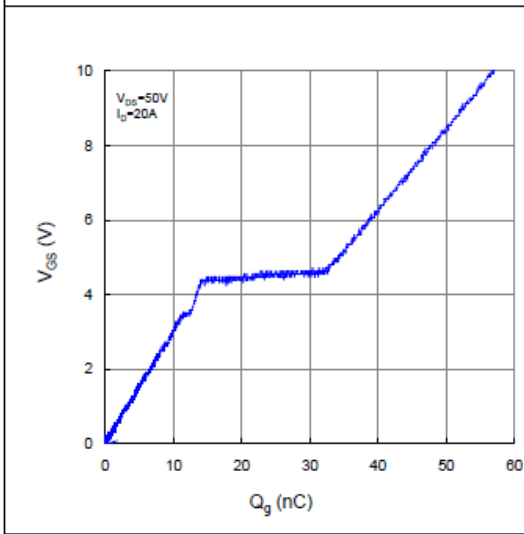


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

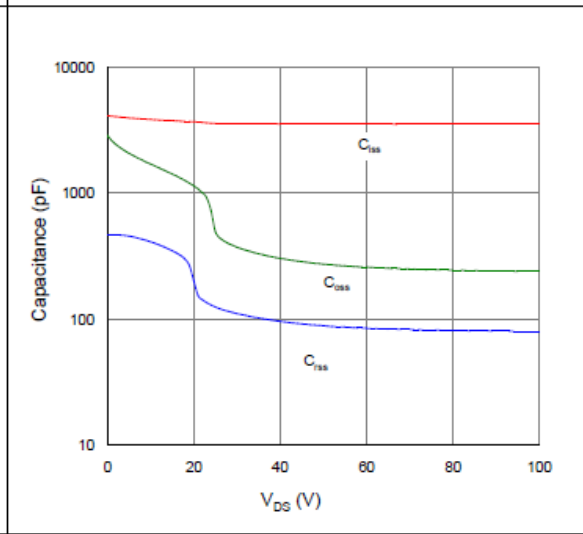


Figure 9. Maximum Safe Operating Area

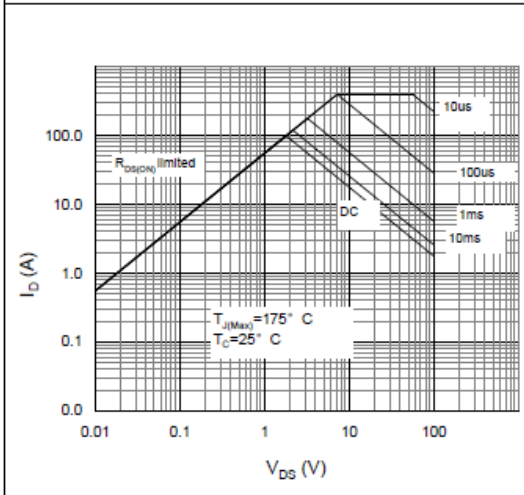


Figure 10. Maximum Drain Current vs. Case Temperature

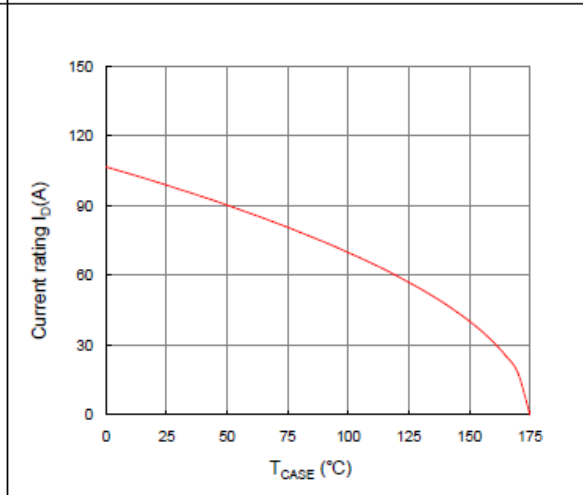
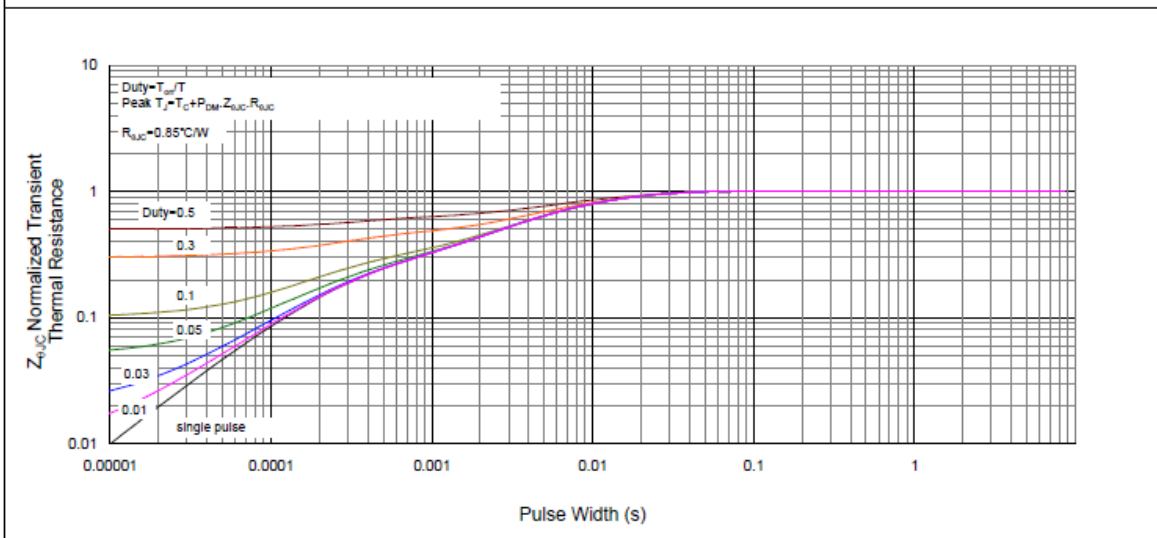


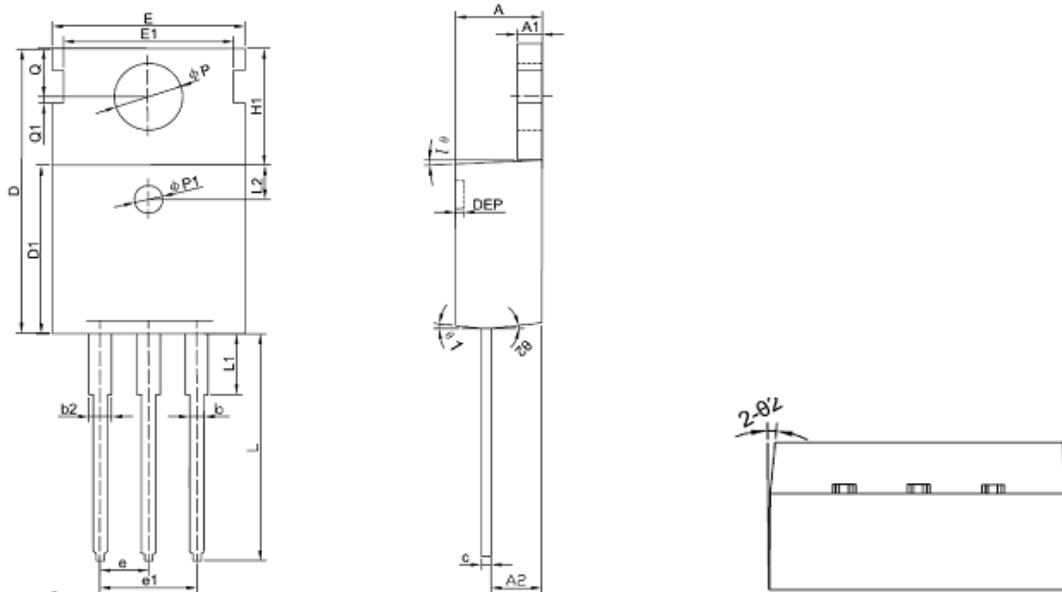
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



# SE100130GA

## Package Outline Dimension

### TO-220



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.590	2.690	2.790	0.102	0.106	0.110
b	0.770	-	0.900	0.030	-	0.035
b2	1.230	-	1.360	0.048	-	0.054
c	0.480	0.500	0.520	0.019	0.020	0.020
D	15.100	15.400	15.700	-	0.606	-
D1	9.000	9.100	9.200	0.354	0.358	0.362
DEP	0.050	0.285	0.520	0.002	0.011	0.020
E	10.060	10.160	10.260	0.396	0.400	0.404
E1	-	8.700	-	-	0.343	-
$\Phi P1$	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.100	6.300	6.500	0.240	0.248	0.256
L	12.750	12.960	13.170	0.502	0.510	0.519
L1	-	-	3.950	-	-	0.156
L2	1.85REF			0.073REF		
$\Phi P$	3.570	3.600	3.630	0.141	0.142	0.143
Q	2.730	2.800	2.870	0.107	0.110	0.113
Q1	-	0.200	-	-	0.008	-
$\theta 1$	5 <sup>0</sup>	7 <sup>0</sup>	9 <sup>0</sup>	5 <sup>0</sup>	7 <sup>0</sup>	9 <sup>0</sup>
$\theta 2$	1 <sup>0</sup>	3 <sup>0</sup>	5 <sup>0</sup>	1 <sup>0</sup>	3 <sup>0</sup>	5 <sup>0</sup>

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