SHANGHAI SINO-IC MICROELECTRONICS CO., LTD.

Jun 2015

SE30P50B

P-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

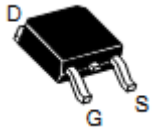
Features

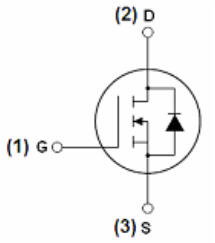
For a single MOSFET

- V_{DS} = -30V
- $R_{DS(ON)}$ = 5.8mΩ @ V_{GS}=-10

Pin configurations

See Diagram below





Absolute Maximum Ratings

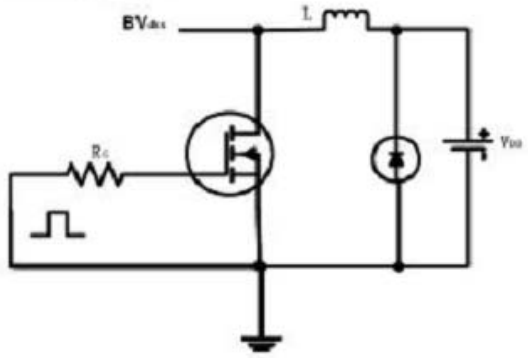
Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	-50	A
	Pulsed		-120	
Total Power Dissipation	@TA=25℃	P_D	90	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0 V	-30			V
I_{DSS}	Drain to Source Leakage Current	V_{DS}= -30V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20 V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	-0.4	-1.5	-2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance [2]	V_{GS}=-10V, I_D=-20A	-	5.8	7	mΩ
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		7032		pF
C_{oss}	Output Capacitance			898		pF
C_{rss}	Reverse Transfer Capacitance			743		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge [2]	V_{GS}=10V, V_{DS}=15V, I_D=30A		80		nC
Q_{gs}	Gate Source Charge			19		nC
Q_{gd}	Gate Drain Charge			38		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=15V, R_{GEN}=1Ω I_D=1A		20		ns
$t_{d(off)}$	Turn-Off Delay Time			80		ns
$t_{d(r)}$	Turn-On Rise Time			36		ns
$t_{d(f)}$	Turn-Off Fall Time			33		ns

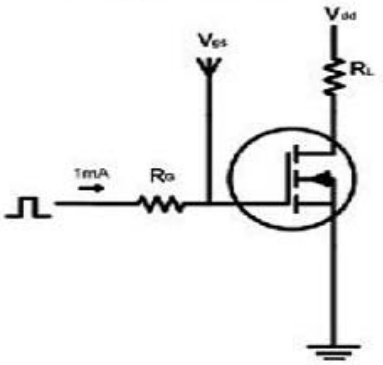
Thermal Resistance				
Symbol	**Parameter**	**Typ**	**Max**	**Units**
$R_{\theta JC}$	Junction to Case	-	2	℃/W
$R_{\theta JA}$	Junction to Ambient (t≦10s)	-	50	℃/W

Test Circuits and Waveform

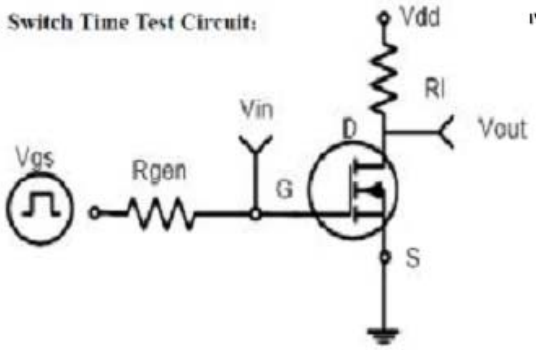
EAS test circuits:



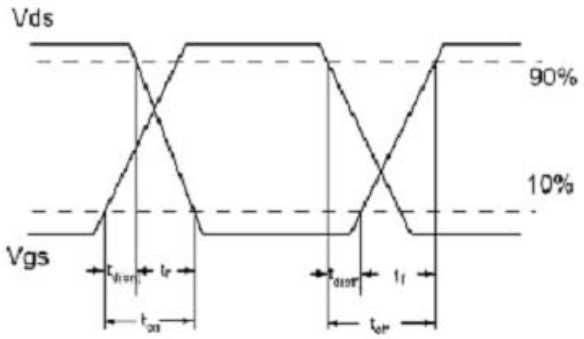
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Typical Characteristics

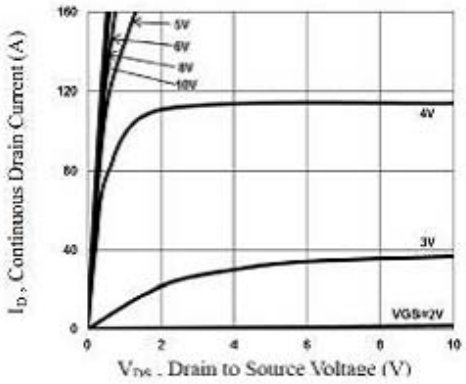


Figure 1: Typical Output Characteristics

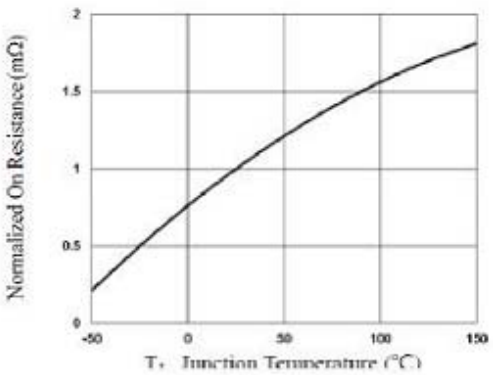


Figure 2: Normalized RDSON vs. TJ

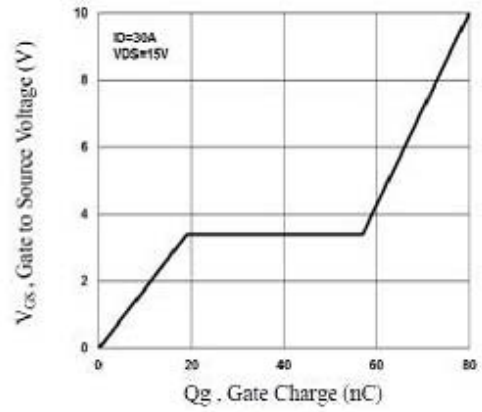


Figure 3: Gate-Charge Characteristics

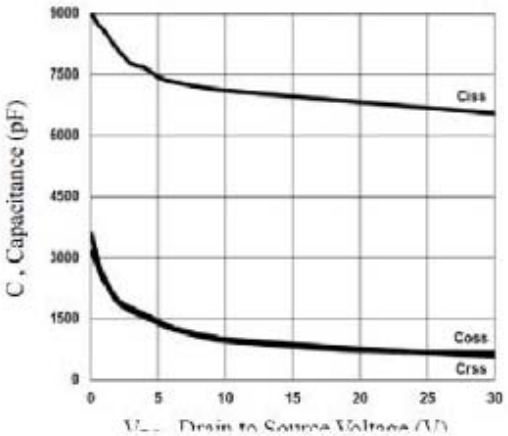


Figure 4: Capacitance Characteristics

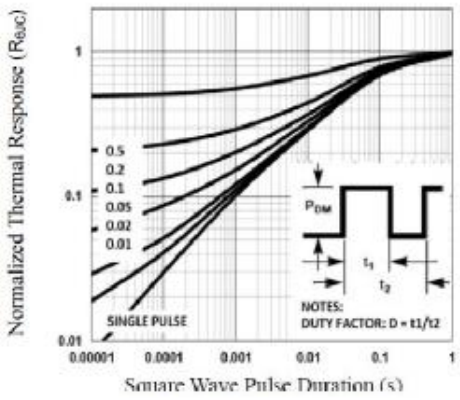


Figure 5: Normalized Thermal transient Impedance Curve

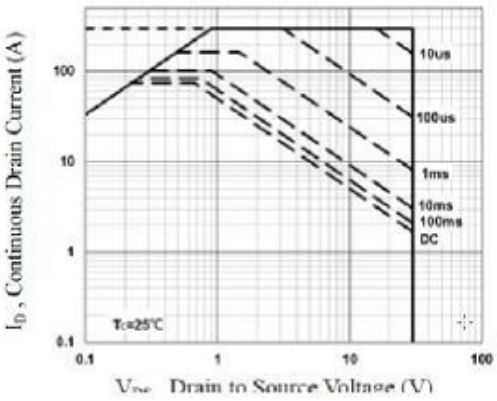
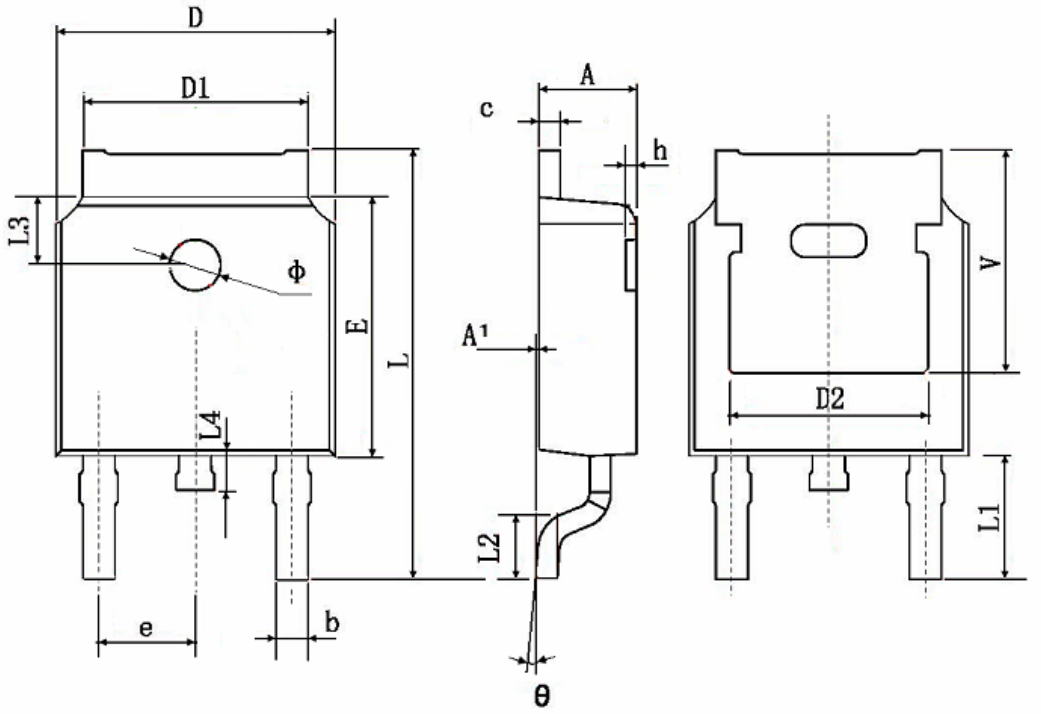


Figure 6: Maximum Safe Operation Area

Package Outline Dimension

TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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