IVCSP002 Dual Channel Low Side Gate Drive IC

Features

- 4A peak source and sink current
- Wide VDD range up to 24V
- Under Voltage Lockout
- Non-inverting input with Enable control
- TTL and CMOS compatible input
- Low propagation delay

Applications

- Generic Low Side Gate Driver
- Power Tools
- Motor Control
- AC/DC and DC/DC converters
- Emerging Wide Band-Gap Power Devices

Description

The IVCSP002 is a dual channel 4A low side Gate drive IC. The input is compatible with TTL or CMOS logic levels. When input is low or floating, output stays low.

Each channel output is independently controlled by its enable control input. The output stays low if enable control input is pulled low. The enable control inputs are TTL or CMOS compatible.

Wide VDD operating range from 4.5V to 20V enables effective driving with Si MOSFET, IGBT or GaN power switches. Under Voltage Lockout (UVLO) ensures output held at low when VDD is low.

Typical Application Diagram

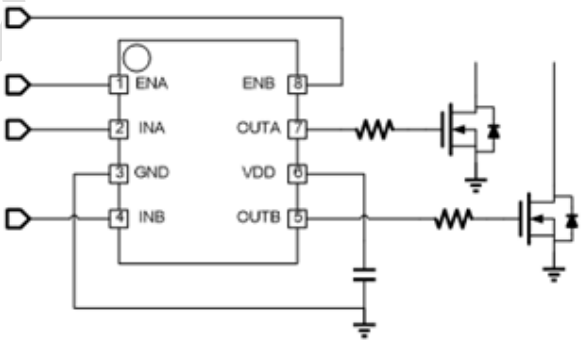


Table of Contents

1. Device Information

PART NUMBER	PACKAGE	PACKING
IVCSP002DR	SOIC-8	Tape and Reel
IVCSP002D	SOIC-8	Tube

2. Pin Configuration and Functions

PIN	NAME	I/O	DESCRIPTION
1	ENA	I	Channel A enable input
2	INA	I	Channel A input
3	GND	G	Driver ground
4	INB	I	Channel B input
5	OUTB	O	Channel B driver output
6	VDD	P	Positive bias supply
7	OUTA	O	Channel A driver output
8	ENB	I	Channel B enable input

3. Truth Table

VDD is higher than UVLO threshold.

ENx	INx	OUTx
L	X	L
H or floating	L	L
H or floating	H	H
H or floating	floating	L

4. Specifications

4.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Total supply voltage (reference to GND)	-0.3	24	V
OUTA, OUTB	Gate driver output voltage	-0.3	V_{DD}+0.3	V
INA, INB	Signal input voltage	-5	24	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

4.2 ESD Rating

		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	4.5	20	V
$V_{INx, ENx}$	Input voltage	0	20	V
T_A	Ambient temperature	-40	125	°C

4.4 Thermal Information

		SOIC-8	UNIT
$R_{\theta JA}$	Junction-to-Ambient	128	°C/W
$R_{\theta JB}$	Junction-to-PCB	68.5	°C/W

4.5 Electrical Specifications

Unless otherwise noted, V_{DD} = 12 V, T_A = –40°C to 125°C
Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
I_{DDoff}	Startup current	VDD=3V, INA=INB=0V		70		μA
I_{DDq}	Quiescent current	INA=INB=0V		180		μA
UVLO						
V_{ON}	Under voltage thresholds	Rising threshold		3.8	4.2	V
V_{OFF}		Falling threshold	3.2	3.5		V
INPUT (INA, INB)						
V_{INH}	Input rising threshold			2.0	2.4	V
V_{INL}	Input falling threshold		0.8	1.2		V
V_{INHYS}	Input hysteresis			0.8		V
V_{INNS}	Input negative voltage capability		-5			V
ENABLE INPUT (ENA, ENB)						
V_{ENH}	Enable input rising threshold			1.8	2.2	V
V_{ENL}	Enable input signal threshold		0.8	1.1		V
V_{INHYS}	Enable input hysteresis			0.7		V
OUTPUTS (OUTA, OUTB)						
I_O	Peak source and sink currents	C_{LOAD} =0.22uF, with external current limiting resistors, 1kHz switching frequency		4		A
V_{OH}	Output high voltage	I_{OUTH} = -10mA		V_{DD}-0.05	V_{DD}-0.12	V
V_{OL}	Output low voltage	I_{OUTL} = 10mA		0.0057	0.012	V
R_{OH}	Output static pull-up resistance			5	12	Ω
R_{OL}	Output pull-down resistance			0.57	1.2	Ω
Timing						
TD_{rr}	Rising delay	C_{LOAD} = 1.8nF		16	30	ns
TD_{ff}	Falling delay			16	30	
T_r	Rise time	C_{LOAD} = 1.8nF		6	12	ns
T_f	Fall time			6	12	
T_{dm}	Delay mismatch	INA=INB, ENA=ENB=VDD		1		ns

5. Typical Characteristics

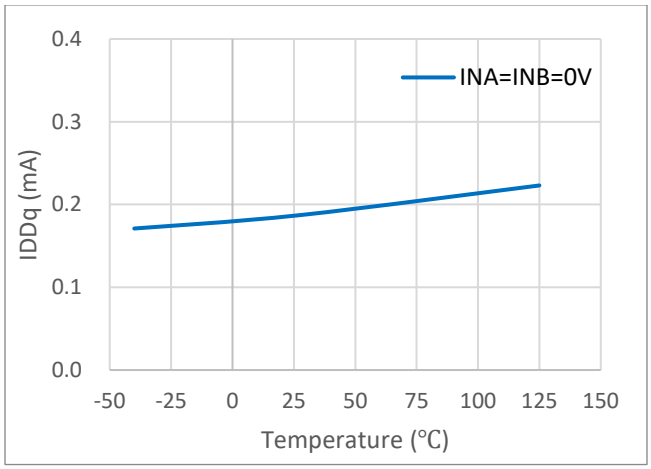


Figure 1. Quiescent Current IDDq vs Temperature

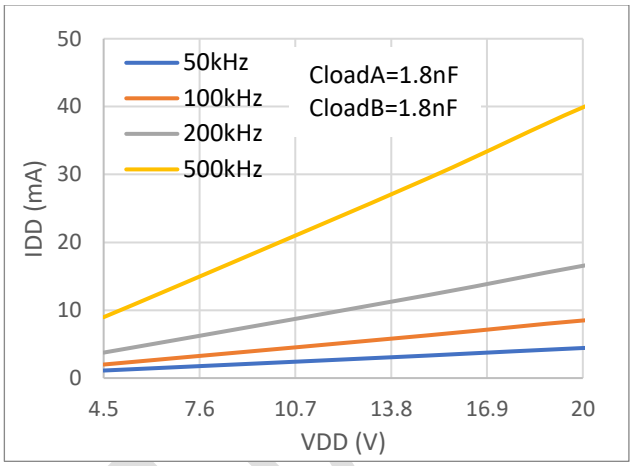


Figure 2. Operating Current IDD vs VDD

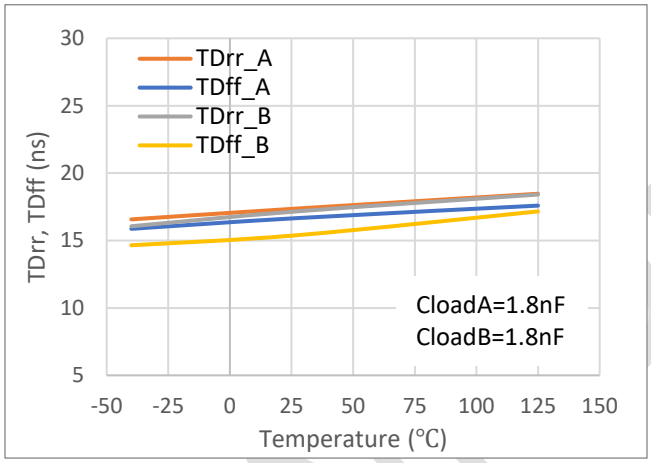


Figure 3. Propagation Delay vs Temperature

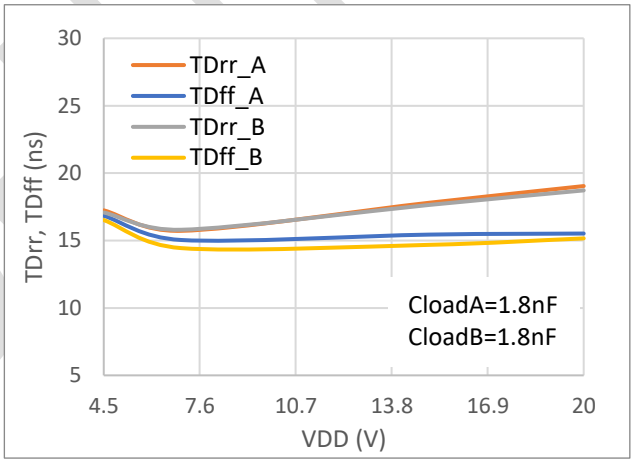


Figure 4. Propagation Delay vs VDD

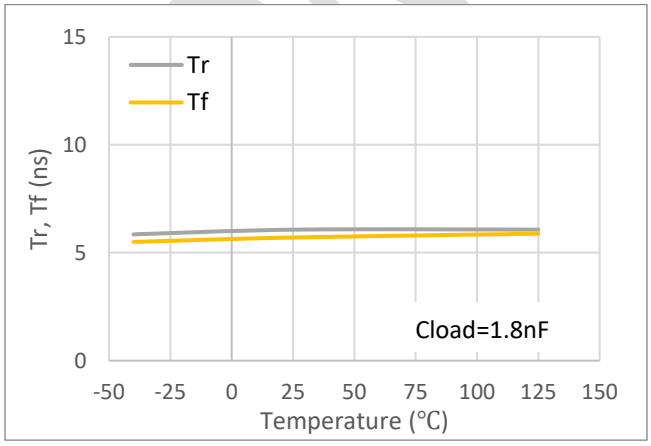


Figure 5. Rise Time and Fall time vs Temperature

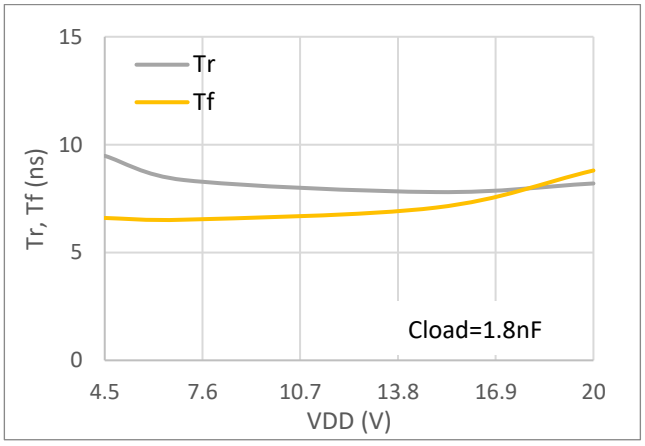
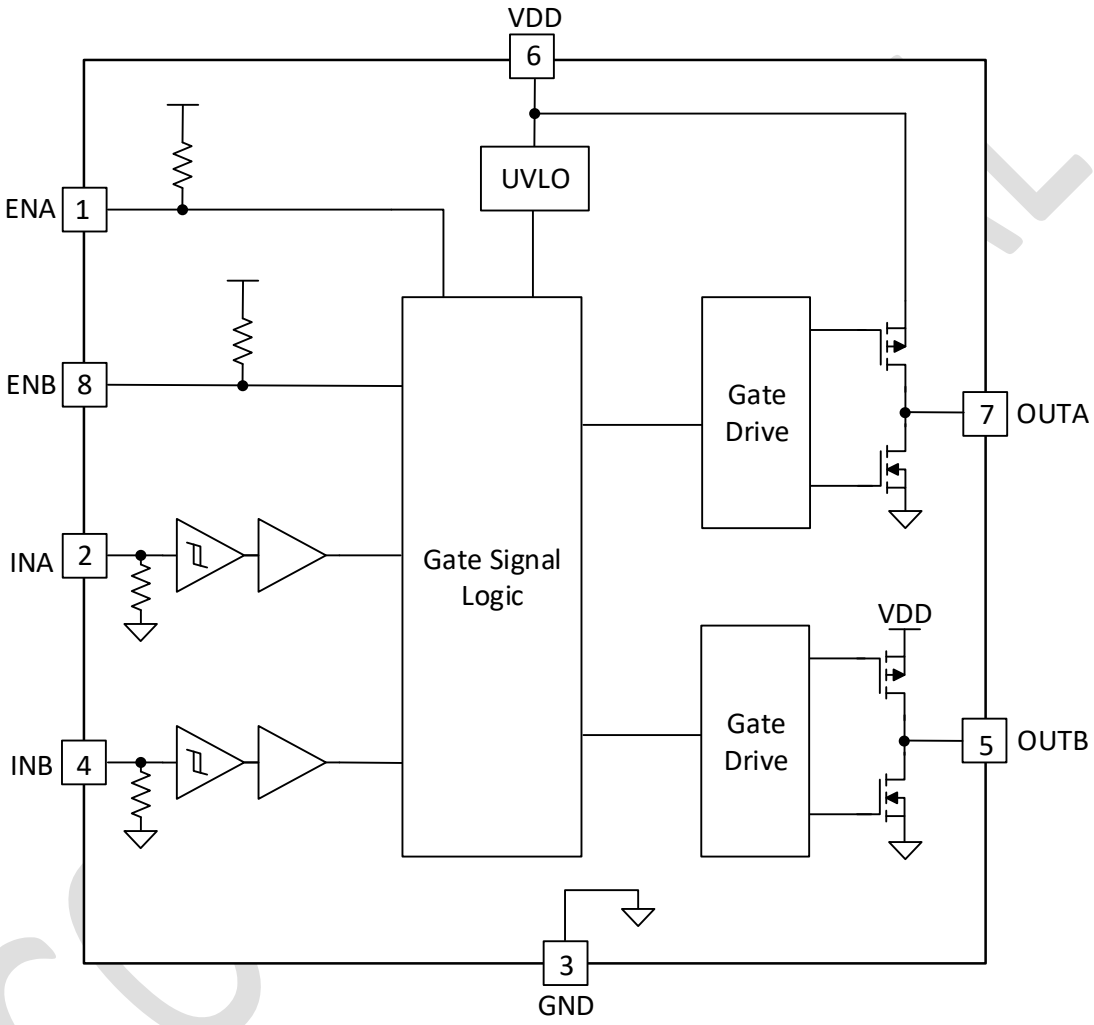


Figure 6. Rise Time and Fall time vs VDD

6. Detail Descriptions

IVCSP002 driver provides dual-channel high-speed low-side gate drive. It features tight mismatching outputs when two channels are paralleled to drive large or paralleled power switches.

Function Block Diagram



6.1 Input Signals INA and INB

INA and INB are non-inverting logic gate driver inputs. The pins have a weak pulldown. When left floating, outputs are pulled to GND. The input is a TTL and CMOS logic level with maximum 24V input tolerance.

6.2 Enable Signals ENA and ENB

ENA and ENB are enable control signals. The enable control signal is a TTL and CMOS compatible logic level with maximum 24V tolerance. When ENx is driven low the OUTx is pulled to GND. When ENx is driven high the OUTx follows INx. The enable pins have a weak pullup. When left floating, outputs follow inputs. The enable signal is a TTL and CMOS logic level with maximum 24V input tolerance.

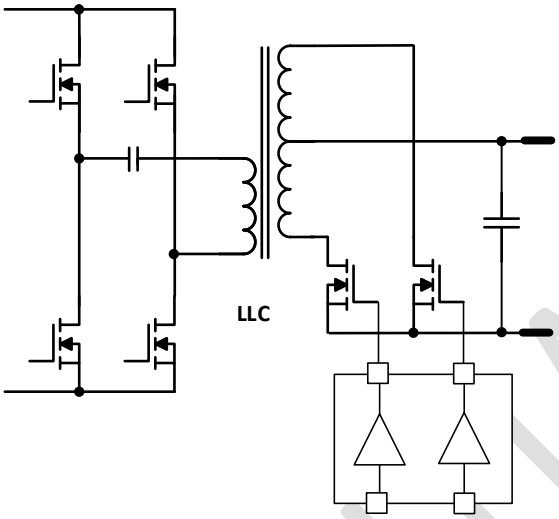
6.3 OUTA and OUTB

OUTA and OUTB are totem-pole outputs, which consist of a hybrid pullup and an N-channel MOSFET for pulldown. Each output stage can supply 4A peak source and 4A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation. The presence of the MOSFET body diodes also offer voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

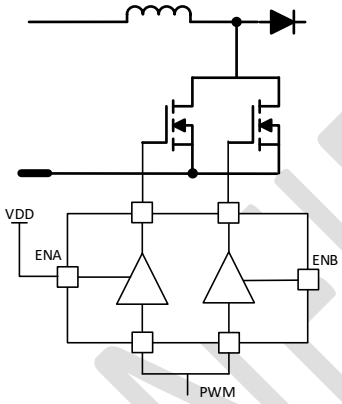
6.4 VDD and Under Voltage Protection

The maximum voltage rating is 24V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The driver has internal under voltage lockout (UVLO) protection feature. When VDD level is below UVLO threshold, this circuit holds the output LOW, regardless of the status of the inputs.

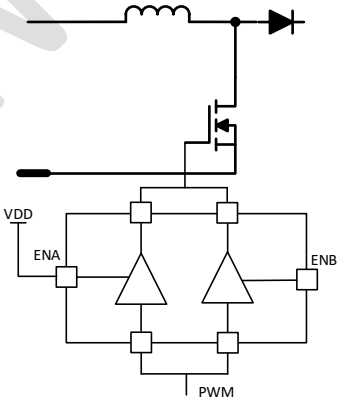
7. Application Implementation



Two channels driven separately



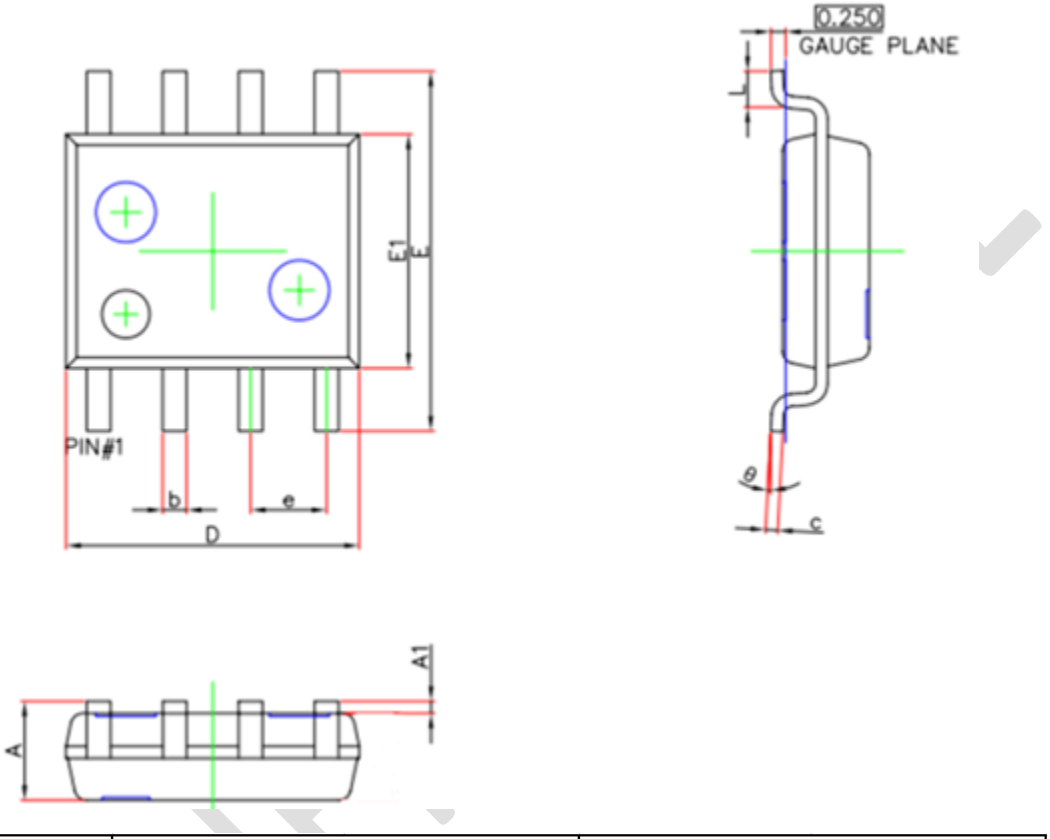
Two paralleled switches driven by two outputs with minimized mismatch



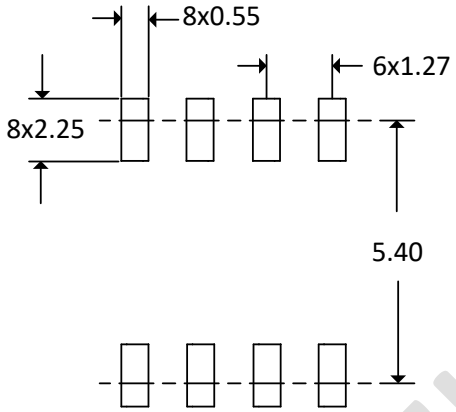
A large switch driven by two paralleled outputs with minimized mismatch

8. Package Information

SOIC-8 Package Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.110	0.250	0.004	0.010
b	0.310	0.510	0.012	0.020
c	0.130	0.250	0.005	0.010
D	4.810	5.000	0.189	0.197
E	5.800	6.190	0.228	0.244
E1	3.810	3.980	0.150	0.157
e	1.270		0.050	
L	0.410	1.270	0.016	0.050
θ	0.000	8.000	0.000	0.315



SOIC-8 Recommended Soldering Dimensions