1Gb NAND FLASH

AFND1G08S3

Revision No.	History	Draft Date	Remark
Rev. 00	Initial Draft	Jan. 2014	Preliminary

FEATURES SUMMARY

- **Single level cell technology**
- **OPEN NAND FLASH INTERFACE(ONFI) 1.0 COMPLIANT**

- **POWER SUPPLY VOLTAGE**
  - VCC/VCCQ = 1.7V ~ 1.95V
- **MEMORY CELL ARRAY (with SPARE)**
  - Page size : x8-(2K+64)bytes
  - Block Size : x8-(128K+4K) bytes
- **PAGE READ / PROGRAM TIME**
  - Random Read Time(tR) : 25us(Max)
  - Sequential access time : 45ns(Min)
  - Page program : 300us(Typ)
- **BLOCK ERASE**
  - Block Erase Time : 3ms(Typ)
- **COMMAND SET**
  - ONFI1.0 Compliant command set
  - Read Unique ID
- **SECURITY**
  - OTP area
  - Serial number(unique ID)
  - Read ID2 extension
  - Non-volatile protection
- **ELECTRONIC SIGNATURE**
  - 1st cycle: Manufacturer Code
  - 2nd cycle: Device Code
  - 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages
  - 4th cycle: Page size, Block size, Organization, Spare size
- **RELIABILITY**
  - 50,000 Program / Erase cycles (with 4 bit ECC per 512 Byte)
- **DATA RETENTION**
  - 10 years
- **CHIP ENABLE DON'T CARE OPTION**
  - Simple interface with microcontrollers

Product Information

Part number	Voltage	Bus Width	Package
AFND1G08S3-CKD	1.7~1.95V	x8	6.5x8.0mm FBGA
AFND1G08S3-CKDI*			

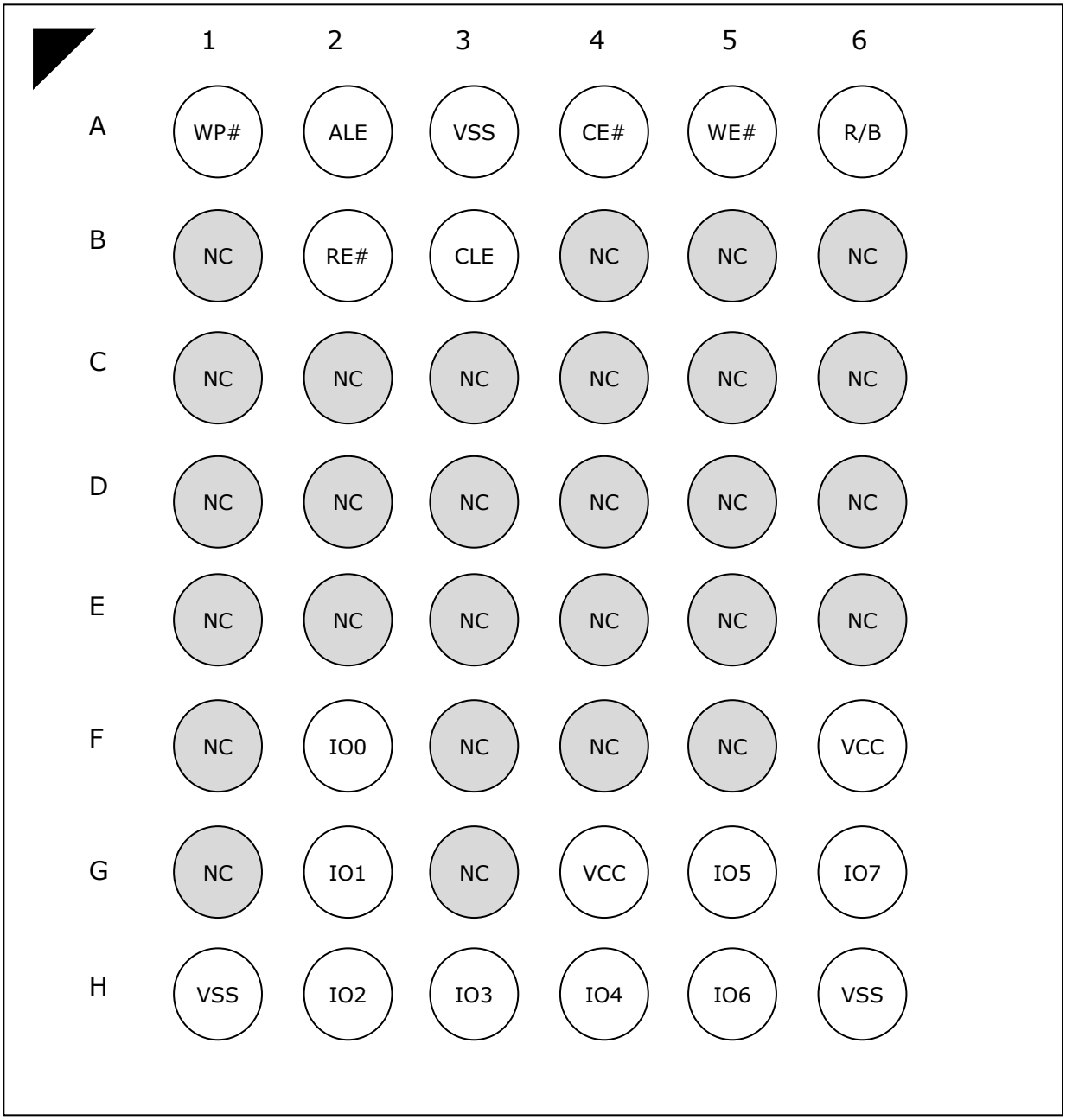
Note) I* : Industrial temperature grade

1 GENERAL DESCRIPTION

This devices are offered in 1.8 Vcc and VccQ Power Supply, and with x8 I/O interface.
Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
Depending on whether the devices have a x8 or x16 bus width, the page size is (2048 + 64 spare) bytes. Each block can be programmed and erased up to 50,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND Flash devices, the implementation of an ECC is mandatory.
The chip supports CE# don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.
In addition, device supports ONFI 1.0 specification. The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.
A write protect pin is available to provide hardware protection against program and erase operations.
The devices feature an open-drain ready/busy output that identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to connect to a single pull up resistor.
The devices have a cache read feature that improves the read throughput for large files. During cache reading, the devices loads the data in a cache register while the previous data is transferred to the I/O buffers to be read. This feature is implemented according to ONFI 1.0 specification.

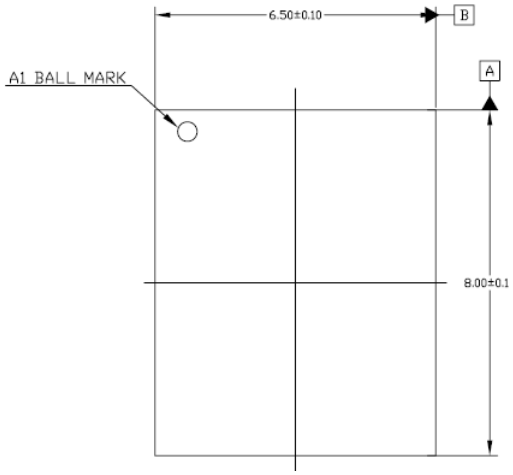
- OTP (one time programmable) area which is a restricted access area where sensitive data/code can be store permanently.
- Serial number(unique identifier) which allows the devices to be uniquely indentified.
- Read ID2 extension
- Non-volatile protection to lock sensible data permanently.

PIN CONFIGURATION (48ball-FBGA)

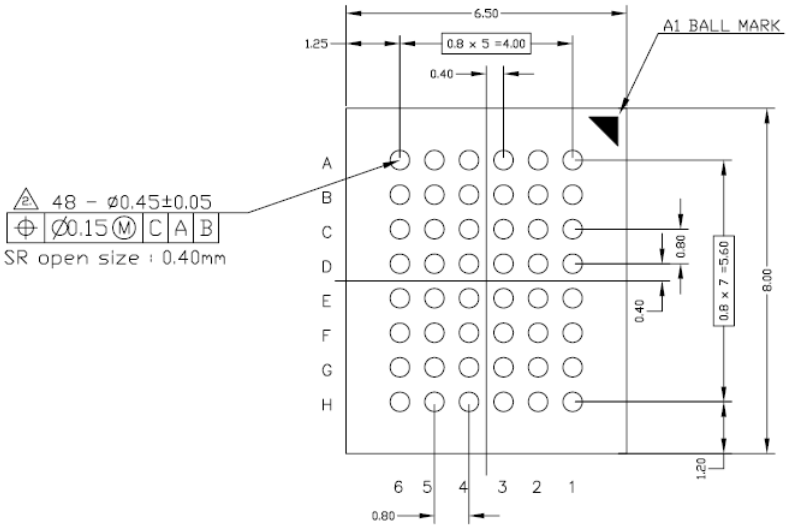


TOP VIEW

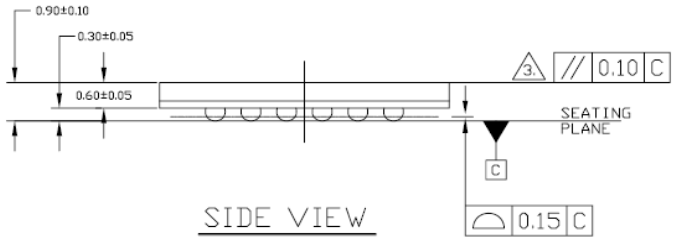
PACKAGE OUTLINE DRAWING (48ball-FBGA 6.5x8mm)



TOP VIEW



BOTTOM VIEW



Description
FBGA 48BALL
Dimension
6.5mm x 8.0mm x 0.90mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

1.1 PIN DESCRIPTION

Pin Name	Pin Function
I/O0 - I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
/CE	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, CE# low does not deselect the memory. The device goes into Stand-by mode when CE# goes High during the device is in Ready state. The CE# signal is ignored when device is in Busy state, and will not enter Standby mode even if the CE# goes high.
/RE	**READ ENABLE** The /RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of /RE which also increments the internal column address counter by one.
/WE	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
/WP	**WRITE PROTECT** The WP# pin, when Low, provides a hardware protection against undesired write operations. Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.
R/B	**READY/BUSY OUTPUT** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**POWER** The VCC supplies the power for all the operations. (Read, Write, and Erase).
VSS	**GROUND**
N.C	**NO CONNECTED / DON'T USE**

Note :
A 0.1uF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

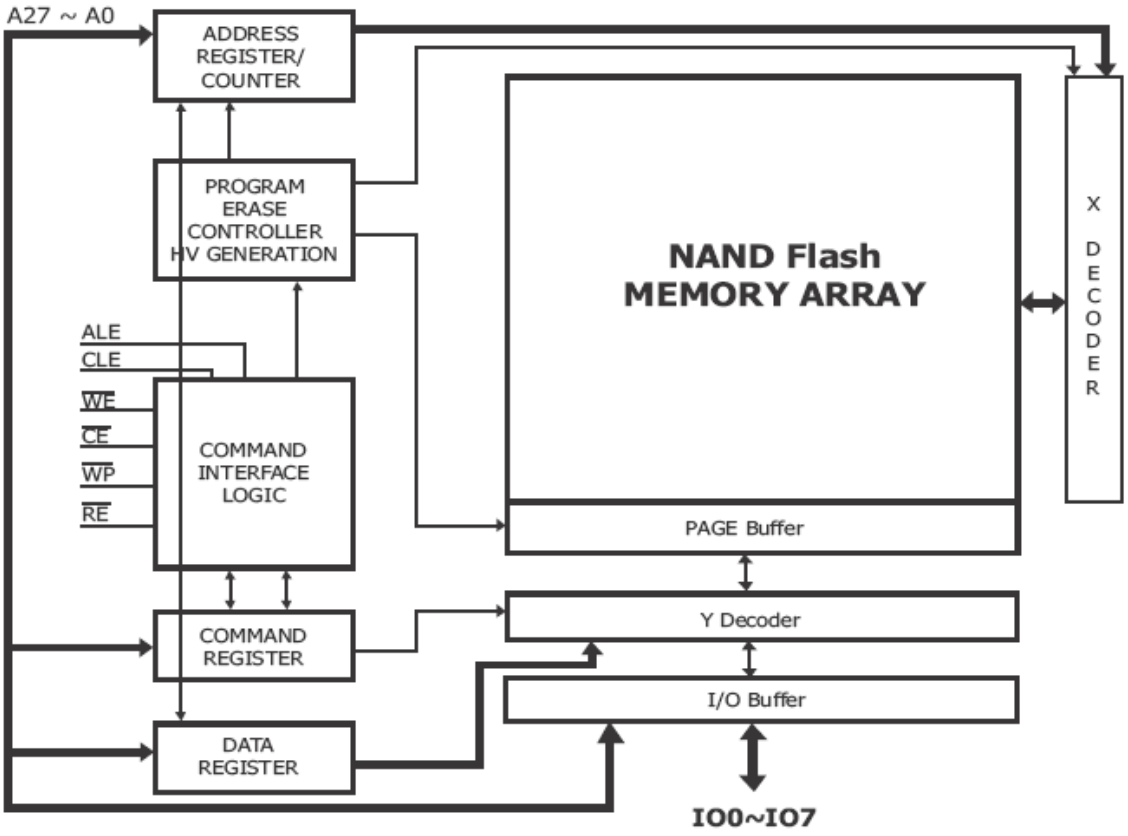
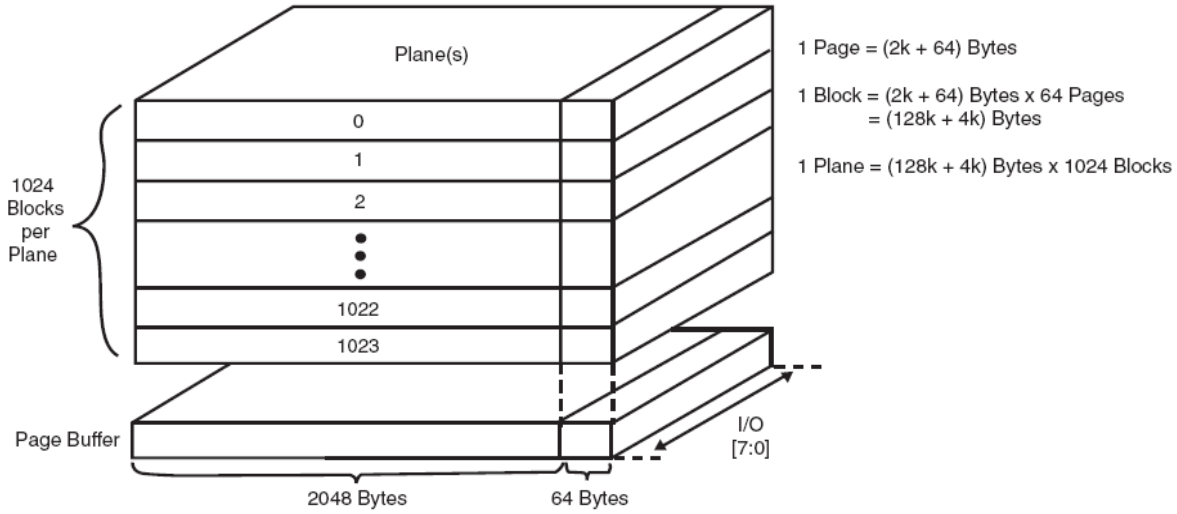


Figure5 : BLOCK DIAGRAM

1.2 Array Organization



X8 Device

Figure6 : ARRAY ORGANIZATION

1.3 Addressing

Table5 : Address Cycle Map (x8)

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1ST Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27

Notes:
1. L must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 4th cycle are Row Address.

1.4 Command Set

FUNCTION	1ST Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable Command During Busy
PAGE READ	00h	30h	-	-	No
READ FOR COPY-BACK	00h	35h	-	-	No
RANDOM DATA OUTPUT	05h	E0h	-	-	No
CACHE READ(Start)	31h	-	-	-	No
CACHE READ(End)	3Fh	-	-	-	No
READ ID	90h	-	-	-	No
READ STATUS REGISTER	70h	-	-	-	Yes
PAGE PROGRAM(Start) CASHE PROGRAM(End)	80h	10h	-	-	No
RANDOM DATA INPUT	85h	-	-	-	No
COPY BACK PROGRAM	85h	10h	-	-	No
CACHE PROGRAM(Start)	80h	15h	-	-	No
BLOCK ERASE	60h	D0h	-	-	No
RESET	FFh	-	-	-	No
PAGE RE-PROGRAM	8Bh	10h	-	-	No
CACHE READ RANDOM	00h	31h	-	-	No

Table6 : Command Set

1.5 Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(4Cycle)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H[1)]	L	Rising	H	H		Address Input(4Cycle)
L	L	L	Rising	H	H	Data Input	
L	L[1)]	L	H	Faling	X	Sequential Read and Data Output	
L	L	L	H[3)]	H[3)]	X	During Read (Busy)	
X	X[1)]	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0V / V_{CC}[2)]	Stand-By	

Table 7 : Mode Selection

Notes:
1. X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and Multi Plane Read Status can be input to the device.

1.6 Block Management

Devices with Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the First or Second page does not contain FFh is a Block. The Block Information must be read before any erase is attempted as the Block Information may be erased. For the system to be able to recognize the Blocks based on the original information it is recommended to create a Block table following the flowchart shown in Figure 7. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

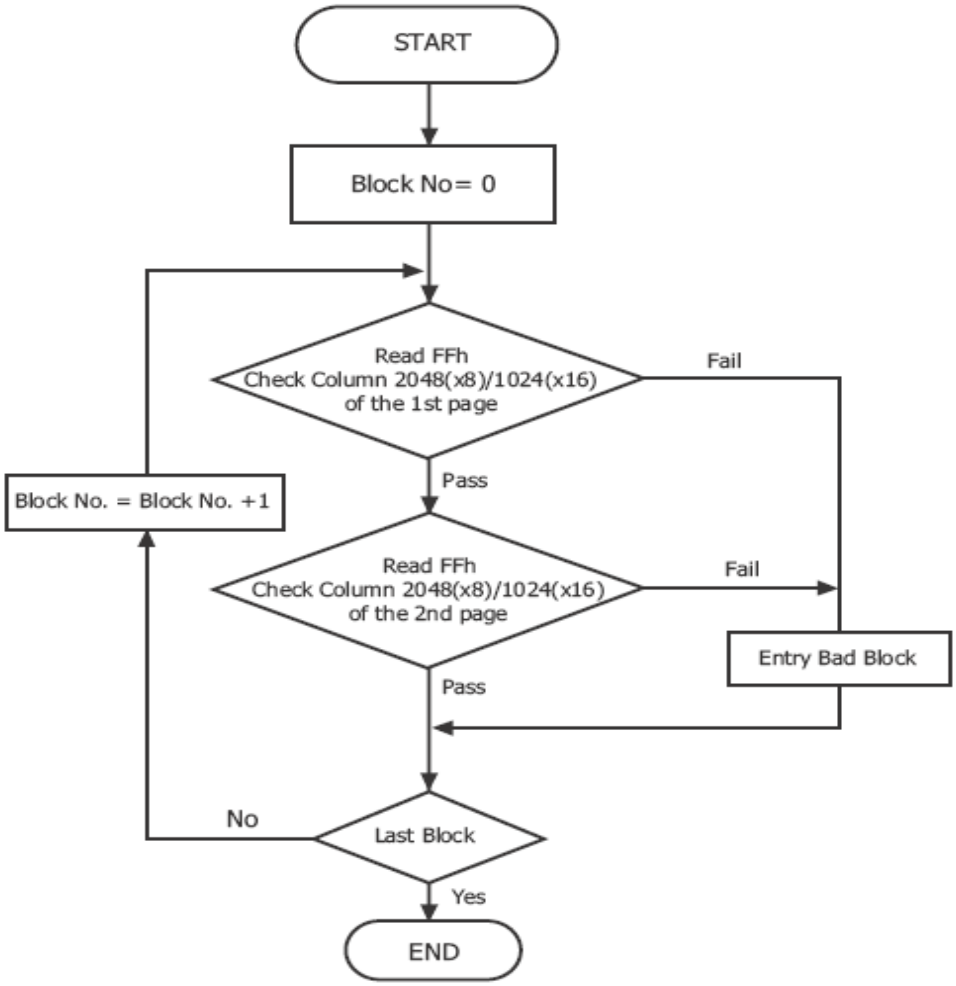


Figure7 : Block management flow chart

Notes:
1. Do not try to erase the detected blocks, because the bock information will be lost.
2. Do not perform program and erase operation in invalid block, it is impossible to guarantee the Input data and to ensure that the function is normal.

1.7 Block Replacement

This device may have the invalid blocks when shipped from factory. An invalid block is one that contains one or more bits. Over the lifetime of the device additional Blocks may develop. In this case, the block has to be replaced by copying the data to a valid block. These additional Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block. block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
Refer to Table 8 and Figure 8 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (4bit / 512+16 Byte)

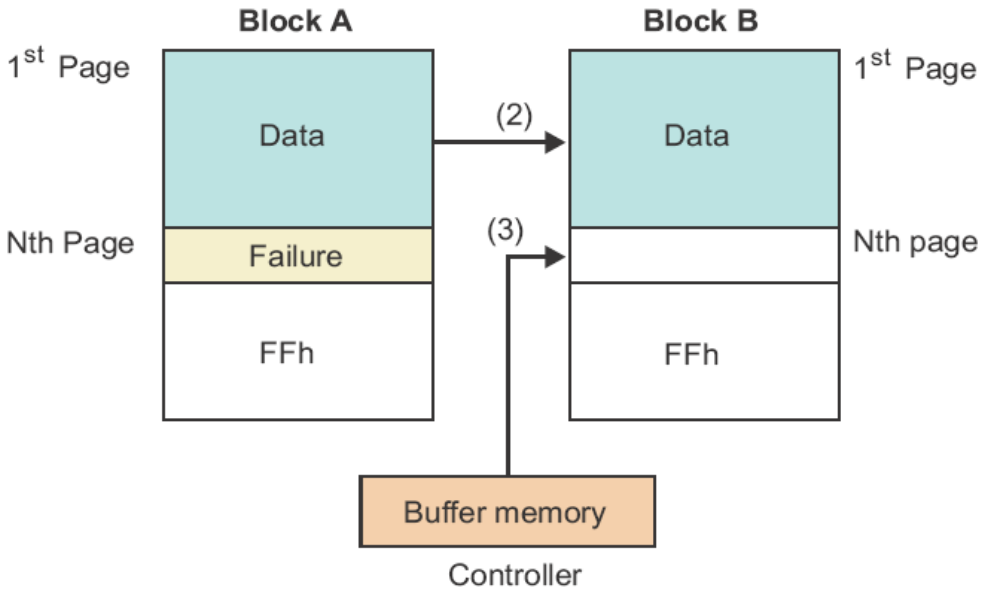


Figure 8 : Block replacement

Notes:
1. An error occurs on nth page of the Block A during Program or Erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth page of block A which is in controller buffer memory is copied into nth page of Block B
4. block table should be updated to prevent from erasing or programming Block A.

2. Electrical Characteristics

2.1 Valid Blocks

	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	1004		1024	Blocks

Notes:
1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bits. The device may contain blocks upon shipment.

2.2 Absolute Maximum Rating

Symbol	Parameter	Value	unit
		Min	
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	°C
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	°C
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	°C
T_{BIAS}	Temperature Under Bias	-50 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
V_{IO}	Input or Output Voltage	-0.6 to 4.6	V
T_{CC}	Suooly Voltage	-0.6 to 4.6	V

Notes:
1. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings Only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied.
   Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2.3 DC and Operating Characteristics

Parameter		Symbol	Test Conditions	1.7V~1.95V			Units
				Min	Typ	Max	
Power on reset current		I_{CC0}	FFh comand input after power on	-	-	50 per device	mA
Operating Current	Read	I_{CC1}	$t_{RC}=t_{RC}$(min), CE#=V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	Normal	0	15	30	mA
			Cache	0	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{CC5}	CE#=V_{CC} -0.2, WP#=0V/V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}= 0 to V_{CC}(MAX)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC}(MAX)	-	-	±10	
Input High Current		V_{IH}	-	V_{CC} x 0.8	-	V_{CC}+0.3	V
Input Low Current		V_{IL}	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH} = 100μA	V_{CC}-0.1	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL} = 100μA	-	-	0.1	V
Output Low Current(R/B#)		I_{OL}(R/B#)	V_{OL}=0.1V	3	4	-	mA
VCC supply voltage (erase and prigram lockout)		V_{LKO}	-	-	1.1	-	V

2.4 AC Test Conditions

Parameter	Value
	1.7V ≤ Vcc ≤ 1.95V
Input Pulse Levels	0 V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load(1.7V-1.95V)	1 TTL GATE and CL=30pF

Note:
These parameters are verified device characterization and are not 100% tested.

2.5 Pin Capacitance (TA=25℃, F=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	10	pF
Input/Output Capacitance	CI/O	VI=0V	-	10	pF

2.6 Program / Read / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	tPROG	-	300	700	us
Read Cache busy time	tCBSYR		3	tR	us
Cache Program short busy time	tCBSYW		5	tPROG	us
Number of Partial Program Cycles in the same page	NOP	-	-	4	cycles
Block Erase Time	tBERS	-	3	10	ms

Notes:
Typical value is measured at Vcc=1.8 V, TA=25℃ (1.8V Device)..Not 100% tested.

2.7 AC Timing Characteristics

Parameter	Symbol	1.8V		Unit
		Min	Max	
CLE setup Time	tCLS	25	-	ns
CLE Hold Time	tCLH	10	-	ns
/CE setup Time	tCS	35	-	ns
/CE Hold Time	tCH	10	-	ns
/WE Pulse Width	tWP	25	-	ns
ALE setup Time	tALS	25	-	ns
ALE Hold Time	tALH	10	-	ns
Data setup Time	tDS	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	45	-	ns
/WE High Hold Time	tWH	15	-	ns
Address to Data loading Time	tADL	100	-	ns
Data Transfer from Cell to Register	tR	-	25	us
ALE to /RE Delay	tAR	10	-	ns
CLE to /RE Delay	tCLR	10	-	ns
Ready to /RE Low	tRR	20	-	ns
/RE Pulse Width	tRP	25	-	ns
WE High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	45	-	ns
/RE Access Time	tREA	-	30	ns
/RE High to Output Hi-Z	tRHZ	-	100	ns
/CE High to Output Hi-Z	tCHZ	-	50	ns
/CE High to ALE or CLE Don't Care	tCSD	10	-	ns
/RE high to Output Hold	tRHOH	15	-	ns
/RE Low to Output Hold	tRLOH	-	-	ns
/RE or /CE High to Output hold	tCOH	15	-	ns
/RE High Hold Time	tREH	15	-	ns
Output Hi-Z to /RE Low	tIR	0	-	ns
/RE High to /WE Low	tRHW	100	-	ns
/WE High to /RE Low	tWHR	60	-	ns
WE# high to RE# low for Random data out	tWHR2	200	-	Ns
CE# low to RE# low	tCR	10	-	Ns
Device resetting time (Read/Program/Erase)	tRST	-	5/10/500	us
Write protect time	tWW	100	-	ns

Notes:
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

2.8 Status Register Coding

I/O	Page Program	Block erase	Read	Cache	Cache Program	Coding
0	Pass / Fail	Pass / Fail	N/A	N/A	Pass / Fail(N)	N page pass : '0' Fail : '1'
1	N/A	N/A	N/A	N/A	Pass / Fail(N-1)	N-1 page pass : '0' Fail : '1'
2	N/A	N/A	N/A	N/A	N/A	-
3	N/A	N/A	N/A	N/A	N/A	-
4	N/A	N/A	N/A	N/A	N/A	-
5	Ready/Busy	Ready/Busy	Ready/Busy	P/E/R Controoler Bit	Ready/Busy	Ready / Busy Busy: '0' Ready: '1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data Cache Ready / Bus y Busy: '0' Ready: '1'
7	Write Protect	Write Protect	Write Protect	N/A	Write Protect	Protected : '0' Not Protected : '1'

Notes:

1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2. I/O1: This bit is only valid for cache program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache program sequence. When Cache program is not supported, this bit is not used.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4. I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the operation is complete.

2.9 Device Identifier Coding

Device Identifier Byte	Description
1st byte	Maker Code
2nd byte	Device Code
3rd byte	Internal chip number, cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
4th byte	Page size, Block size, Spare Size, Organization

2.10 Read ID Data Table

VCC	VCCQ	Bus Width	Maker code	Device Code	3rd	4th
1.8V	1.8V	x8	ADh	A1h	80h	15h

3rd byte of Device Identifier Description

Part Number	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleaved Program Between Multiple die	Not Supported Supported		0 1						
Write Cache	Not Supported Supported	0 1							

4th byte of Device Identifier Description

4th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Number of IO	8 16						0 1		
Serial Access Time	45ns 25ns Reserved Reserved	0 0 1 1				0 1 0 1			
Block Size (Without Spare Area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Organization	x8 x16		0 1						

3. Timing Diagram

Bus Operation
There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. Typically glitches less than 5ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

3.1 Command Latch Cycle Timings

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high.

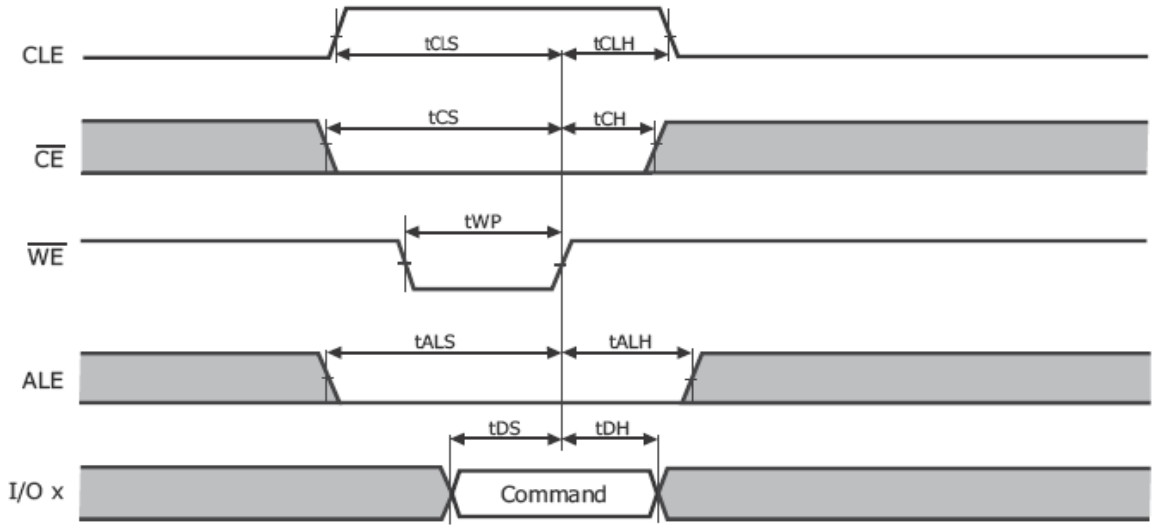


Figure 9 : Command latch timings

Note:
All command except Reset, Read Status is issued to command register on the rising edge of /WE, when CLE is high, CE# and ALE is low, and device is not busy state.

3.2 Address Latch Cycle Timings

Address Input bus operation allows the insertion of the memory address. To insert the 27 (x8 Device) or 26 (x16Device) addresses needed to access the 1Gbit 4 clock cycles are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation(write/erase) the Write Protect pin must be high.

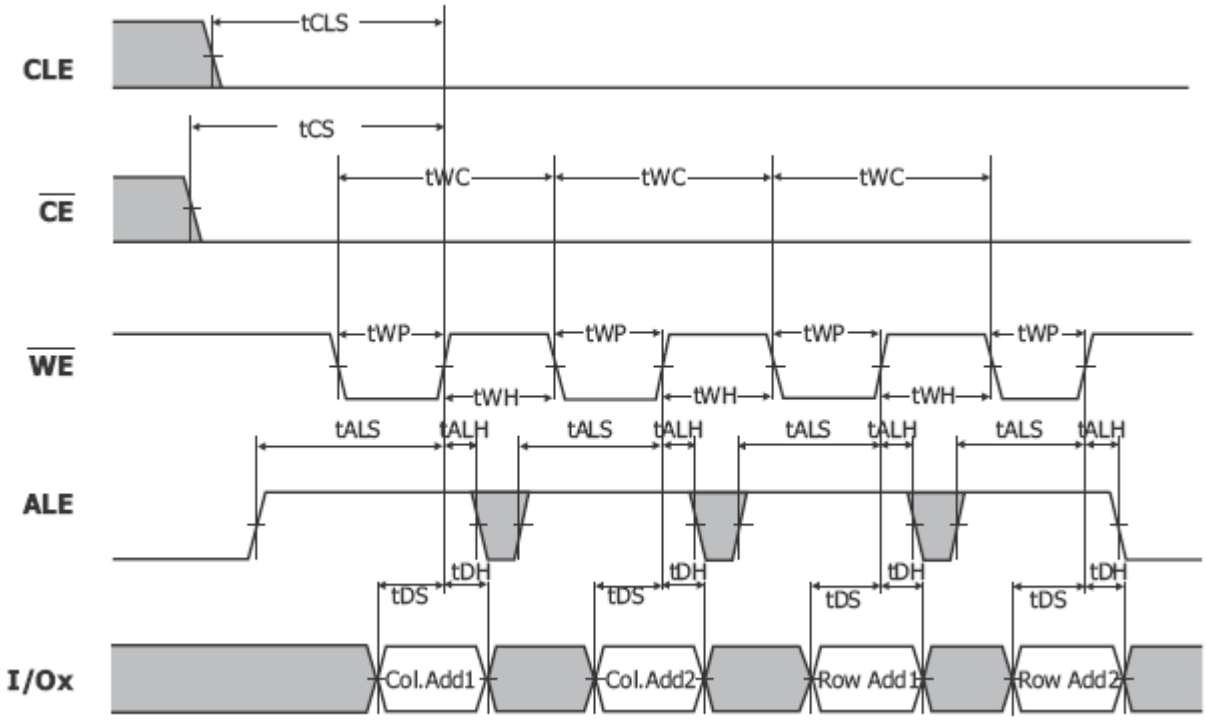


Figure 10 : Address latch timings

3.3 Data Input Cycle Timings

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

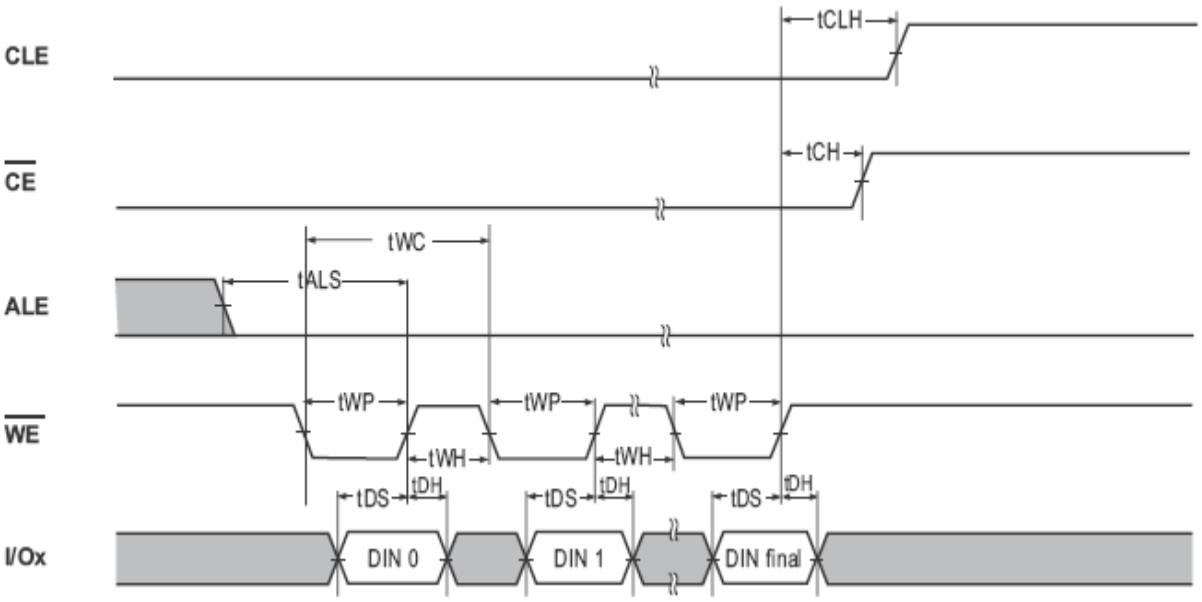


Figure 11 : Data Input cycle timings

Note:
Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

3.4 Data Output Cycle Timings (CLE=L, WE#=H, ALE=L, WP#=H)

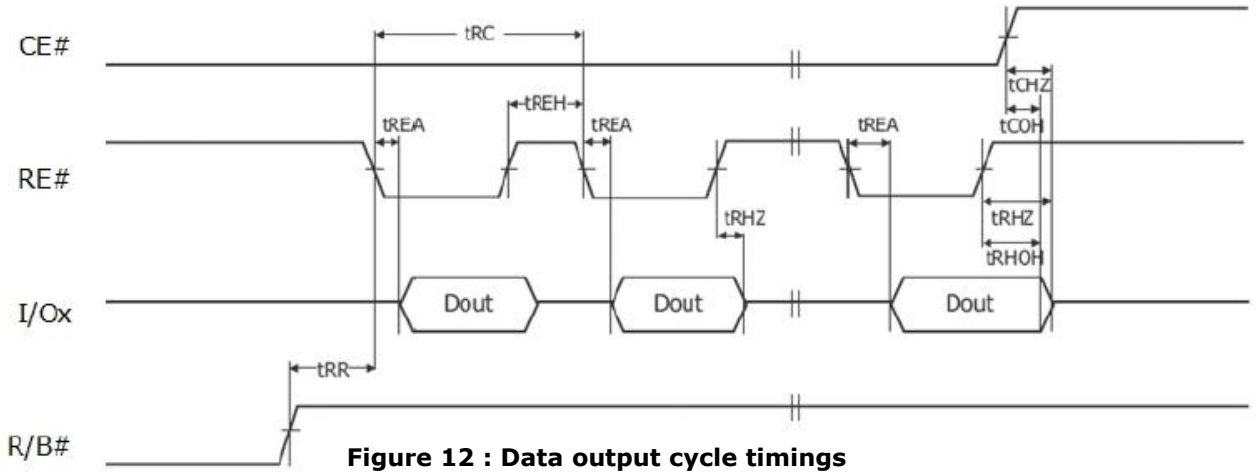


Figure 12 : Data output cycle timings

Notes:
1. Transition is measured at +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRHOH is valid when frequency is lower than 33 MHz.

3.5 Data Output Cycle Timings (EDO type, CLE=L, WE#=H, ALE=L)

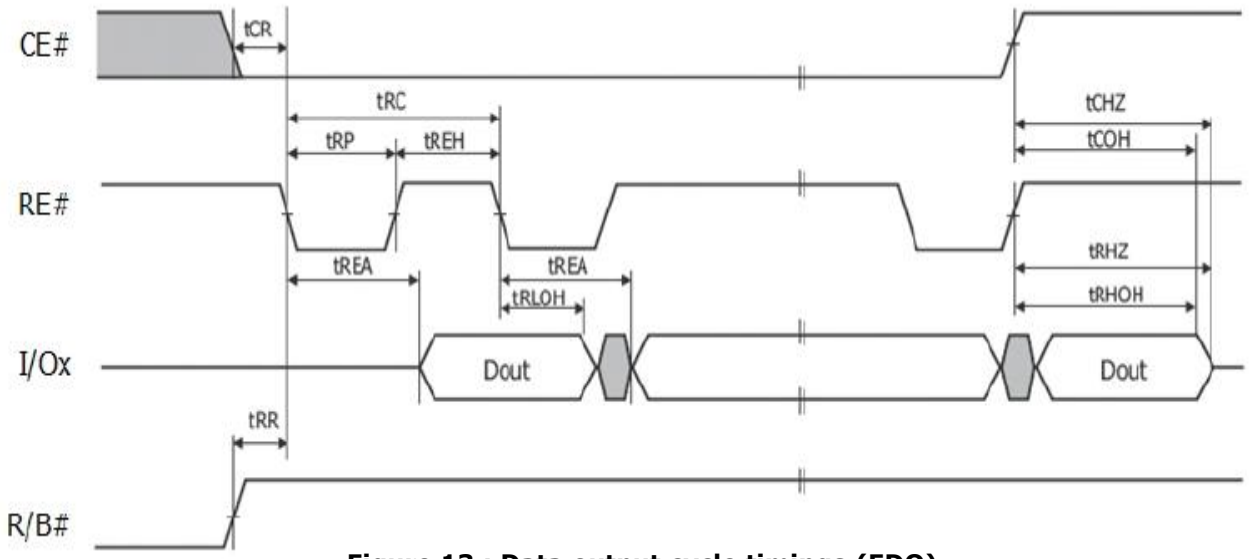


Figure 13 : Data output cycle timings (EDO)

Notes:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRLOH is valid when frequency is higher than 33 MHz. tRHOH starts to be valid when frequency is lower than 33 MHz.

3.6 Read Status Cycle Timings

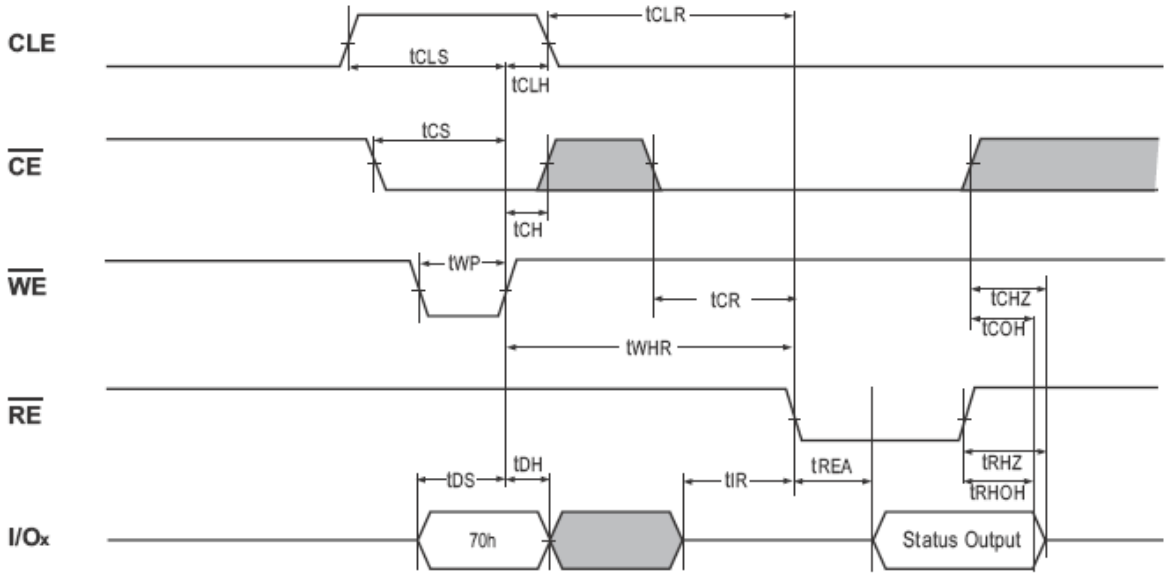


Figure 14 : Read Status timings

3.7 Page Read Operation Timings (Read One Page)

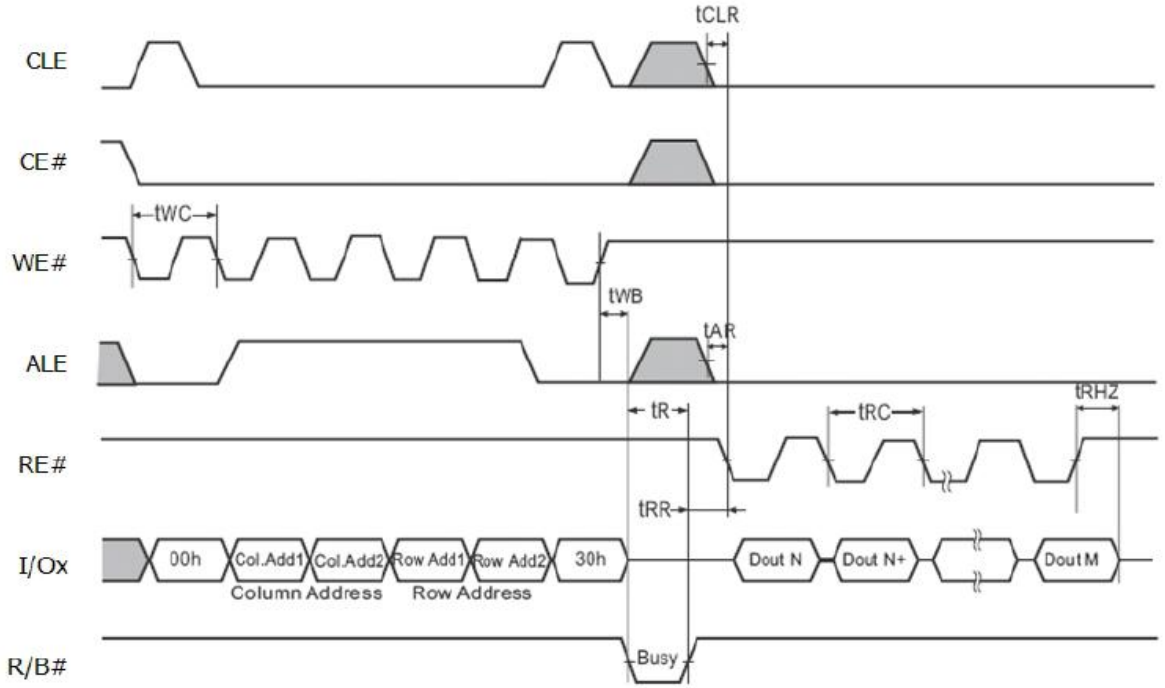


Figure 15 : Page Read Operation timings

3.8 Page Read Operation Timings (Intercepted by CE#)

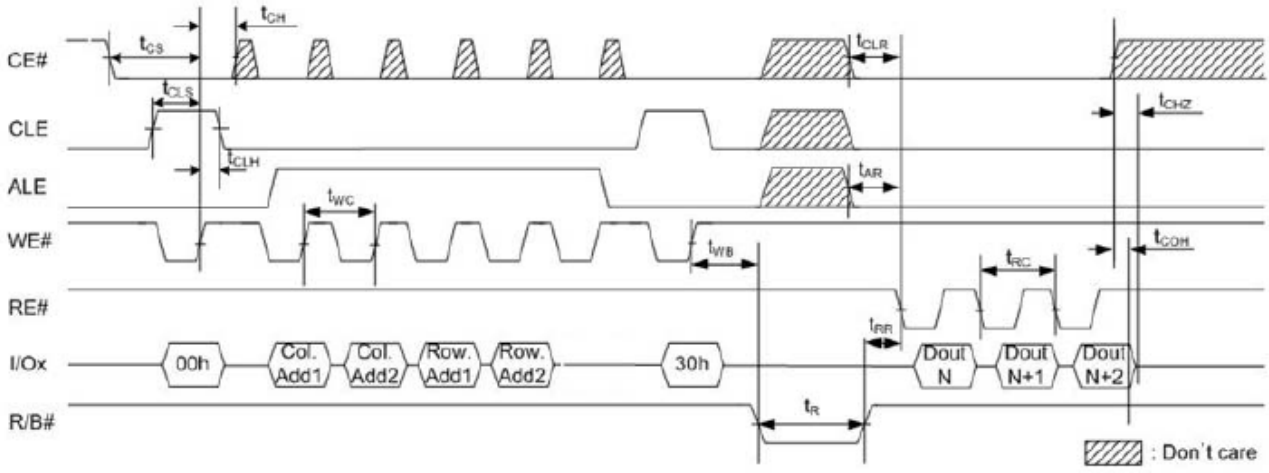


Figure 16 : Page Read Operation timings (Intercepted by CE#)

3.9 Page Read Operation Timings with CE# don't care

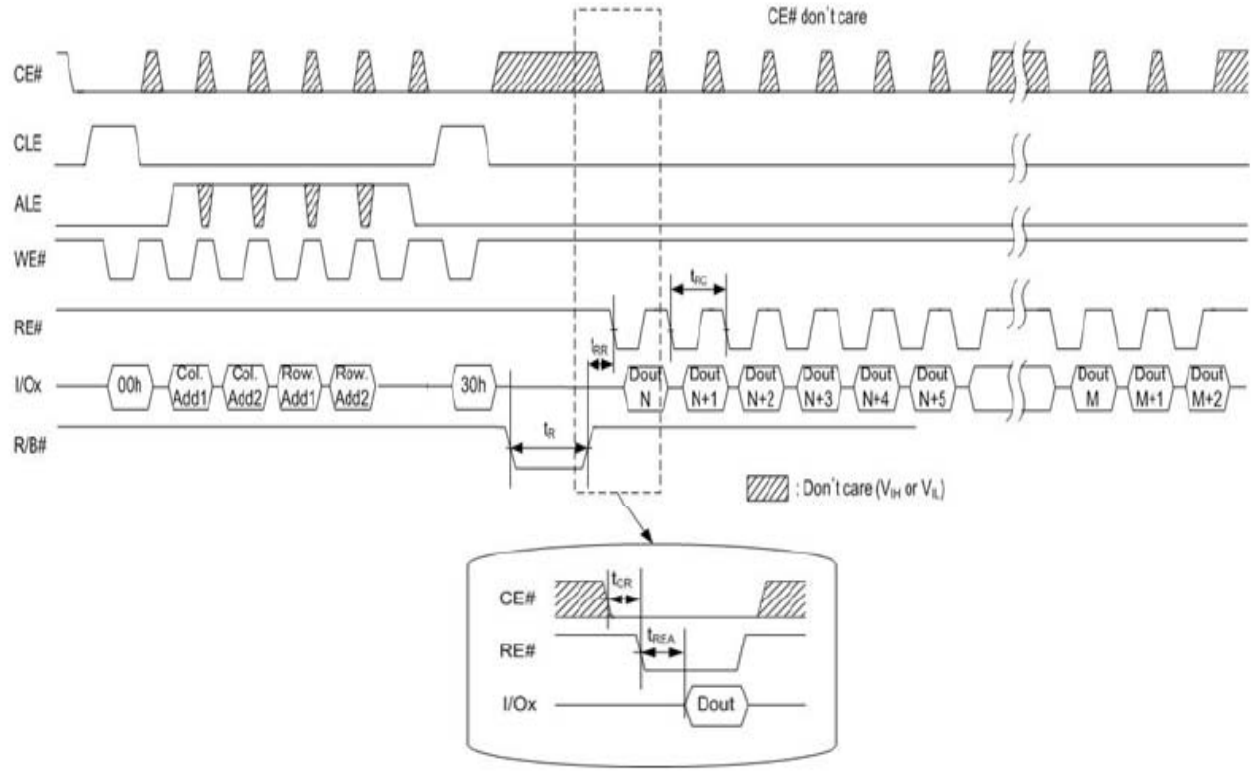


Figure 17 : Page Read Operation Timings with CE# don't care

3.10 Random Data Output Timings

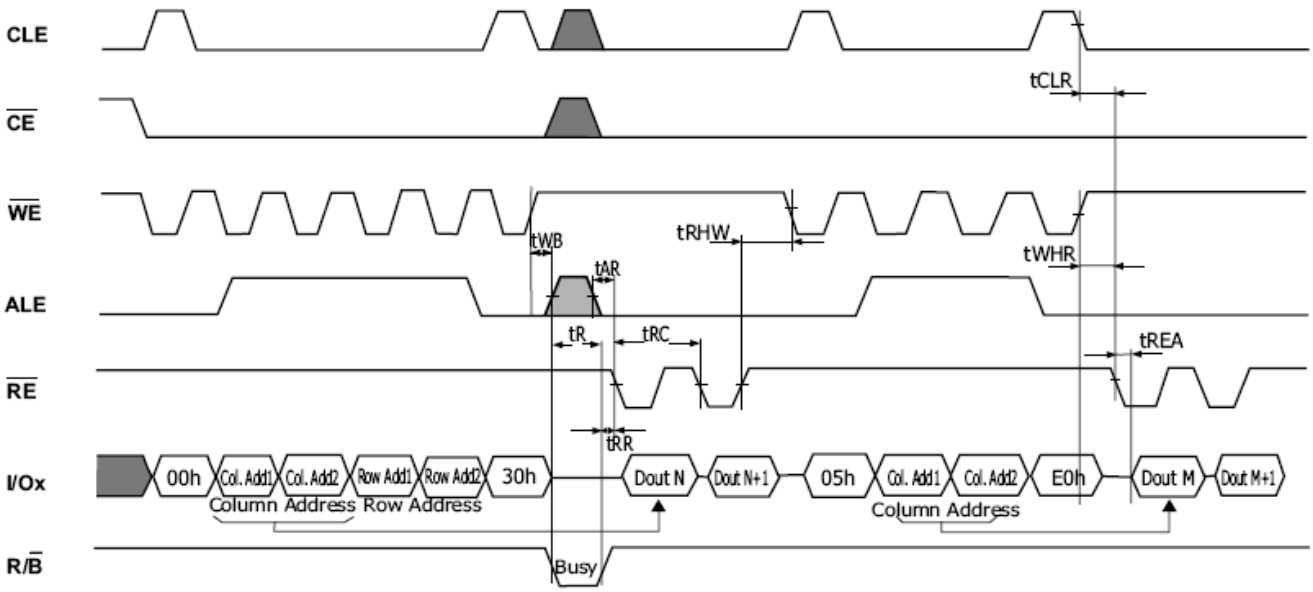


Figure 18 : Random data output timings

3.11 Cache Read Operation Timings

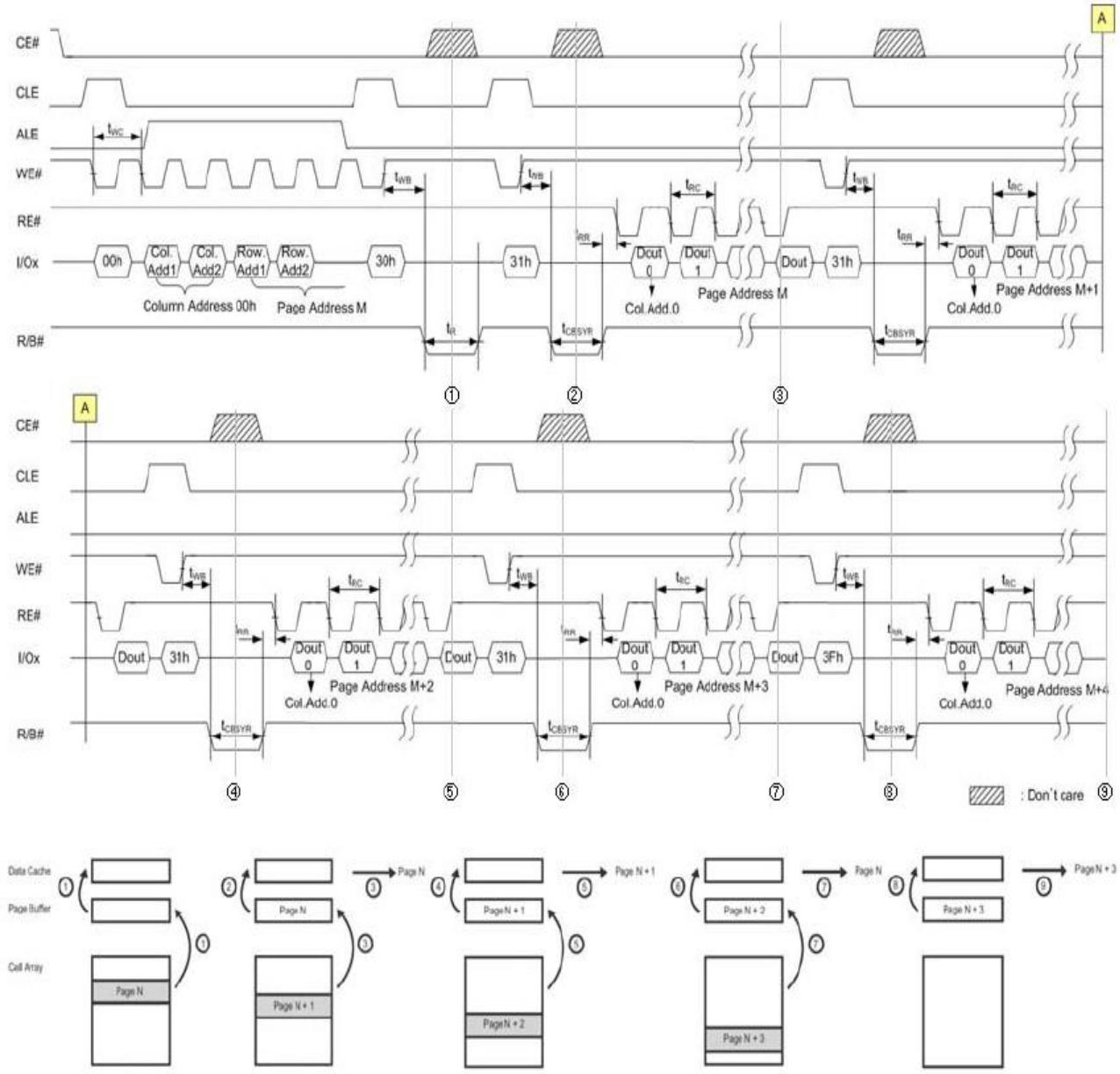


Figure 19 : Cache Read Operation Timings

3.12 Read ID Operation Timings

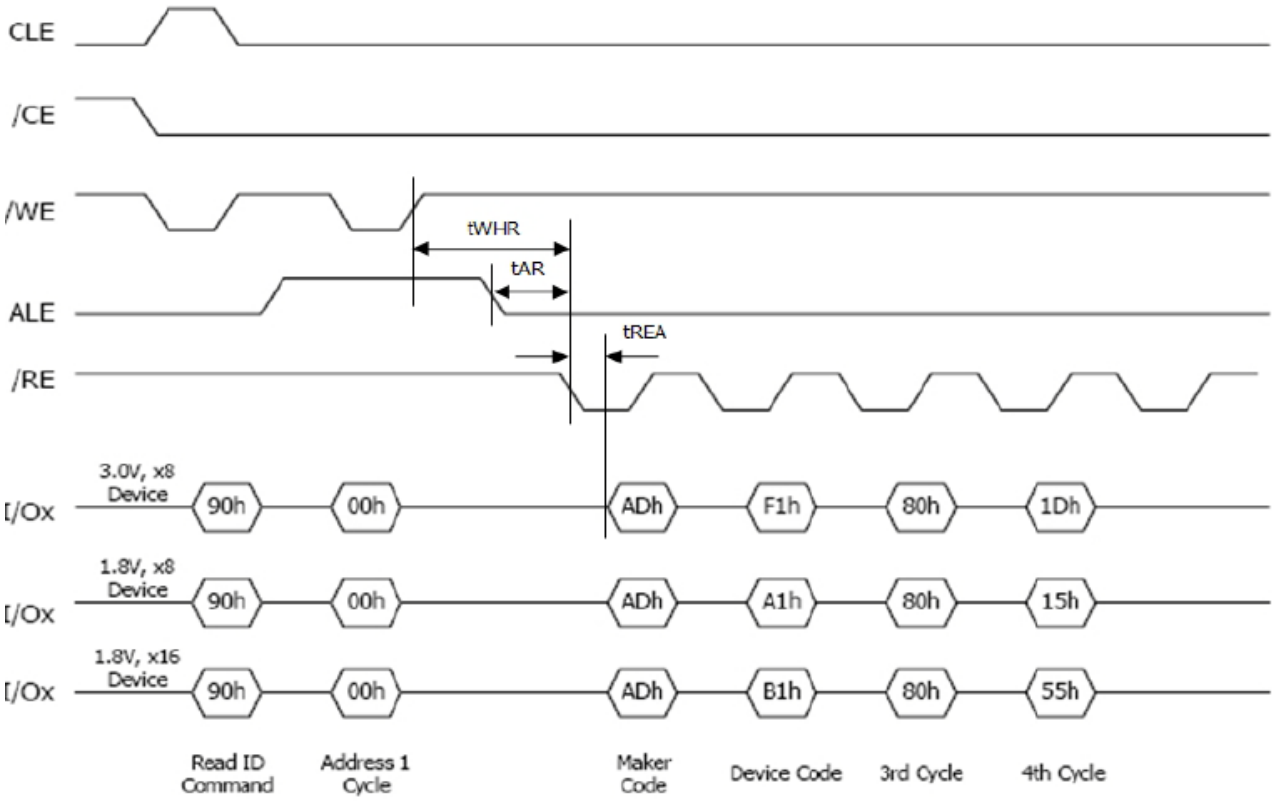


Figure 20 : Read ID operation timings

3.13 Page Program Operation Timings

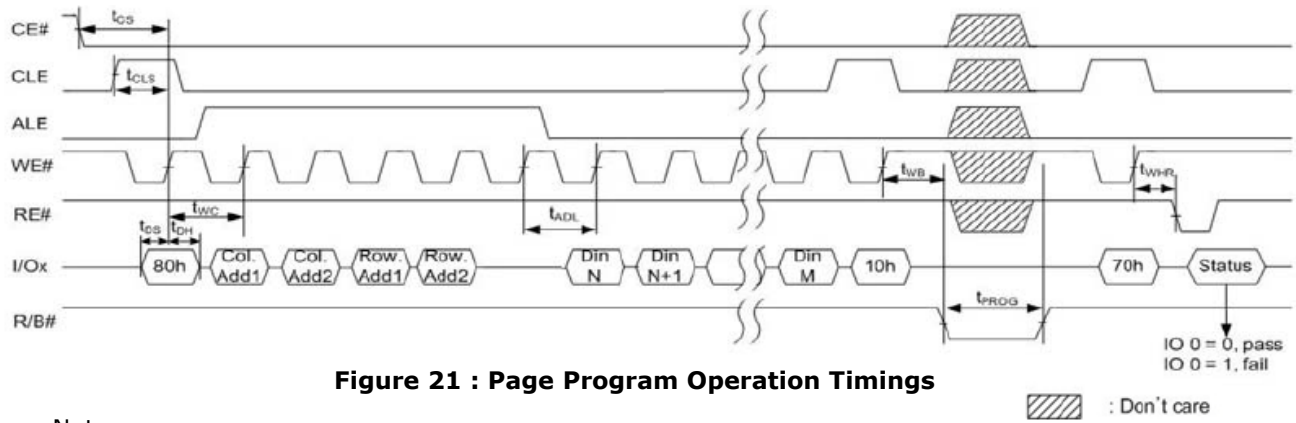


Figure 21 : Page Program Operation Timings

Notes:
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

3.14 Page Program Operation Timings with CE# don't care

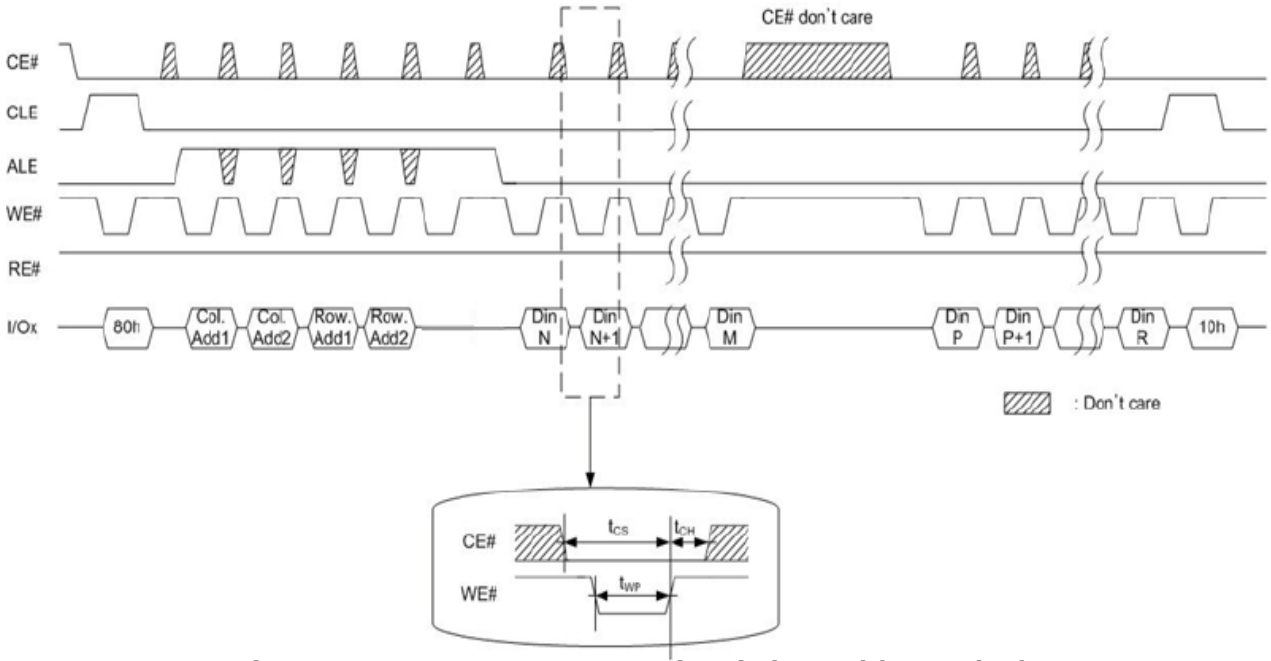


Figure 22 : Page program operation timings with CE# don't care

Notes:
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

3.15 Random Data Input Timings

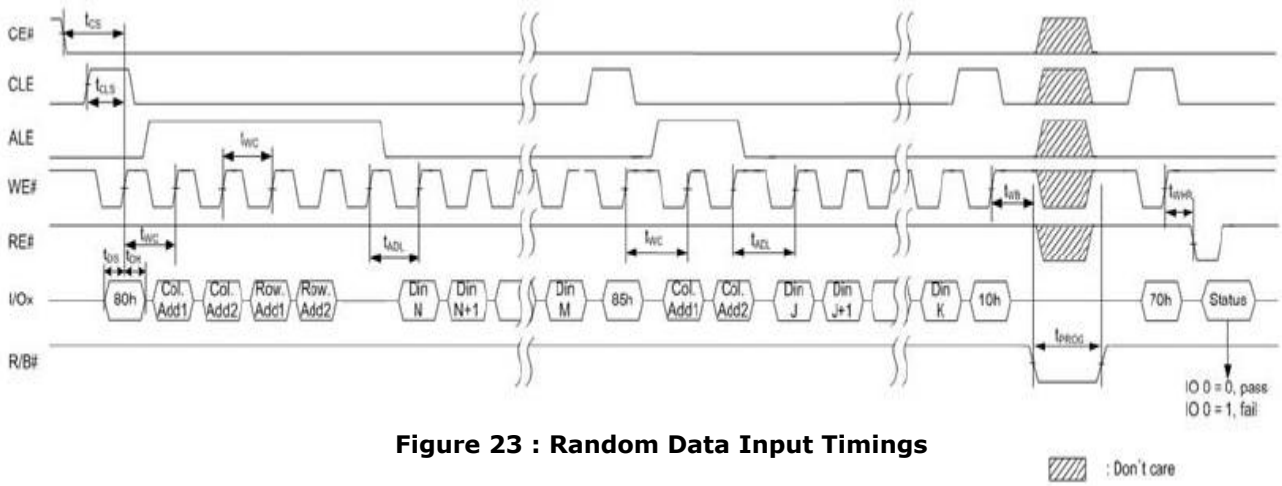


Figure 23 : Random Data Input Timings

Notes:
1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
2. Random data input can be performed in a page.

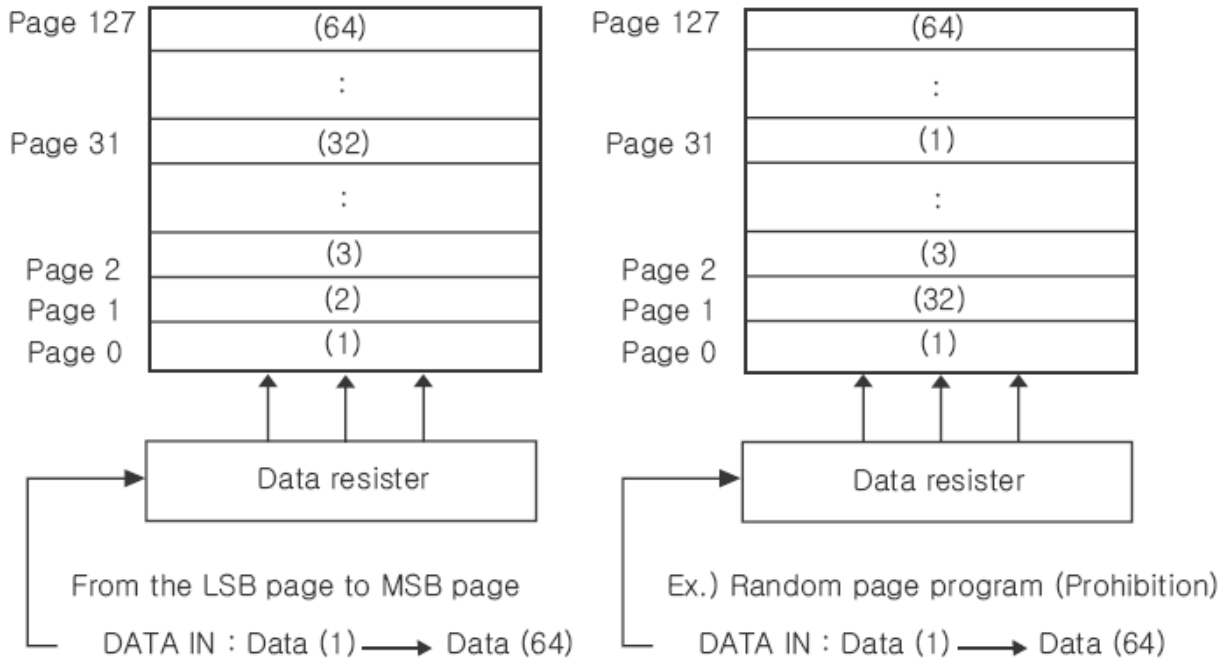


Figure 24 : Page Programming within a block

Note : Both programming methods can be used. However, we recommend sequential page programming

3.16 Copy-Back Program Operation Timings with Random Data Input

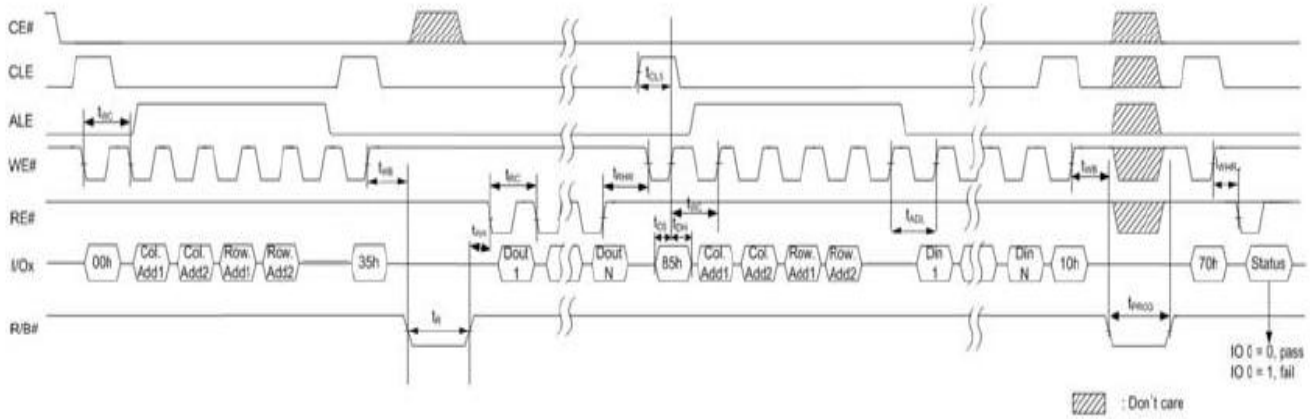


Figure 25 : Copyback program operation timing with random data input

Note:
tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

3.17 Cache Program Operation Timings

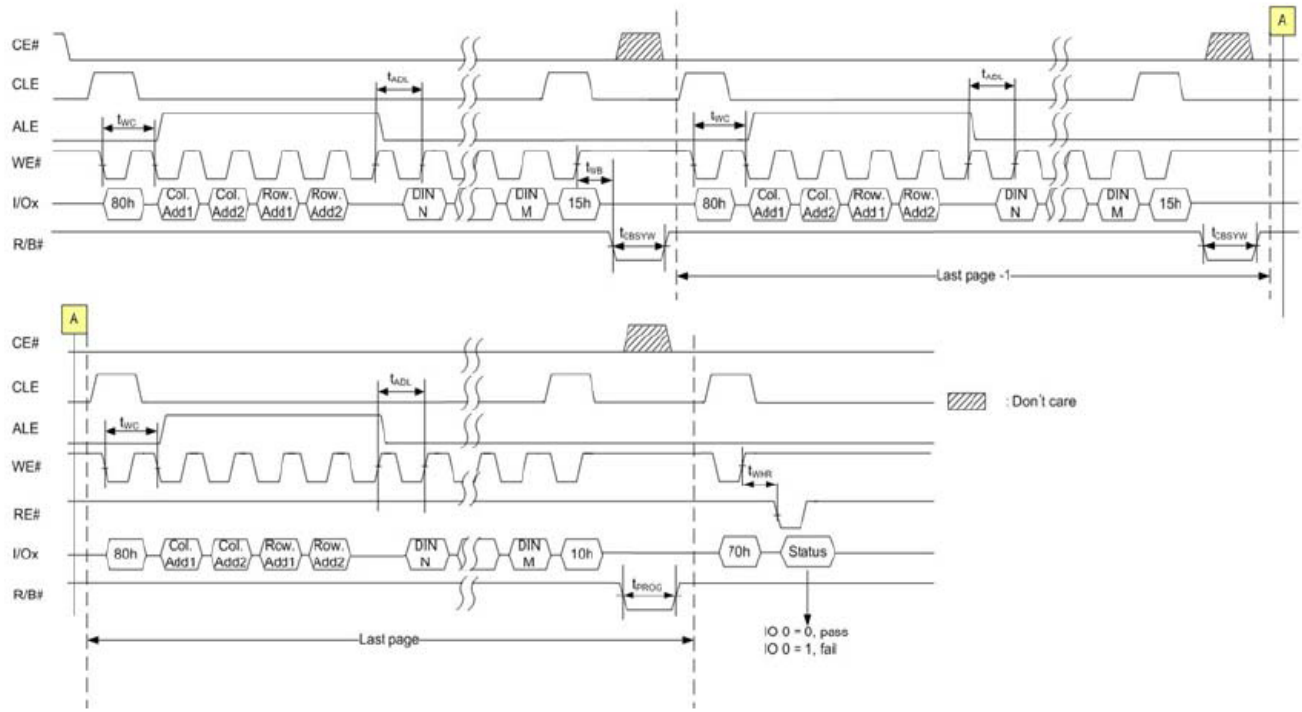


Figure 26 : Cache program operation timings

Note:
tPROG = Program time for the page + Program time for the (-1)th page
- (command input cycle time + address input cycle time + page data loading time)

3.18 Block Erase Operation Timings

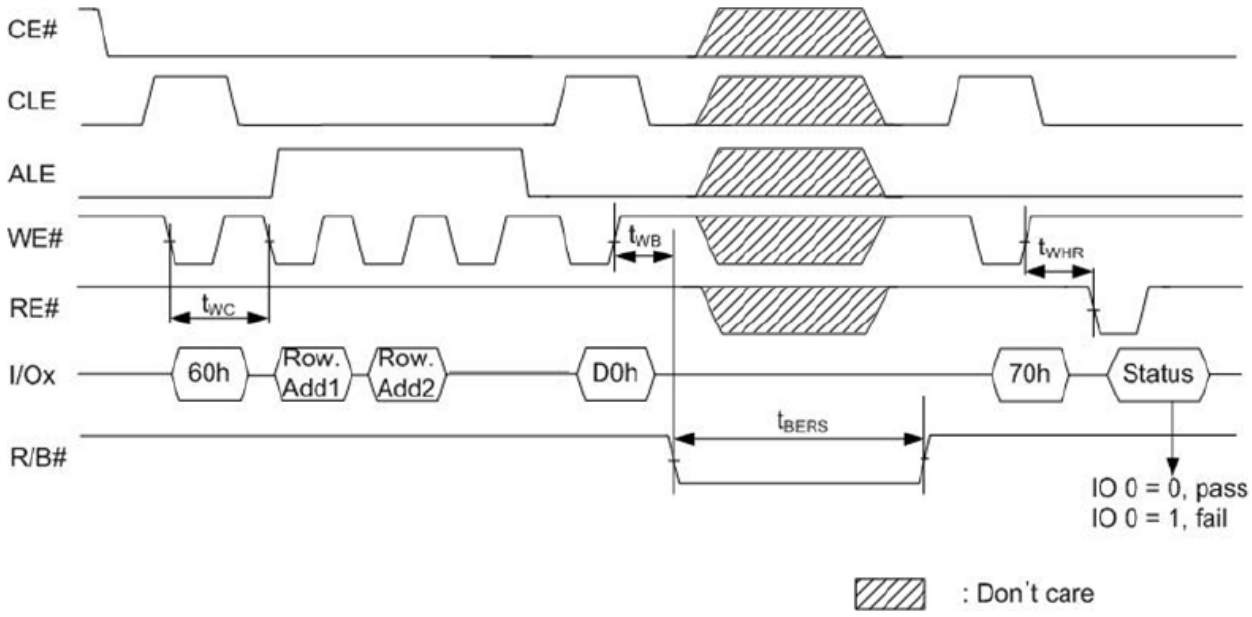


Figure 27 : Block erase operation timings

3.19 Reset Timings

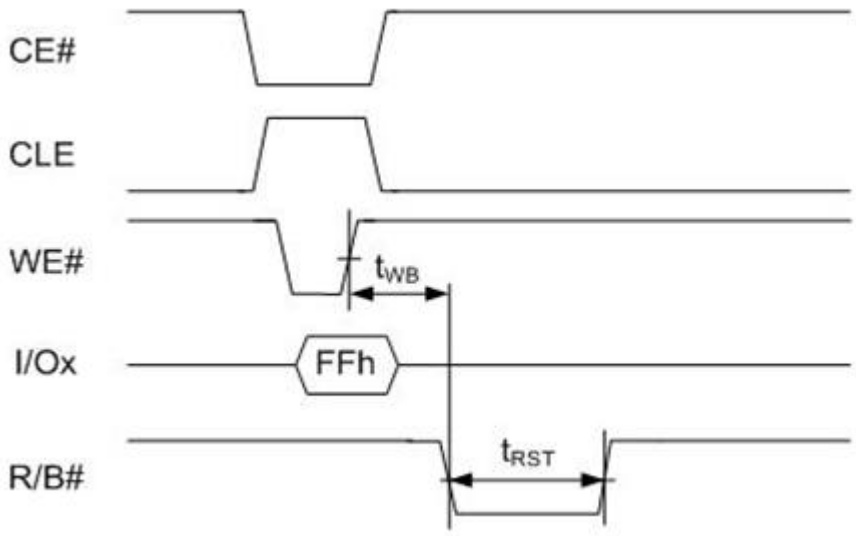


Figure 28 : Reset timings

4. Device Operation

4.1 Page Read

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h and 30h to the command register along with four address cycles. In two consecutive read operations, the second one does need 00h command, which four address cycles and 30h command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command. Two types of operations are available: random read , serial page read. The random read mode is enabled when the page address is changed. The 2112 Bytes(x8 Device) or 1056 Words(x16 Device) of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns (3V version) and 45ns (1.8V version) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the column address. The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page. After power up, device is in read mode so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode. Check Figure14~17 as references.

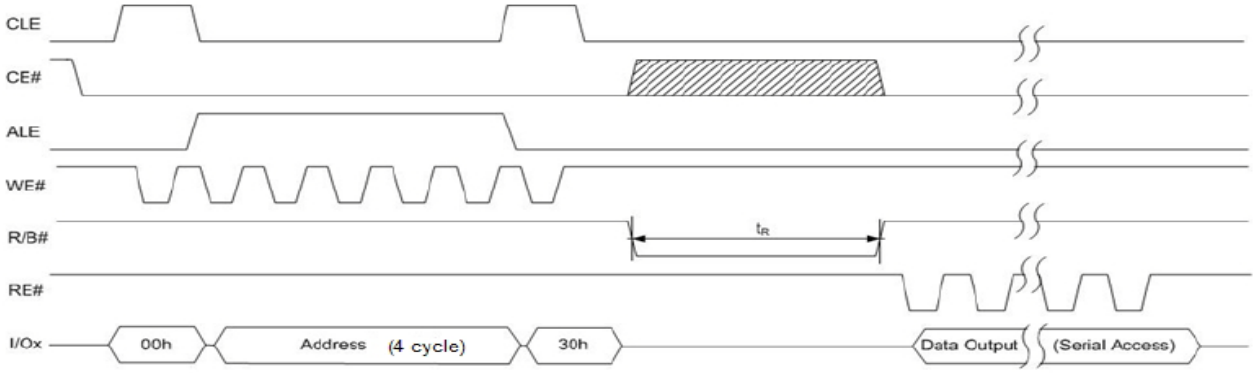


Figure 29 : Page read

Random data output

Random data output operation changes the column address from which data is being read in the page register. Random data output only is issued in Ready state. Refer to Figure 30.

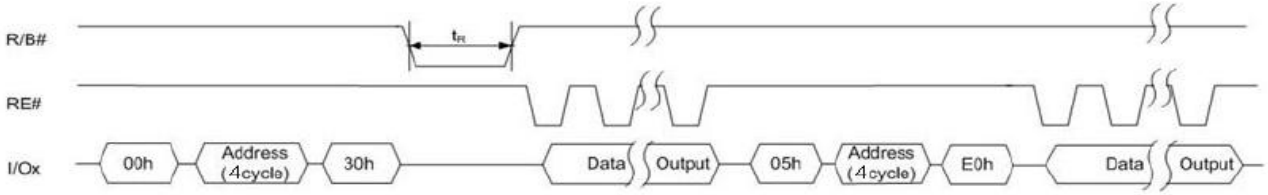


Figure 30 : Random data output

4.2 Cache Read (available only within a block)

The Cache read function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in Section 4.1, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence. The Cache read function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache read function. Issuing an additional Cache read function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command.
The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a sequential Cache read (31h) command after the page of the device is read. Figure19 defines the Cache read behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register.

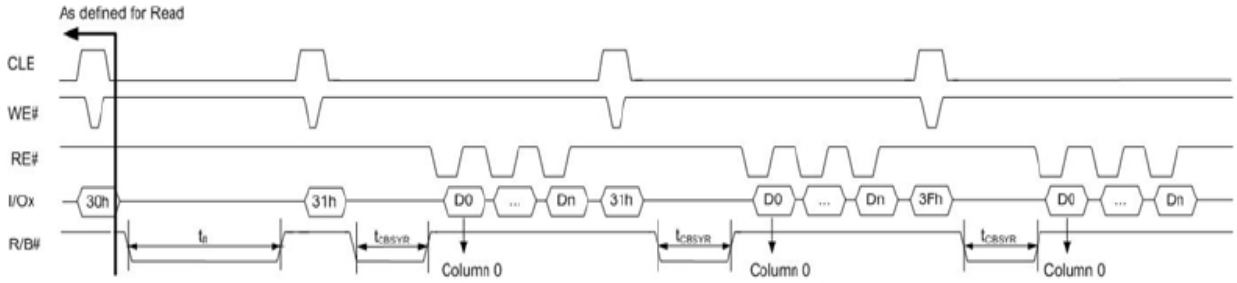


Figure 31 : Cache read

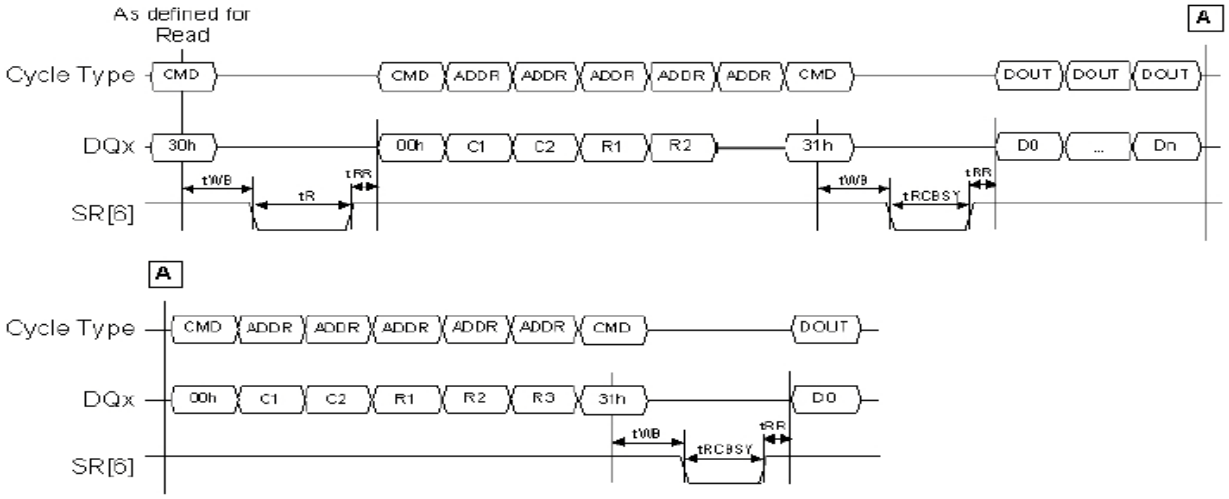


Figure 32 : Cache read Random (Start of the cache operation)

Note:
C1-C2 : Column address of the page to retrieve. C1 is the least significant byte. The column address is ignored.
R1-R3 : Row address of the page to retrieve. R1 is the least significant byte.
D0-Dn : Data bytes/words read from page requested by the original Read or the previous cache operation.

4.3 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

4.3.1 Legacy Read ID

Four read cycles sequentially output the manufacturer code (ADh), and the device code and 80h, 4th cycle ID, respectively.
The command register remains in Read ID mode until further commands are issued to it.
Figure20 shows the operation sequence.

4.4 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing-sand other behavioral parameters. Figure 33 defines the Read Parameter Page behavior. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. The whole data structure is repeated at leat three times.
The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page. The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow fort he Read Parameter Page command.
Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

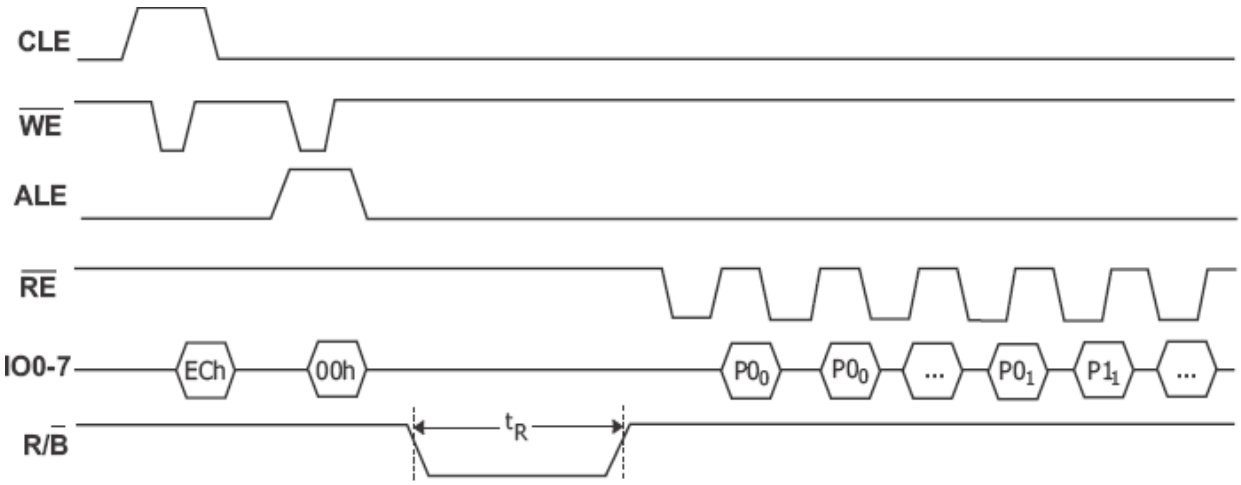


Figure 33 : Read Parameter Page timings

Byte	O/M	Description	Values
Revision Information and Features Block			
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	X8 : 14h,00h X16 : 15h, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command	33h, 00h
10-31		Reserved (0)	00h
Manufacturer Information Block			
32-43	M	Device manufacturer (12 ASCII characters)	48h, 59h, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	48h, 32h, 37h, 53h, 31h, 47h, 38h, 46h, 32h, 43h, 46h, 52h, 2Dh, 42h, 43h, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC manufacturer ID	ADh
65-66	O	Date Code	00h
67-79		Reserved(0)	00h

Memory Organization block			
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	40h, 00h
86-89	M	Number of data bytes per partial page	00h, 00h, 00h, 00h
90-91	M	Number of spare bytes per partial page	00h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	00h, 04h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	22h
102	M	Number of bits per cell	01h
103-104	M	blocks maximum per LUN	20h, 00h
105-106	M	Block endurance	05h, 04h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	05h, 04h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	04h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00h
115-127		Reserved (0)	00h

Electrical parameters block			
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	03h, 00h
131-132	O	Program cache timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0,	03h, 00h
133-134	M	tPROG Maximum page program time (μs)	BCh, 02h
135-136	M	tBERS Maximum block erase time (μs)	10h, 27h
137-138	M	tR Maximum page read time (μs)	19h, 00h
139-140	M	tccs Minimum Change Column setup time (ns)	3Ch, 00h
141-163		Reserved (0)	00h
Vendor block			
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
Redundant Parameter Pages			
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Table 9: Parameter Page Description

NOTE: "O" Stands for Optional, "M" for Mandatory

4.5 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values.
Figure 34 shows the operation sequence.

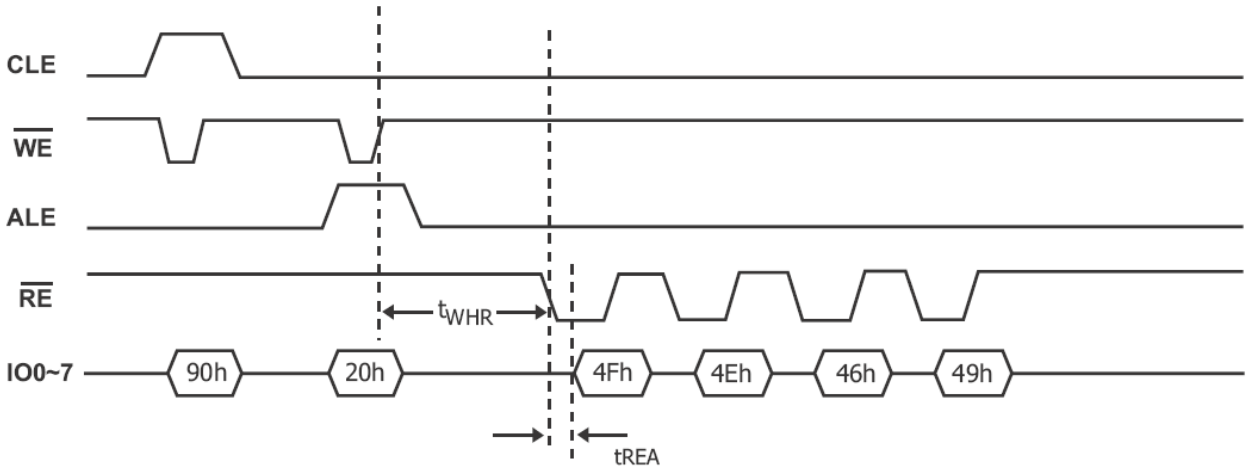


Figure 34: ONFI signature timing diagram

4.6 Parameter Page Data Structure Definition

Table18 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (assign an 8-bit data access device). For example, the chip will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.For more detailed information about Parameter Page Data bits.

4.7 Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs . This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status.
The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

4.8 Page Program

The device is programmed basically by page, but it does allow multiple partial page programming of a words (1 to 1056) or consecutive bytes up to (1 to 2112), in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4; for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte). A page program cycle consists of a serial data loading period in which up to 2112 bytes(x8 Device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the four cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process.
Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit (I/ O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure35~36 detail the sequence.

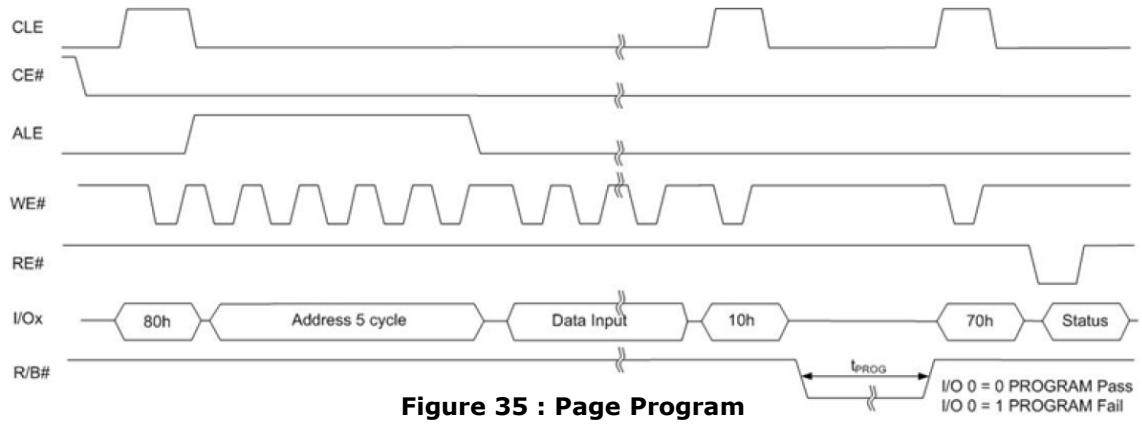


Figure 35 : Page Program

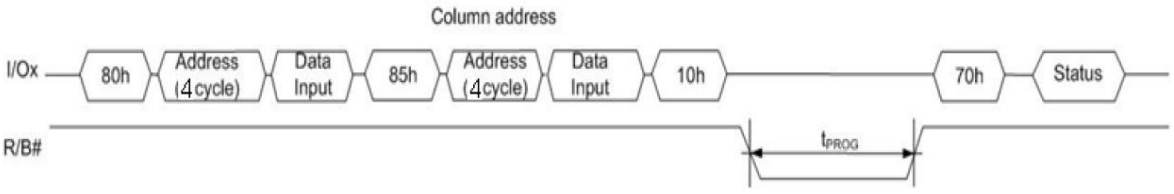


Figure 36 : Random data input

4.9 Cache Program (available only within a block)

Cache Program is used to improve the program throughput by programing data using the cache register. The cache program operation can only be used within one block. The cache register allows new data to be input while the previous data that was transfered to the page buffer is programmed into the memory array. Cache program is available only within a block. After the serial data input command (80h) is loaded to the command register, followed by 4 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state For a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h). The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model. In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCB-SYW). Read Status commands (70h) may be issued to check the status of the different registers, and the pass/ fail status of the cached program operations. More in detail:

a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b) the status bit I/O<5> can be used to determine

when the cell programming of the current data register contents is complete.
c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1" .
d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N.
The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the programming is finished before starting any other operation.

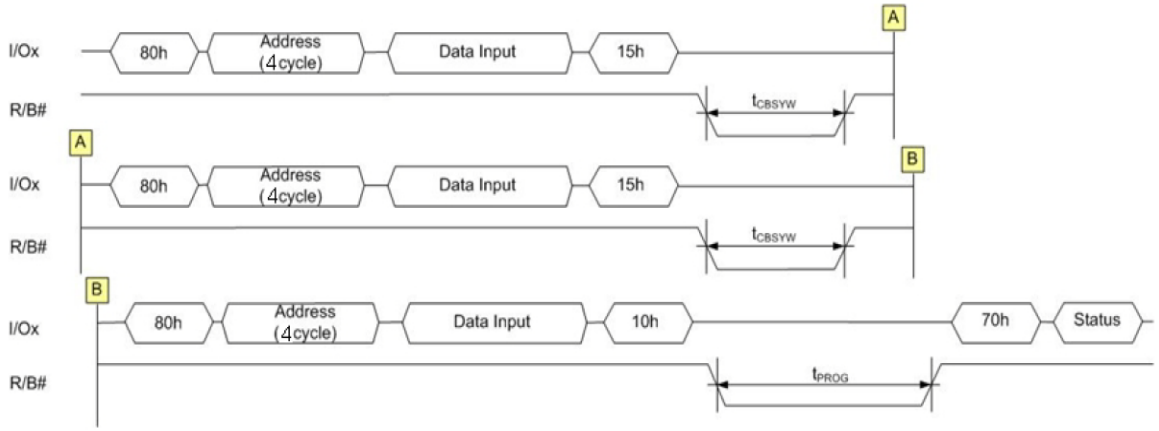


Figure 37-1 : Cache program

Pass/Fail status for each page programmed by the Cache Program operation can be detected by the Read Status operation.
- I/O 0 : Pass/Fail of the current page program operation.
- I/O 1 : Pass/Fail of the previous page program operation.

The Pass/Fail status on I/O 0 and I/O 1 are valid under the following conditions.
- Status on I/O 0 : Ready/Busy is Ready state.

The Ready/Busy is output on I/O 5 by Read Status operation or R/B pin after the 10h command.
- Status on I/O 1 : Data Cache Ready /Busy is Ready State.

The Data Cache Ready/Busy is output on I/O 6 by Read Status operation or R/B pin after the 15h command.

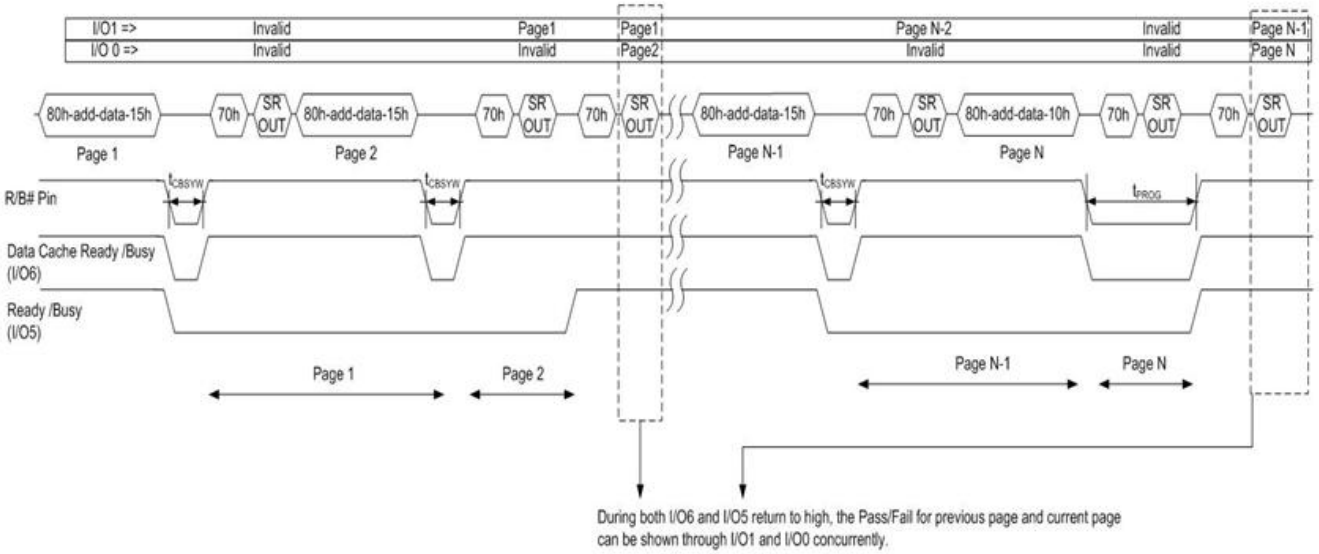


Figure 37-2 : Cache program

4.10 Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112 bytes(x8 Device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure25 "Copy Back Program with Random Data Input". "When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/ correction scheme. For this reason, four bit error correction is recommended for the use of Copy-Back operation. Figure37 shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy back, while it must be set to Vcc When performing the program.

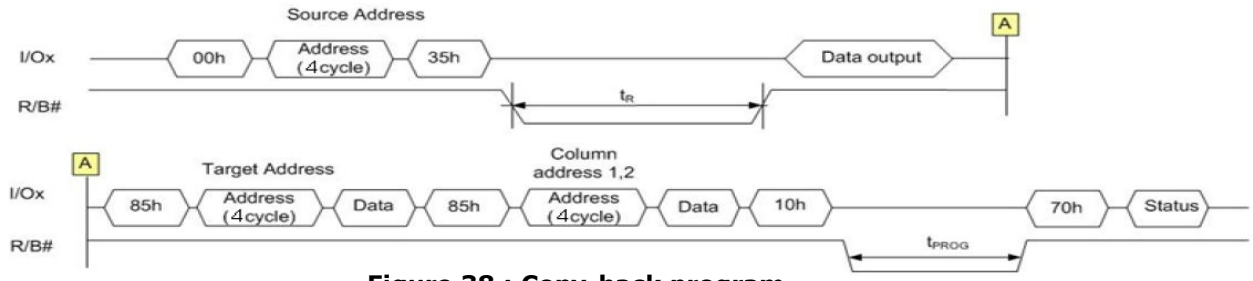


Figure 38 : Copy-back program

4.11 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A18 to A27 is valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of an erase by monitoring the R/B output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. (Figure27 details the sequence.)

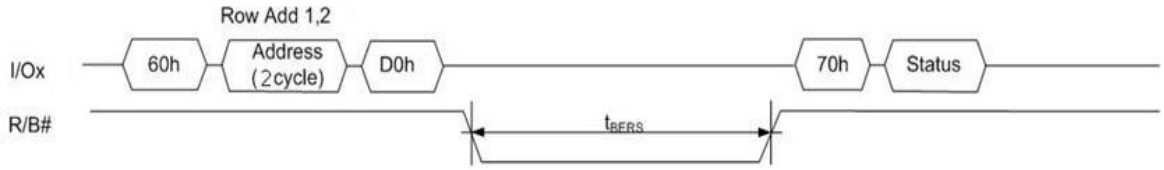


Figure 39 : Block Erase

4.12 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to Table "Status Register Coding" for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B# pin transitions to low for 8 after the Reset command is written (Figure28 details the sequence.)

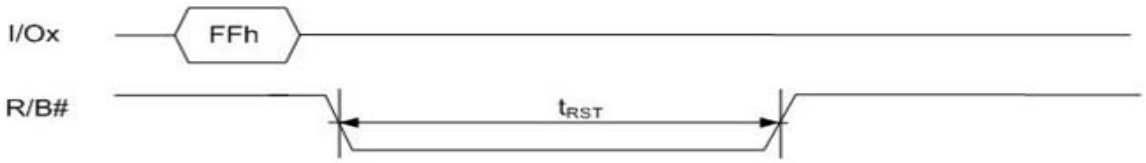


Figure 40 : Reset

4.13 Page Re-program

In above section the feature of page program was explained. In that section, it was also highlighted that page program may result in a fail, which can be detected by Read Status Register.
In this event, the 1Gbit F32 SLC implements the innovative feature of "page re-program". This command allows the reprogramming of the same pattern of the (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the page, the program confirm can be issued (10h) without any data input cycle (as described in Figure 41).

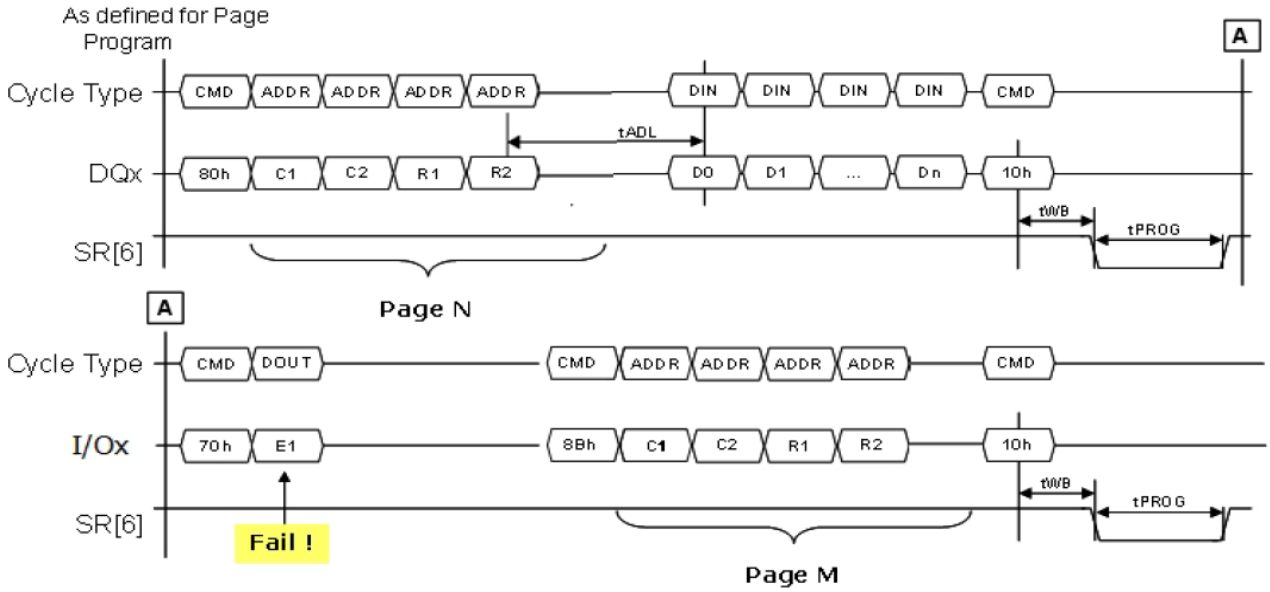


Figure 41 : Page Re-program

On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm "10h" (as described in Figure 42)

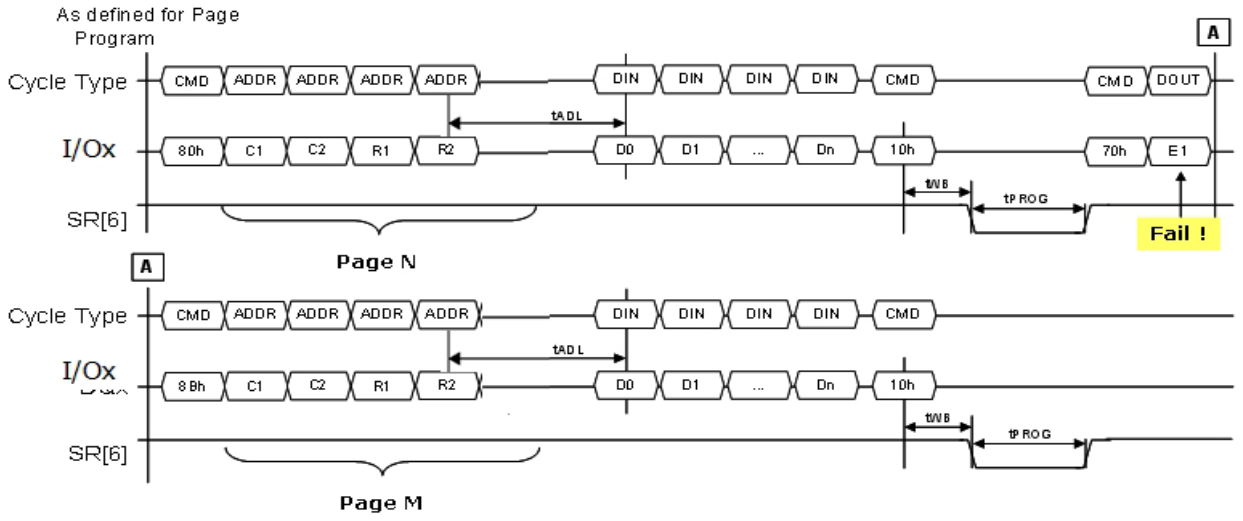


Figure 42 : Page reprogram with data manipulation

The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The “program confirm” command (10h) initiates the re-programming process.
The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

5. Other Features

5.1. Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.1 V (1.8 V Device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power down.
A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 44. The two-step command sequence for program/erase provides additional software protection.

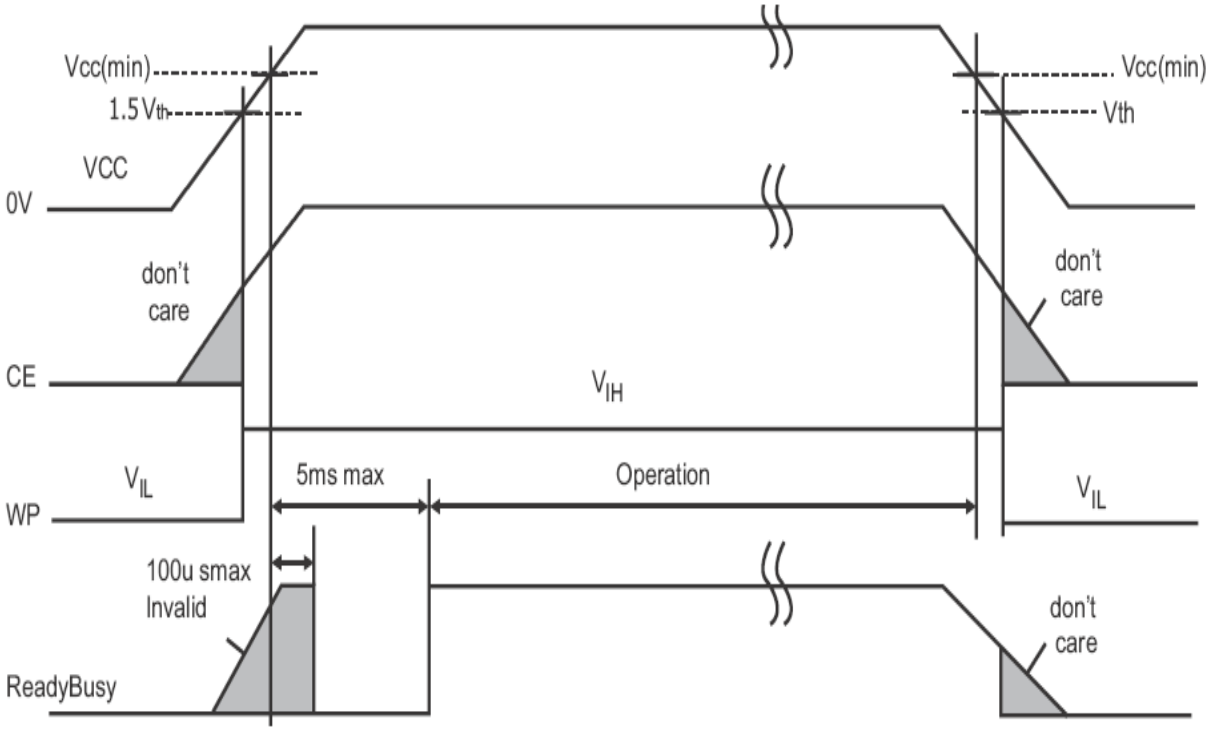
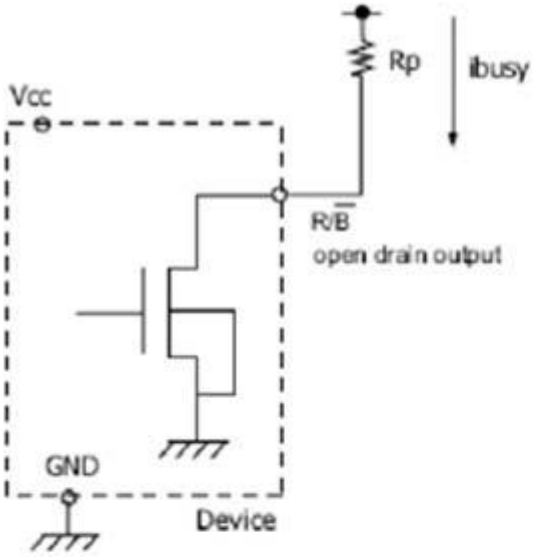


Figure 44 : Data protection and Power on/off(1.8V Device)

5.2. Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation.
The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart.



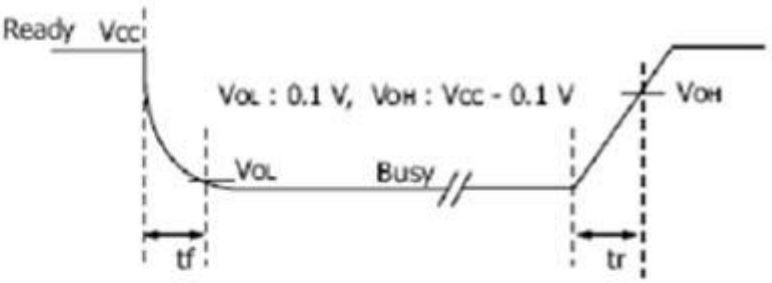
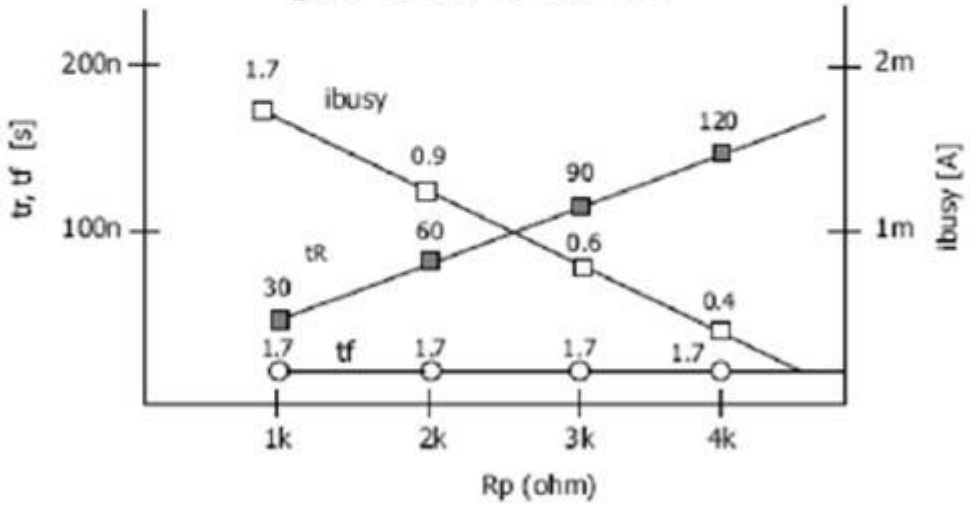


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 1.8 V, Ta = 25 °C, CL = 30 pF



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \Sigma IL} = \frac{1.85\ V}{3\ mA + \Sigma IL}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 46 : Ready/Busy Pin Electrical Specifications (1.8V Device)

5.3. Write Protect Operation

The Erase and Program Operations are automatically reset when WP# goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows(Figure47~50)

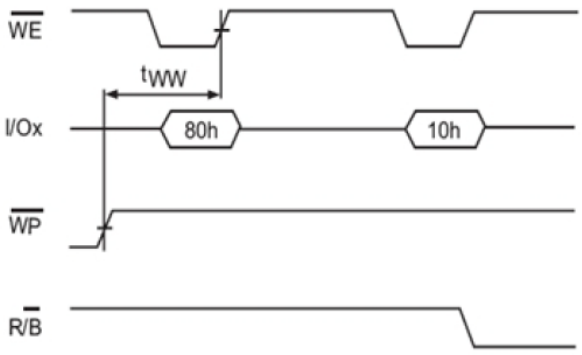


Figure 47 : Enable Programming

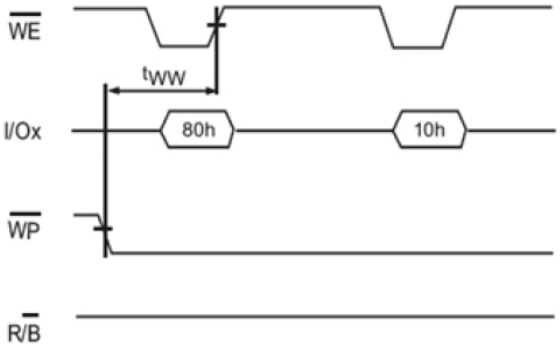


Figure 48 : Disable Programming

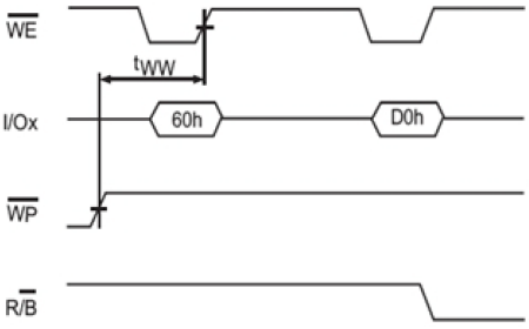


Figure 49 : Enable Erasing

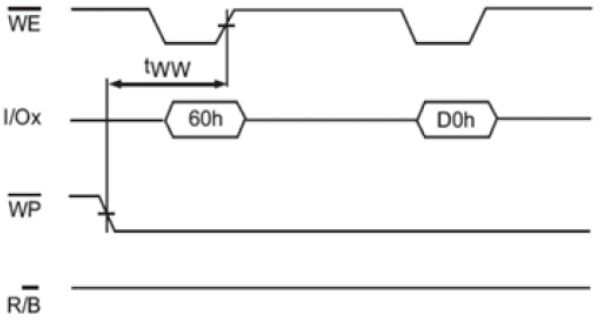


Figure 50 : Disable Erasing

5.4. Stand-by

In Stand-by the device is deselected, Outputs are disable and power consumption reduced.