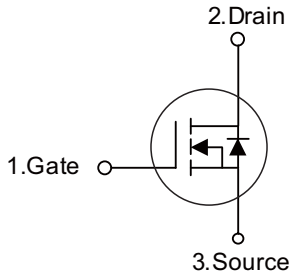
■ PRODUCT CHARACTERISTICS

VDSS	30V
R_{DS}(on)max(@V_{GS} =4.5 V)	5.6mΩ
R_{DS}(on)max(@V_{GS} =10 V)	3.6mΩ
ID	90A

Symbol



■ DESCRIPTION

This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

■ FEATURES

* $R_{DS(on)}$*Q_g industry's benchmark
* Conduction losses reduced
* Switching losses reduced
* Low threshold device

TO-252

■ ORDER INFORMATION

Order codes		Package	Packing
Halogen-Free	Halogen		
N/A	MOT90N03D	TO-252	2500 pieces /Reel
N/A	MOT90N03C	TO-251	70 pieces/Tube

■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}= 0)	30	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_C = 25°C	90	A
I_D	Drain current (continuous) at T_C=100°C	72	A
I_{DM}(2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25°C	95	W
	Derating factor	0.63	W/°C
E_{AS}(3)	Single pulse avalanche energy	350	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

■ THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.58	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	100	°C/W
T_j	Maximum lead temperature for soldering purpose	275	°C

1. Value limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting T_j = 25°C, I_D =40A, V_{DD} =15V

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250μA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 30V			1	μA
		V_{DS} = 30V, Tc=125°C			10	μA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250μA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 40A		3.6	4.5	mΩ
		V_{GS}= 5V, I_D= 40A		5.6	8	
C_{iss}	Input capacitance	V_{DS} =25V, f=1MHz, V_{GS}=0		2805		pF
C_{oss}	Output capacitance			549		pF
C_{rss}	Reverse transfer capacitance			76		pF
Q_g	Total gate charge	V_{DD}=15V, I_D = 80A		22	32	nC
Q_{gs}	Gate-source charge	V_{GS} =5V		10		nC
Q_{gd}	Gate-drain charge	*(see Figure 13)*		7		nC
R_G	Gate input resistance	f=1MHz Gate Bias Bias=0 Test Signal Level=20mV open drain		1.2		Ω
$t_{d(on)}$	Turn-on delay time	V_{DD}=15V, I_D=40A, R_G=4.7Ω, V_{GS}=5V *(see Figure 12)*		19		ns
t_r	Rise time			135		ns
$t_{d(off)}$	Turn-off delay time	V_{DD}=15V, I_D=40A, R_G=4.7Ω, V_{GS}=5V *(see Figure 12)*		24		ns
t_f	Fall time			33		ns
I_{SD}	Source-drain current				80	A
I_{SDM}(1)	Source-drain current (pulsed)				320	A
V_{SD}(2)	Forward on voltage	I_{SD}=40A, V_{GS}=0			1.3	V
t_{rr}	Reverse recovery time	I_{SD}=80A, di/dt = 100A/μs,		36		ns
Q_{rr}	Reverse recovery charge	V_{DD}=19 V, Tj= 150°C		32		μC
I_{RRM}	Reverse recovery current	*(see Figure 15)*		1.8		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300μs, duty cycle 1.5%

■ TYPICAL CHARACTERISTICS

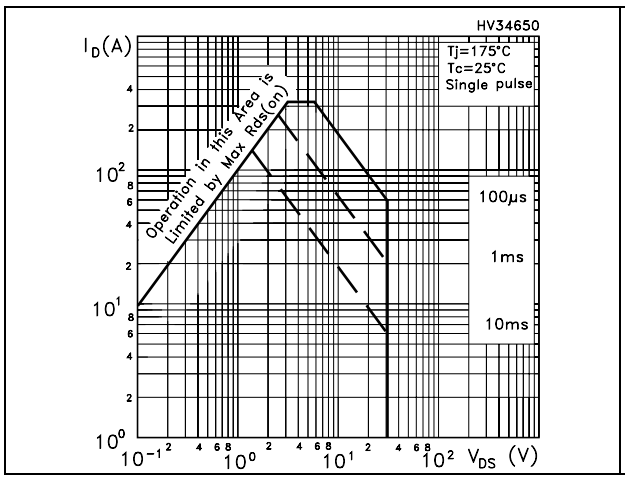


Figure 1. Safe operating area

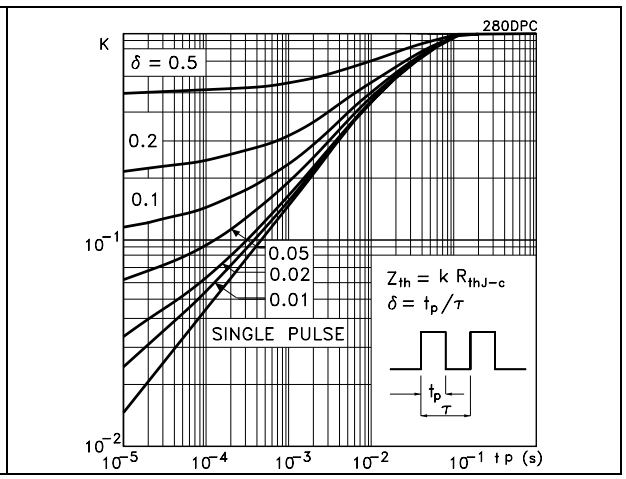


Figure 2. Thermal impedance

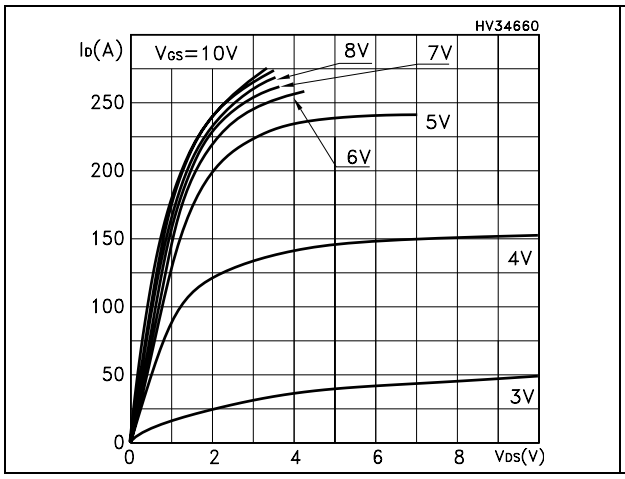


Figure 3. Output characteristics

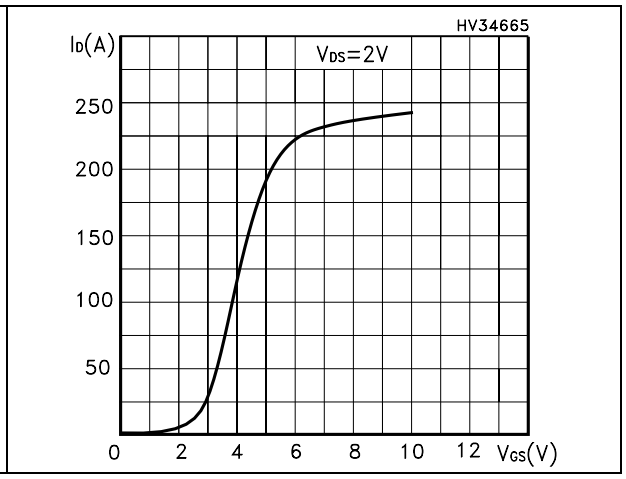


Figure 4. Transfer characteristics

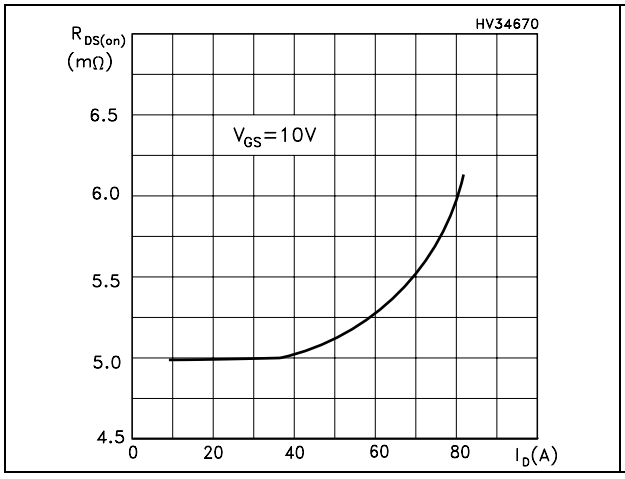


Figure 5. Static drain-source on resistance

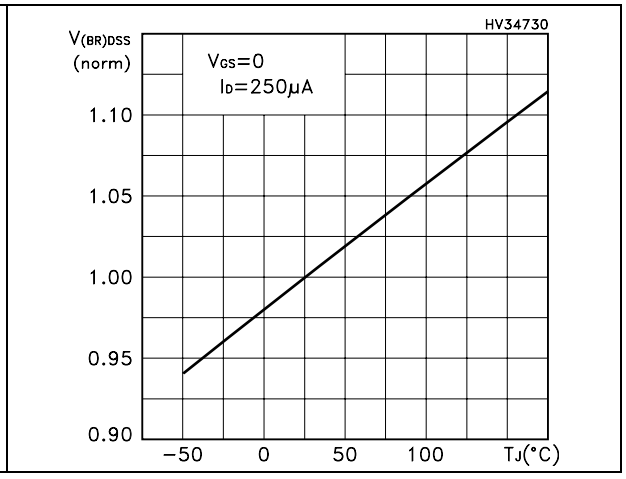


Figure 6. Normalized B_{VDSS} vs temperature

■ TYPICAL CHARACTERISTICS

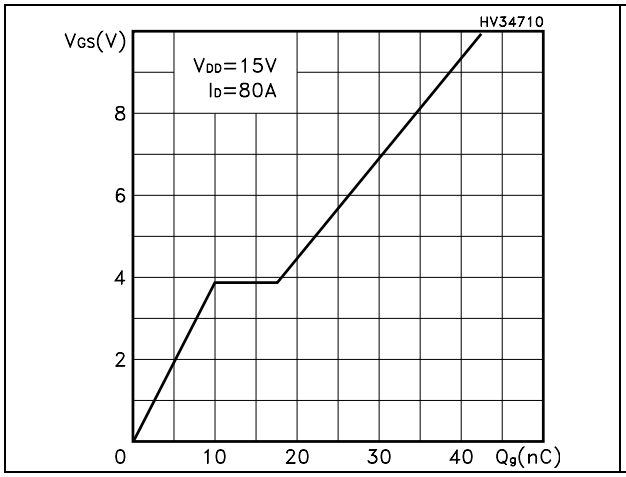


Figure 7. Gate charge vs gate-source voltage

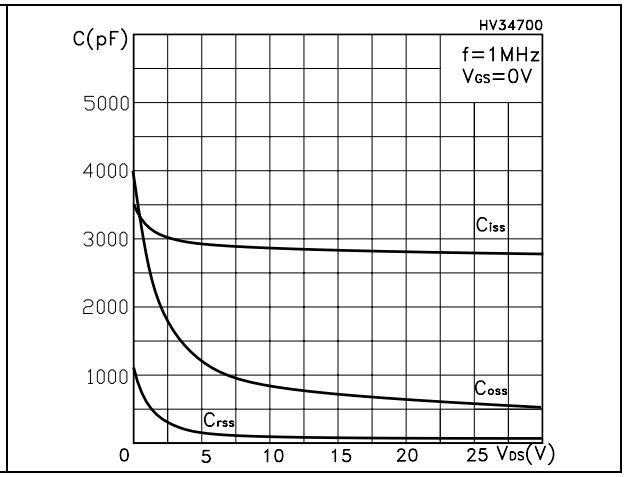


Figure 8. Capacitance variations

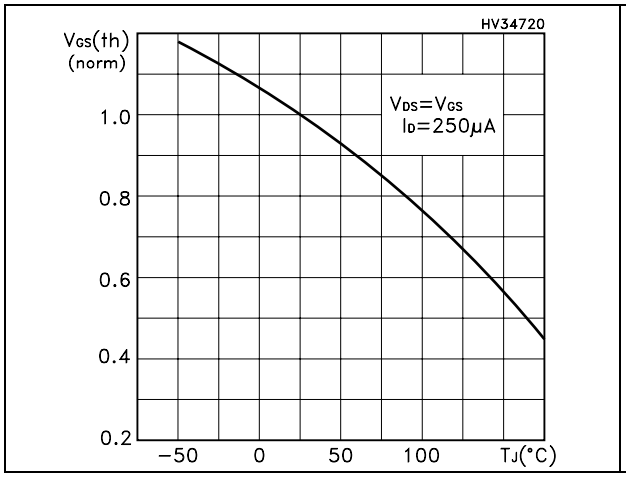


Figure 9. Normalized gate threshold voltage vs temperature

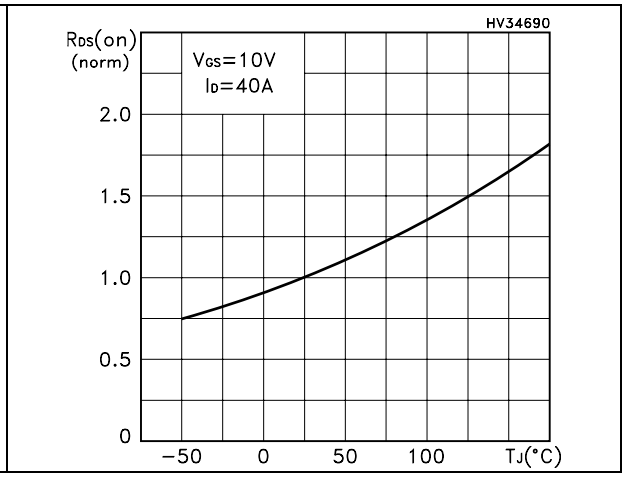


Figure 10. Normlaized on resistance vs temperature

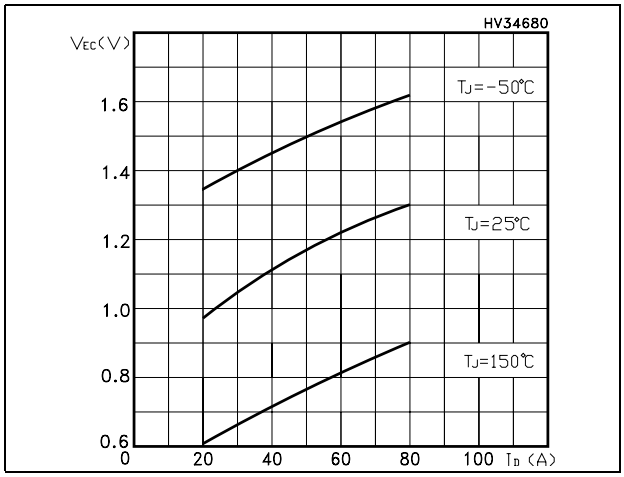
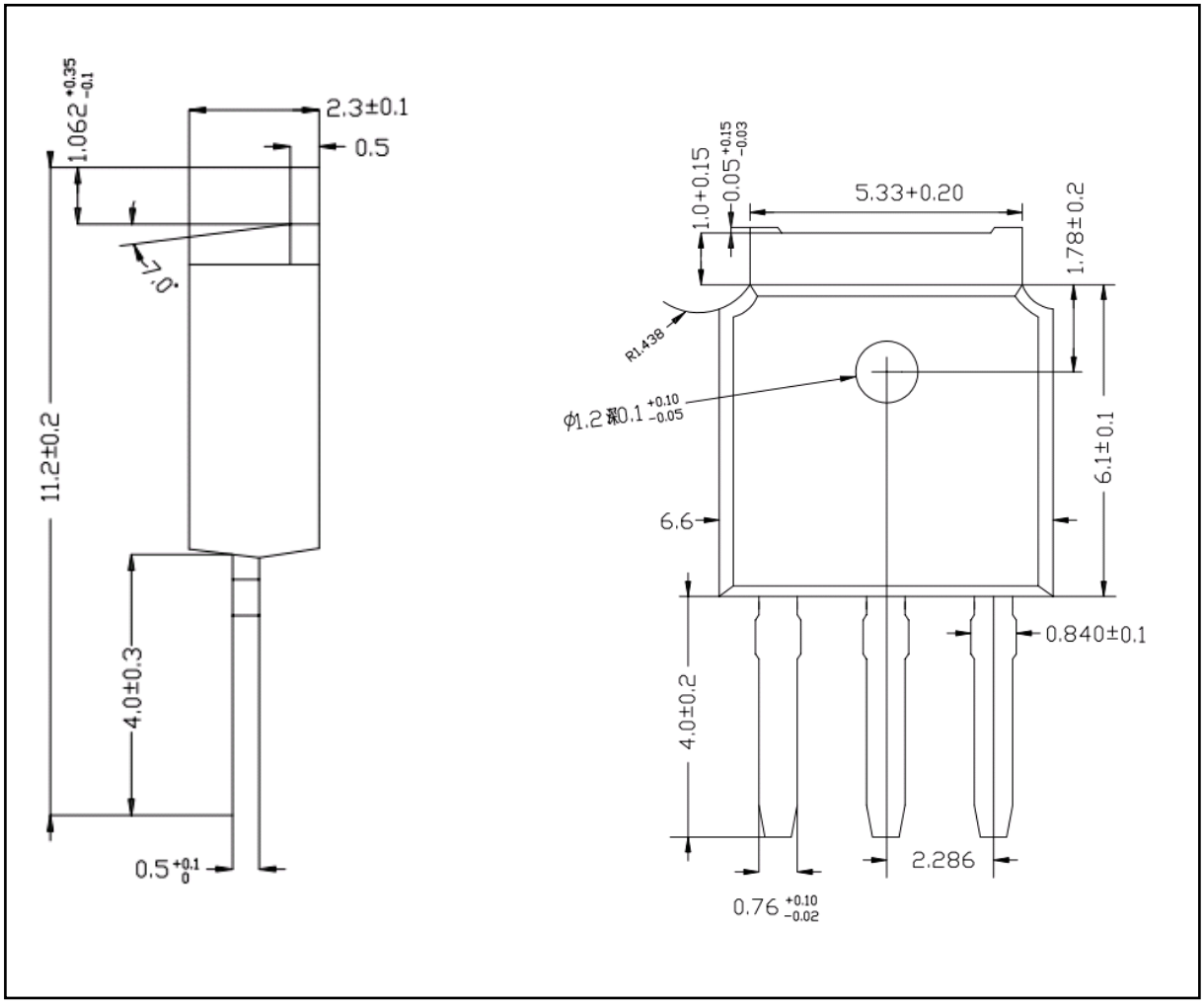


Figure 11. Source-drain diode forward characteristics

■ TO-251 PACKAGE OUTLINE DIMENSIONS



■ TO-252 PACKAGE OUTLINE DIMENSIONS