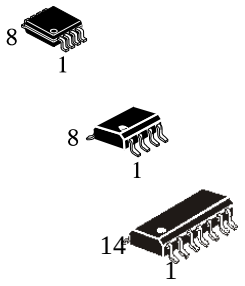
低噪声和低失真通用 **FET** 输入音频运算放大器

1 说明

HT1652A（双通道）和 HT1654A（四通道）FET 输入运算放大器在 1kHz 时可实现 7.5nV/√Hz 的低噪声 密度和 0.0005% 的超低失真。HT1652A 和HT1654A 运算放大器在 2kΩ 负载条件下提供摆幅在 800mV 这有助于提高余量并实现 动态范围的最大化。此外，这些器件还具有 ±50mA 高 输出驱动能力。

2 特性

- 低噪声：
  7.5nV/√Hz（频率为 1kHz 时）
  5.8nV/√Hz（频率为 10kHz 时）
- 低失真：1kHz 时为 0.0005%
- 低静态电流：
  每通道 6mA
- 低输入偏压电流：5nA
- 压摆率： 6V/μs
- 宽增益带宽：15MHz (G = 1)
- 单位增益稳定
- 宽电源电压范围：
  ±2.25V 至 ±18V 或 4.5V 至 36V
- 可提供双通道和四通道版本



订购信息

HT1652ARZ SOP8

HT1652ARMZ MSOP8

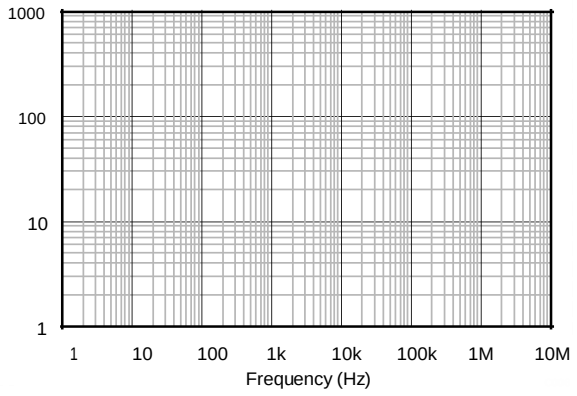
HT1654ARZ SOP14

T_A = -40° to 85°C

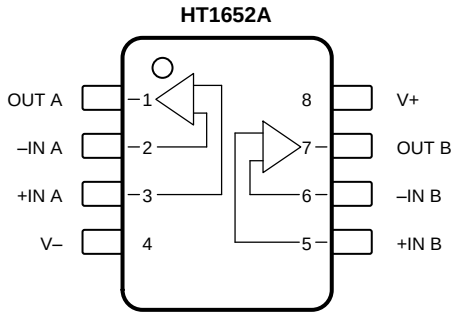
3 应用

- 模拟和数字混音器
- 音效处理器
- 乐器
- A/V 接收器
- DVD 和蓝光(Blu-Ray)™播放器
- 车载音频系统

输入电压噪声频谱密度



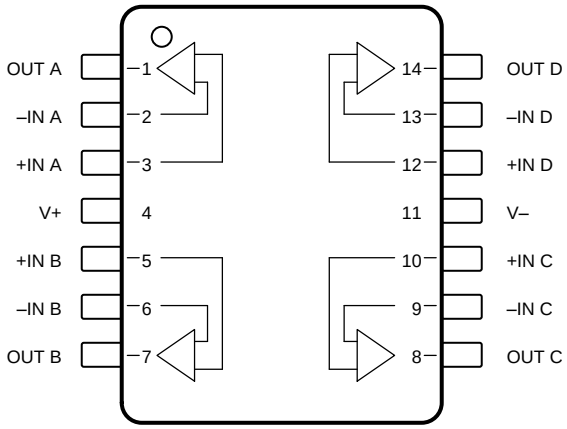
5 Pin Configuration and Functions



Pin Functions: HT1652A

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply
Thermal pad	—	—	Exposed thermal die pad on underside of DRG package; connect thermal die pad to V–. Soldering the thermal pad improves heat dissipation and provides specified performance

HT1654A



Pin Functions: HT1654A

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN D	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		40	V
	Input	(V–) – 0.5	(V+) + 0.5	V
Current	Input (all pins except power-supply pins)	–10	10	mA
	Output short-circuit(2)	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		200	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage	4.5 (±2.25)		36 (±18)	V
T_A	Operating temperature	–40		85	°C

6.4 Thermal Information: HT1652A

THERMAL METRIC(1)		HT1652A			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	143.6	218.9	66.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.9	78.6	54.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.8	103.7	40.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.8	14.6	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.3	101.8	40.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: HT1654A

THERMAL METRIC(1)		HT1654A		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.1	126.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.8	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	58.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	5.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.2	57.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics: V_S = ±15 V

at T_A = 25°C, R_L = 2 kΩ, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1		15		MHz
SR	Slew rate	G = –1		10		V/µs
	Full power bandwidth(1)	V_O = 1 V_P		1.6		MHz
	Overload recovery time	G = –10		1		µs
	Channel separation (dual and quad)	f = 1 kHz		–120		dB
NOISE						
e_n	Input voltage noise	f = 20 Hz to 20 kHz		4.0		μV_{PP}
	Input voltage noise density	f = 1 kHz		7.5		nV/√Hz
		f = 10 kHz		5.8		nV/√Hz
I_n	Input current noise density	f = 1 kHz		3		fA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±2.25 V to ±18 V		±0.5	±1.5	mV
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 85°C(2)		2	8	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2..25 V to ±18 V		3	8	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±10	±100	pA
I_{OS}	Input offset current	V_{CM} = 0 V		±10	±100	pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) + 0.5		(V+) – 2	V
CMRR	Common-mode rejection ratio		100	110		dB
INPUT IMPEDANCE						
	Differential			100 || 6		MΩ || pF
	Common-mode			6000 || 2		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.8 V ≤ V_O ≤ (V+) – 0.8 V, R_L = 2 kΩ	106	114		dB
OUTPUT						
V_{OUT}	Voltage output	R_L = 2 kΩ	(V–) + 0.8		(V+) – 0.8	V
I_{OUT}	Output current		See			mA
Z_O	Open-loop output impedance	f = 1 MHz	See			Ω
I_{SC}	Short-circuit current(3)			±50		mA
C_{LOAD}	Capacitive load drive			100		pF
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current	I_{OUT} = 0 A		2	2.5	mA
	(per channel)	I_{OUT} = 0 A, T_A = –40°C to 85°C(2)			2.8	mA
TEMPERATURE						
	Specified range		–40		85	°C
	Operating range		–55		125	°C

6.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

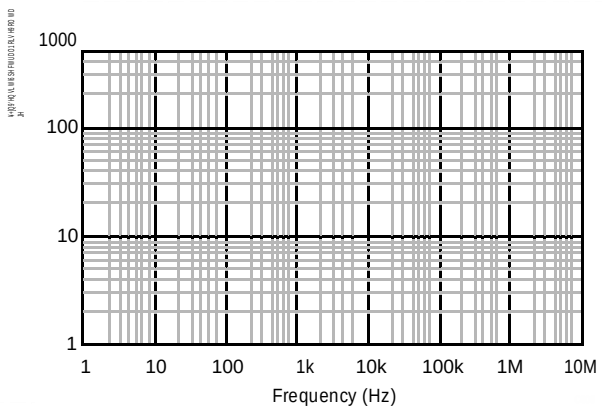


图 **1. Input Voltage Noise Density vs Frequency**

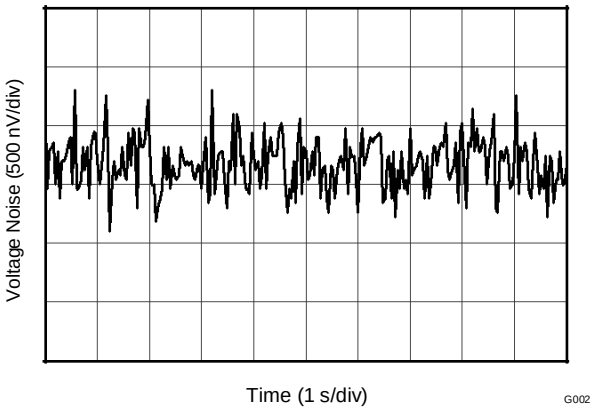


图 **2. 0.1-Hz to 10-Hz Noise**

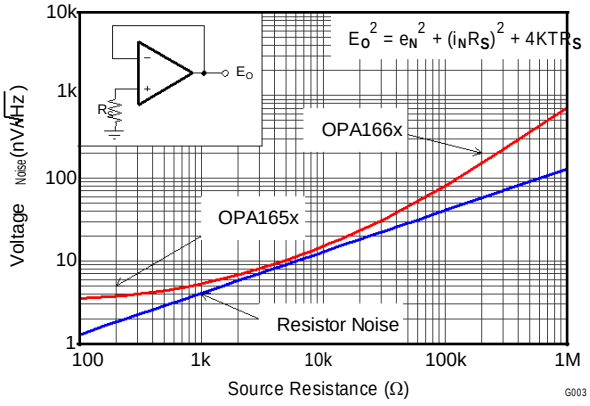


图 **3. Voltage Noise vs Source Resistance**

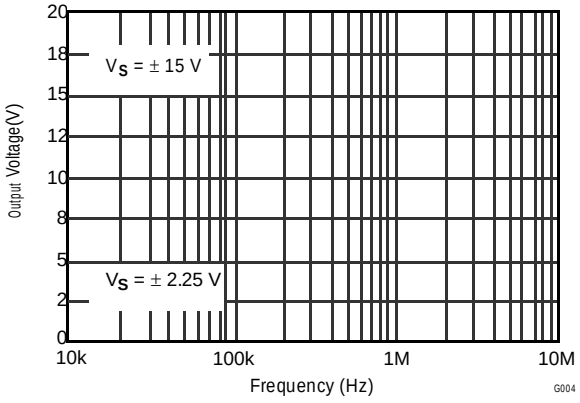


图 **4. Maximum Output Voltage vs Frequency**

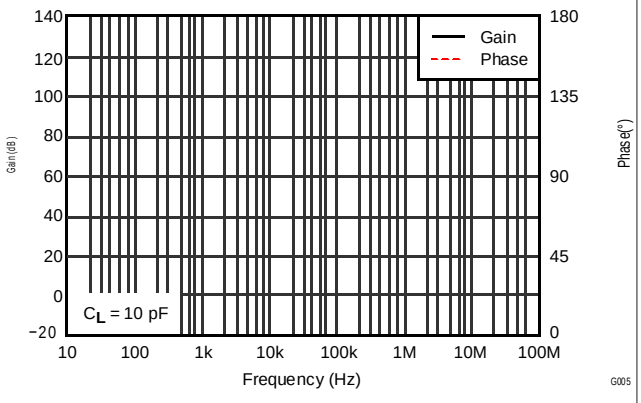


图 **5. Gain and Phase vs Frequency**

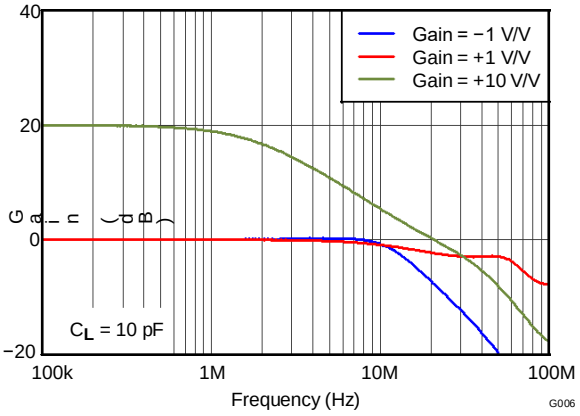


图 **6. Closed-Loop Gain vs Frequency**

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

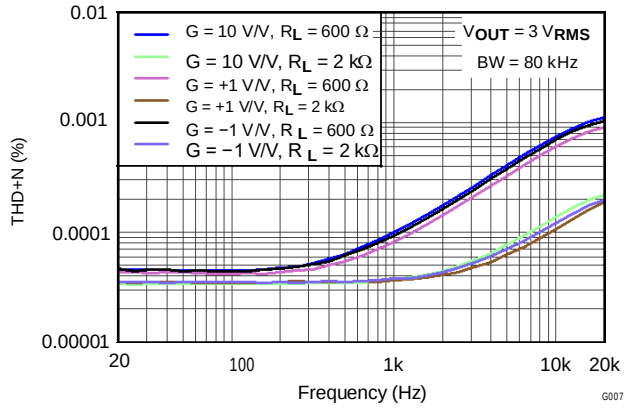


图 **7. THD+N Ratio vs Frequency**

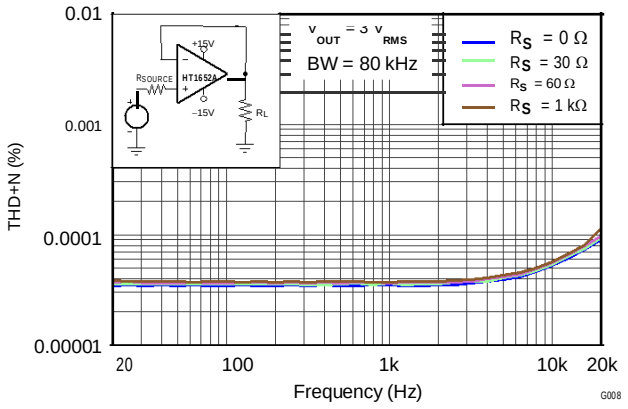


图 **8. THD+N Ratio vs Frequency**

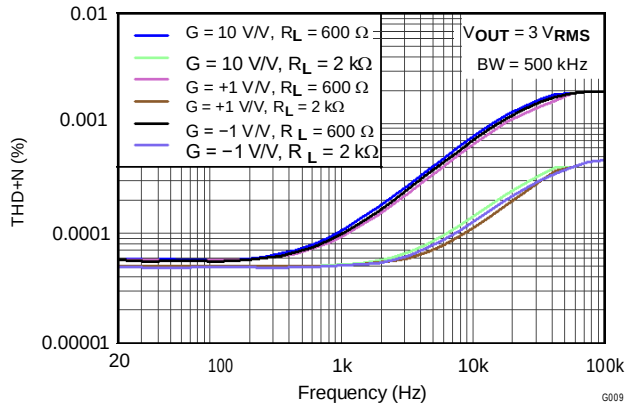


图 **9. THD+N Ratio vs Frequency**

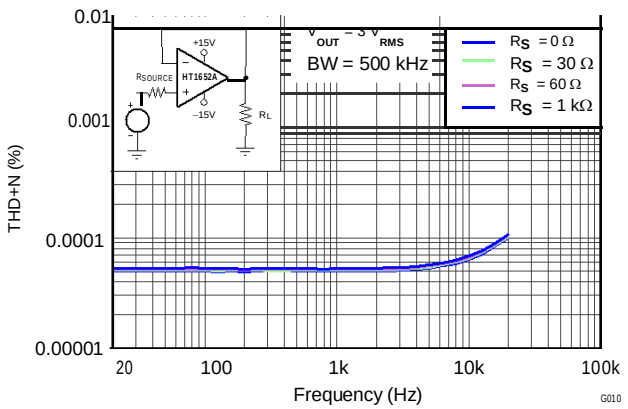


图 **10. THD+N Ratio vs Frequency**

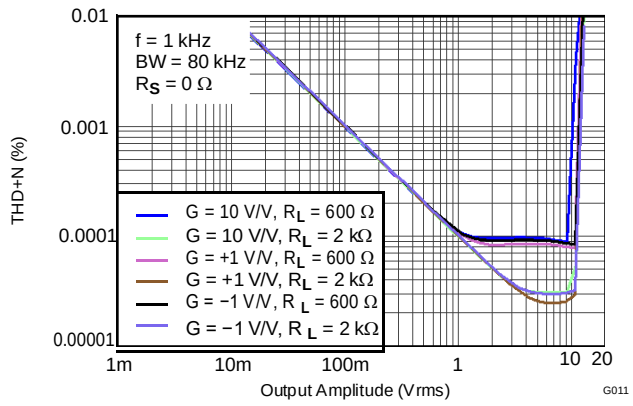


图 **11. THD+N Ratio vs Output Amplitude**

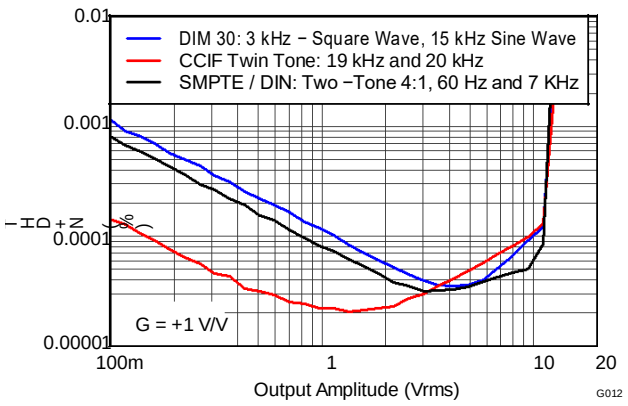


图 **12. Intermodulation Distortion vs Output Amplitude**

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

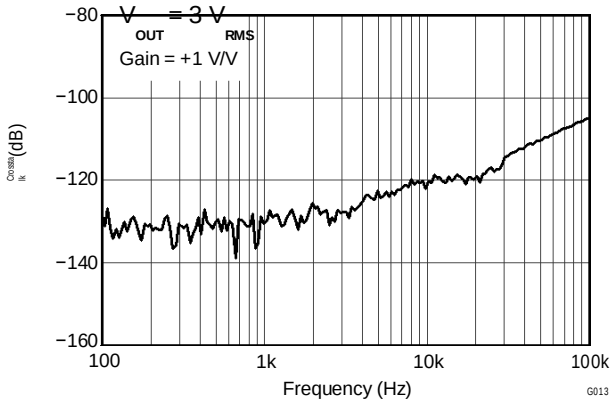


图 13. Channel Separation vs Frequency

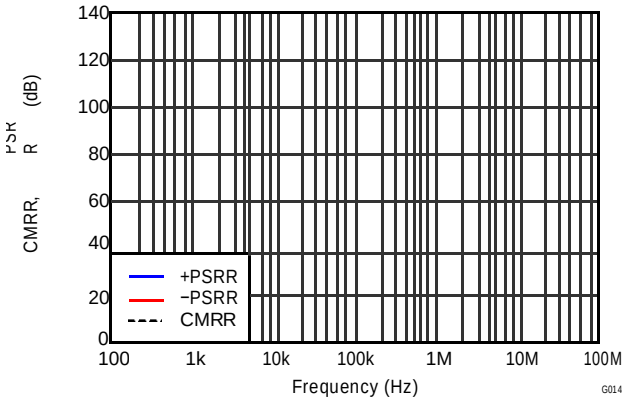


图 14. CMRR and PSRR vs Frequency (Referred to Input)

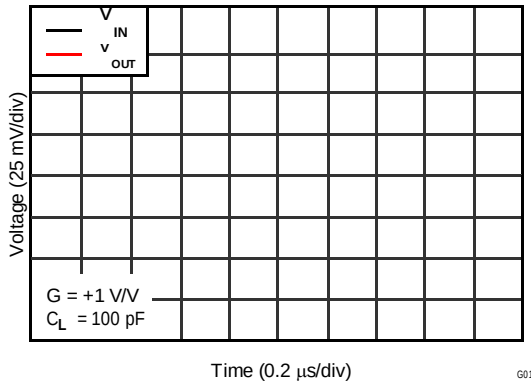


图 15. Small-Signal Step Response (100 mV)

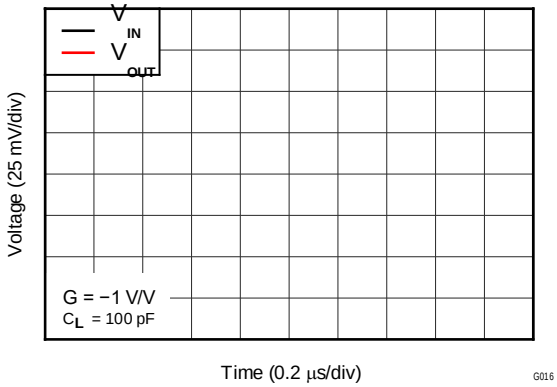


图 16. Small-Signal Step Response (100 mV)

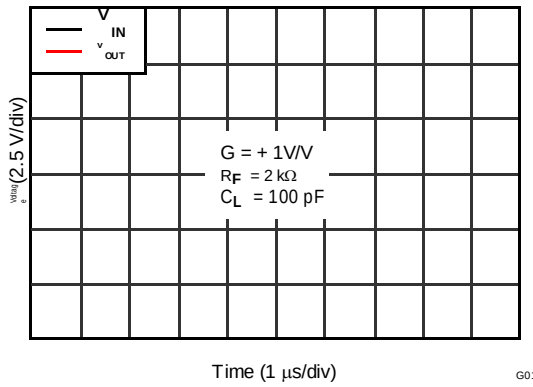


图 17. Large-Signal Step Response

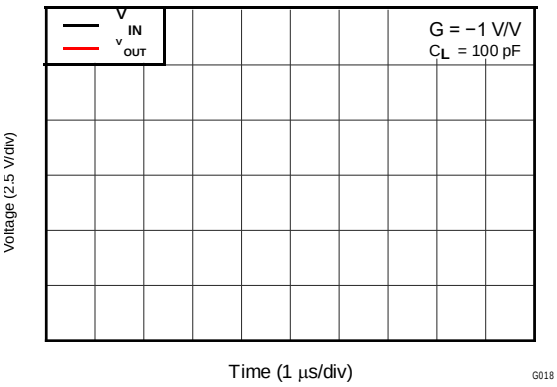


图 18. Large-Signal Step Response

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

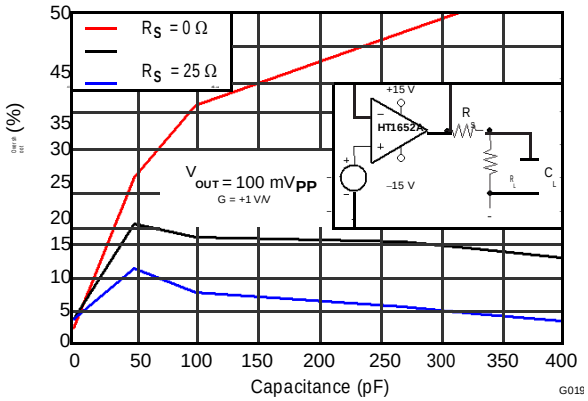


图 **19. Small-Signal Overshoot vs Capacitive Load**

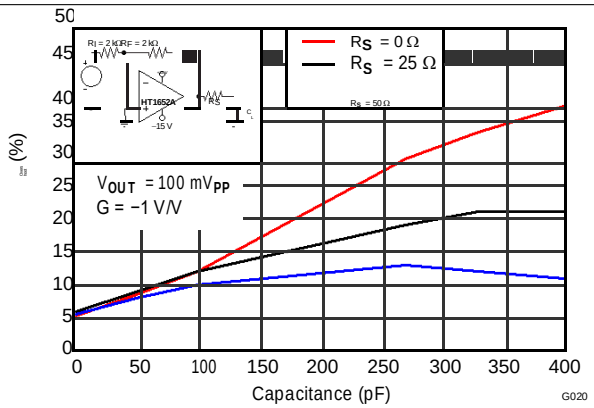


图 **20. Small-Signal Overshoot vs Capacitive Load**

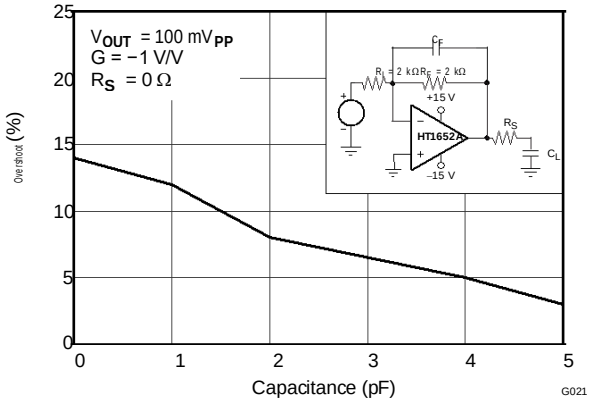


图 **21. Small-Signal Overshoot vs Feedback Capacitor (100-mV Output Step)**

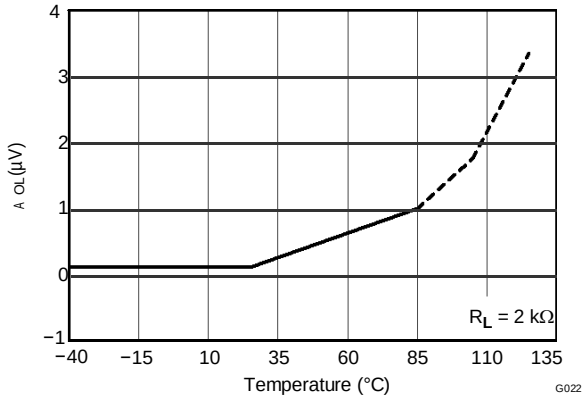


图 **22. Open-Loop Gain vs Temperature**

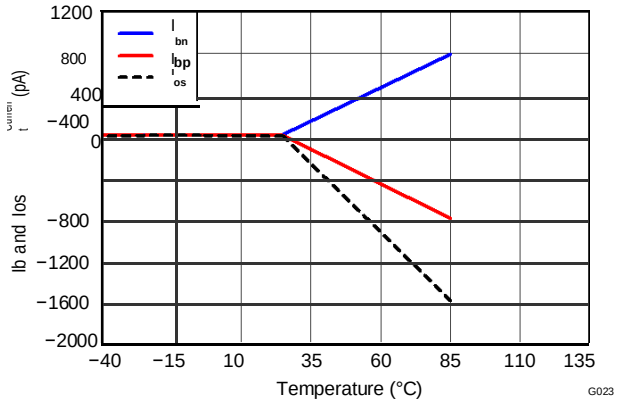


图 **23. I_B and I_{OS} vs Temperature**

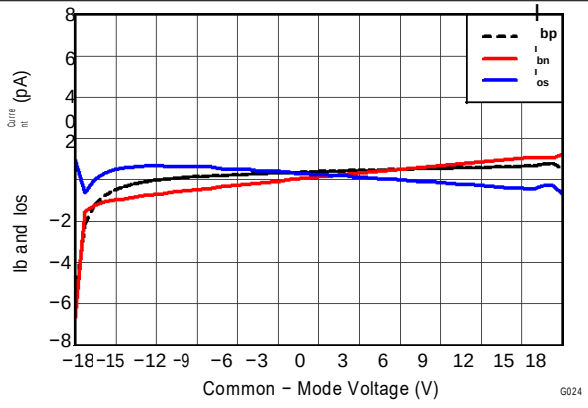


图 **24. I_B and I_{OS} vs Common-Mode Voltage**

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

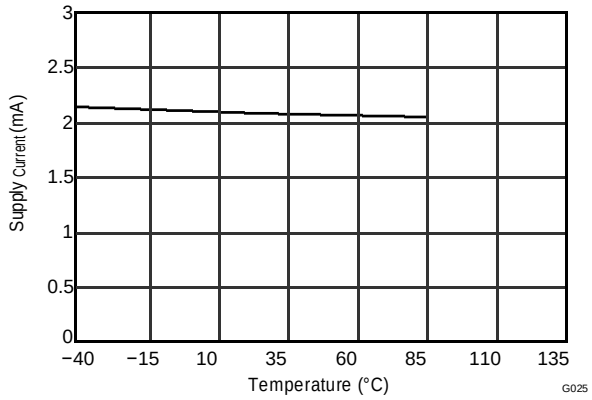


图 **25. Supply Current vs Temperature**

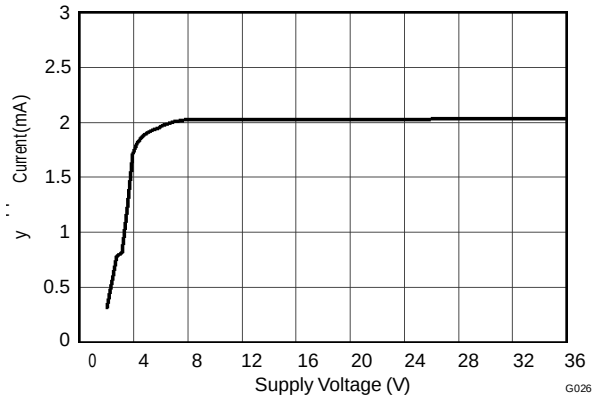


图 **26. Supply Current vs Supply Voltage**

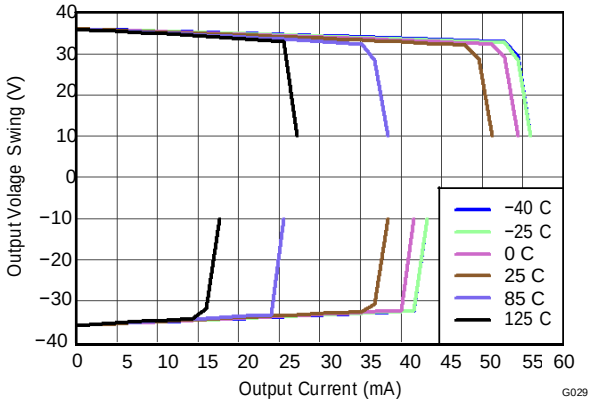


图 **27. Output Voltage vs Output Current**

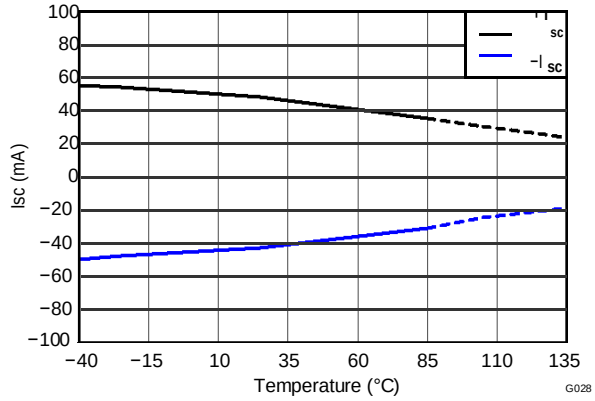


图 **28. Short-Circuit Current vs Temperature**

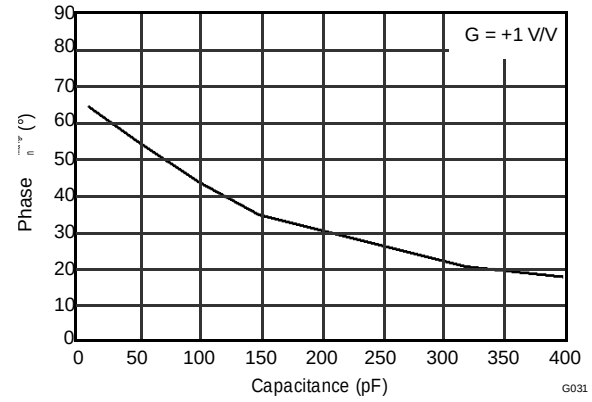


图 **29. Phase Margin vs Capacitive Load**

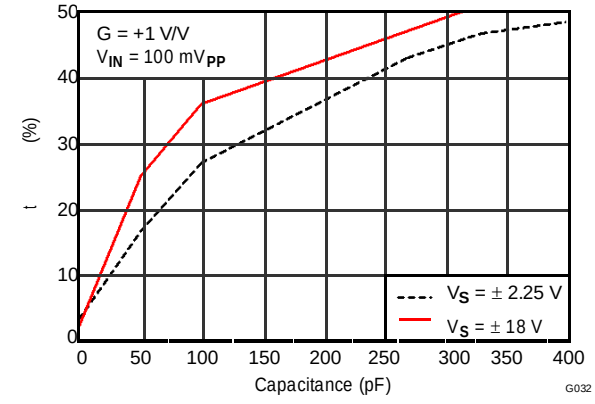


图 **30. Percent Overshoot vs Capacitive Load**

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

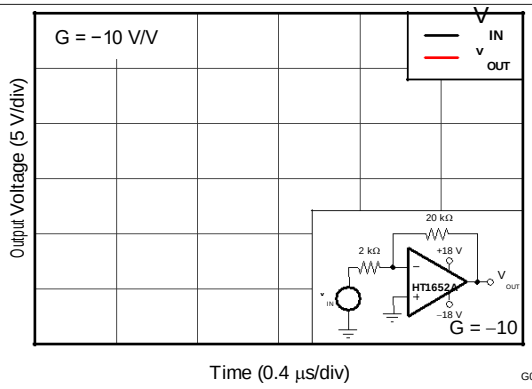


图 **31. Negative Overload Recovery**

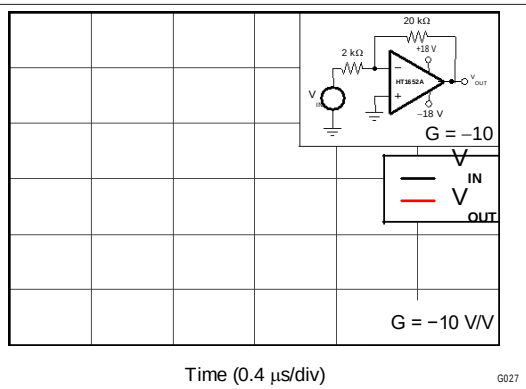


图 **32. Positive Overload Recovery**

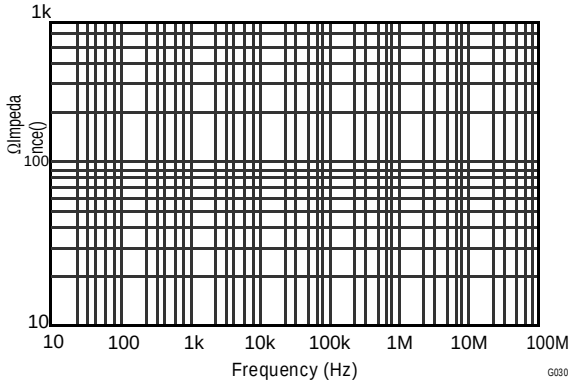


图 **33. Open-Loop Output Impedance vs Frequency**

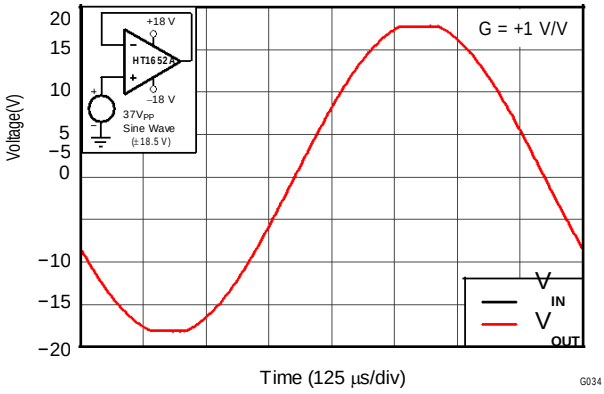


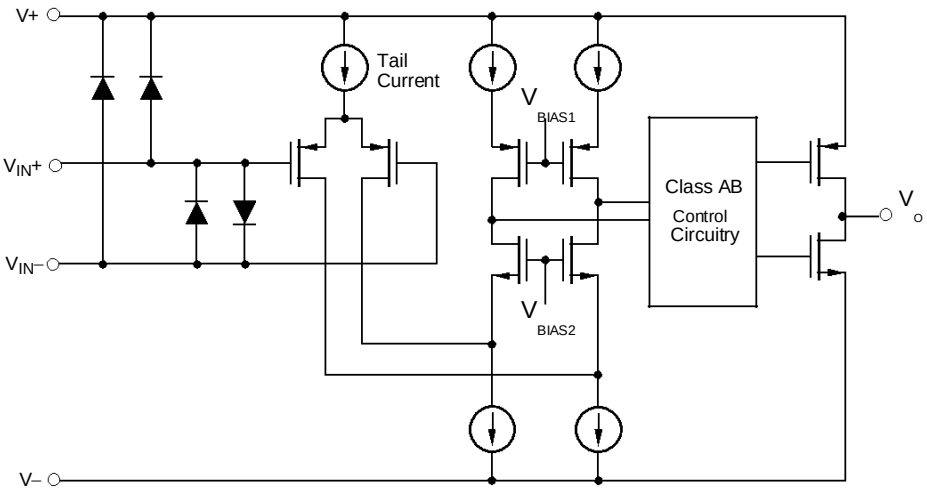
图 **34. No Phase Reversal**

7 Detailed Description

7.1 Overview

The HT1652A and HT1654A are unity-gain stable, precision dual and quad op amps with very low noise. The *Functional Block Diagram* shows a simplified schematic of the OPA165x (with one channel shown). The device consists of a very low noise input stage with a folded cascode and a rail-to-rail output stage. This topology exhibits superior noise and distortion performance across a wide range of supply voltages not previously delivered by audio operational amplifiers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Phase Reversal Protection

The OPA165x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA165x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in 图 35.

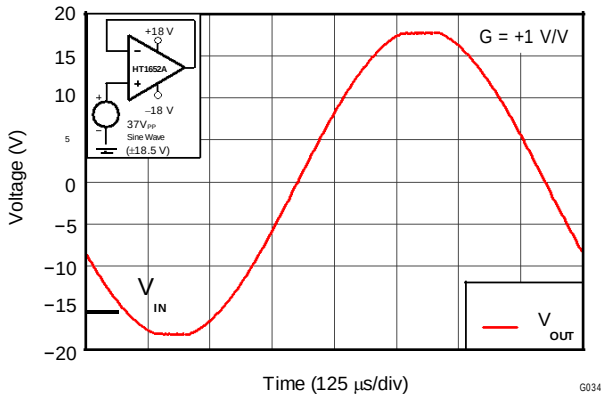


图 **35. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition**

Feature Description (接下页)

7.3.2 Input Protection

The input terminals of the HT1652A and HT1654A are protected from excessive differential voltage with back-to-back diodes, as 图 36 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) or a feedback resistor (R_F) can limit the signal input current. This resistor degrades the low-noise performance of the OPA165x, and is examined in the *Noise Performance* section. 图 36 shows an example configuration when both current-limiting input and feedback resistors are used.

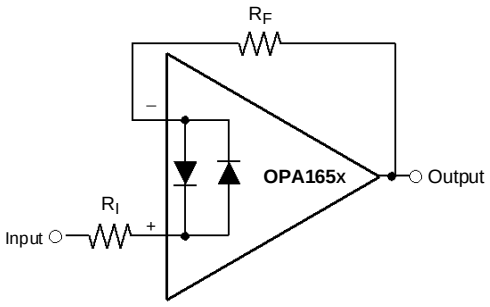


图 **36. Pulsed Operation**

7.3.3 Electrical Overstress

Designers typically ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 图 37 illustrates the ESD circuits contained in the OPA165x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (接下页)

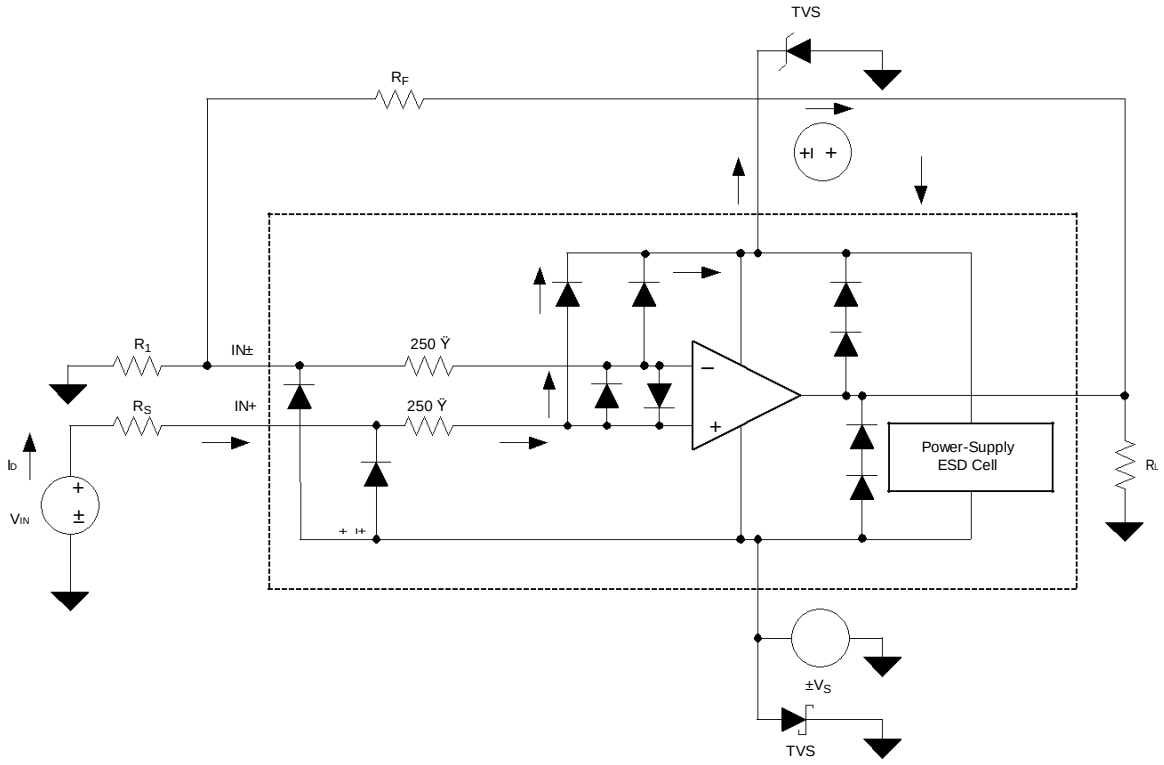


图 **37. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

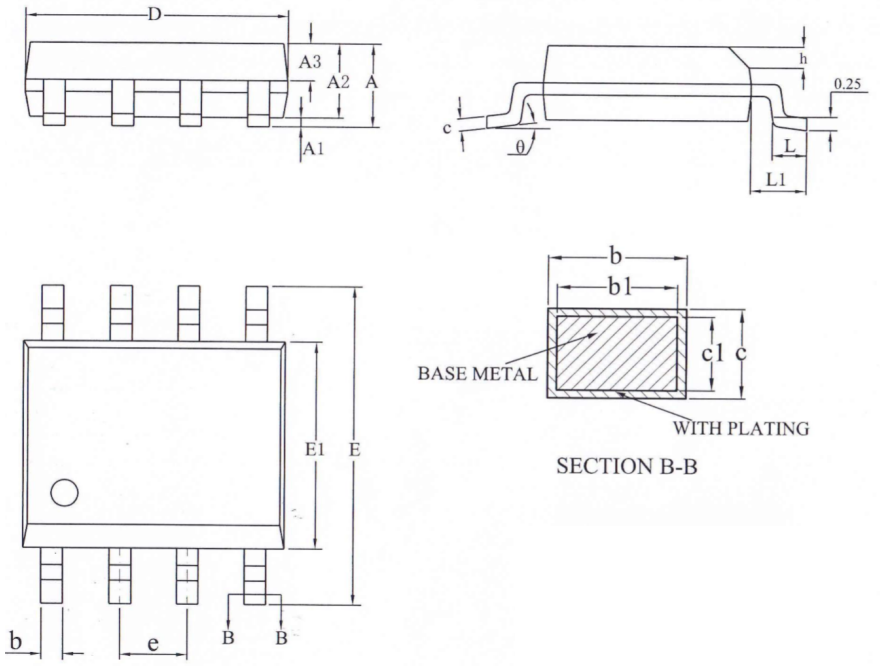
When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. The absorption device activates depending on the path that the current takes. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA165x, but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (refer to 图 37), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 37 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

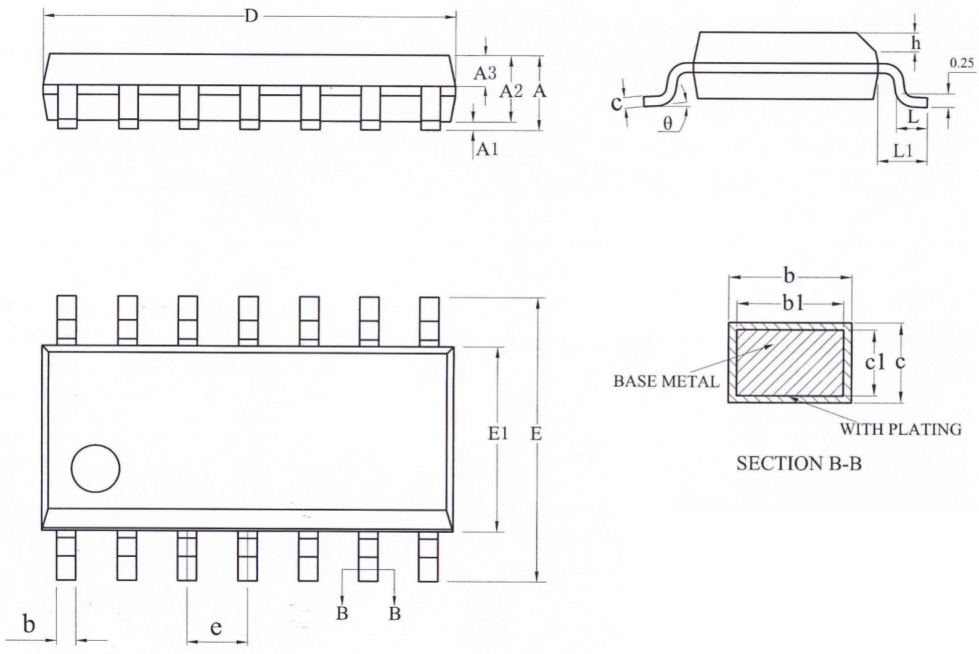
If the supply is not capable of sinking the current, V_{IN} begins sourcing current to the operational amplifier, and then becomes the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the absolute maximum ratings of the operational amplifier.

SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
① b	0.39	—	0.47
① b1	0.38	0.41	0.44
① c	0.20	—	0.24
c1	0.19	0.20	0.21
① D	4.80	4.90	5.00
E	5.80	6.00	6.20
① E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

SOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
① b	0.39	—	0.47
① b1	0.38	0.41	0.44
① c	0.20	—	0.24
c1	0.19	0.20	0.21
① D	8.55	8.65	8.75
E	5.80	6.00	6.20
① E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°