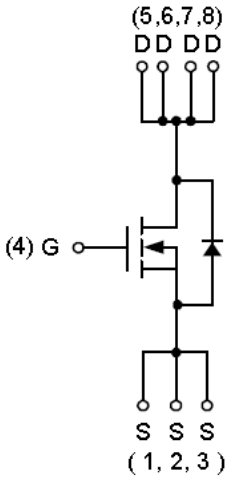
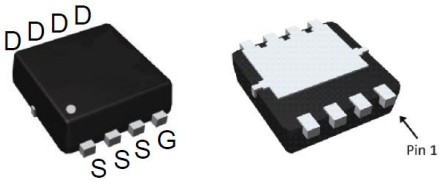
N-Channel Enhancement Mode MOSFET TDM31074A

DESCRIPTION

The TDM31074A uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.





PPAK-3*3-8

GENERAL FEATURES

- RDS(ON) < 16mΩ @ VGS=10V
  RDS(ON) < 22.5mΩ @ VGS=4.5V
- Extremely low switching loss
- Excellent stability and uniformity
- Lead free product is available
- PPAK3*3-8 Package

Application

- High Frequency Switching
- Synchronous Rectification

ABSOLUTE MAXIMUM RATINGS(T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current @ Continuous (Note 1)	I_D（T_C=25℃）	40	A
	I_D（T_C=100℃）	27	A
Pulsed Drain Current (Note 2)	I_{DM}	160	A
Maximum Power Dissipation (Note 3)	P_D(T_C=25℃)	50	W
Thermal Resistance, Junction-to-Case (Note 4)	$R_{\theta JC}$	4.7	℃/W
Thermal Resistance, Junction-to-Ambient (Note 4，Note 5)	$R_{\theta JA}$	60	℃/W
Avalanche Current, Single pulse (Note 2，Note 6)	I_{AS}(L=0.5mH)	6	A
Avalanche Energy, Single pulse (Note 2，Note 6)	E_{AS}(L=0.5mH)	32	mJ
Operating Junction Temperature Range	T_J	-55 To 150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

ELECTRICAL CHARACTERISTICS (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS\ (th)}$	V_{DS}=VGS, I_D=250μA	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	14.3	16	mΩ
	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=10A	-	18.8	22.5	mΩ
Gate Resistance	R_G	V_{DS}=0V, V_{GS}=0V, F=1.0MHz	-	1.5	-	Ω
DYNAMIC CHARACTERISTICS (Note7)						
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, F=1.0MHz	-	1130	-	PF
Output Capacitance	C_{oss}		-	496	-	PF
Reverse Transfer Capacitance	C_{rss}		-	60	-	PF
SWITCHING CHARACTERISTICS (Note 7)						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=50V, V_{GS}=10V, R_G=3.3Ω I_D=40A	-	46	-	nS
Turn-on Rise Time	t_r		-	55	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	249	-	nS
Turn-Off Fall Time	t_f		-	105	-	nS
Total Gate Charge	Q_g	V_{DS}=50V, I_D=40A, V_{GS}=10V	-	30		nC
Gate-Source Charge	Q_{gs}		-	6	-	nC
Gate-Drain Charge	Q_{gd}		-	8.2	-	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Continuous Source Current	I_S		-	40	-	A
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=20A	-	0.8	1.0	V
Reverse Recovery Time	T_{rr}	I_F=20A, dI/dt=100A/μs	-	70	-	nS
Reverse Recovery Charge	Q_{rr}		-	224	-	nC

NOTES:

1. The maximum current rating is package limited.

2. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

3. The power dissipation PD is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

4. The value of $R_{\theta JC}$ is measured in a still air environment with T_A =25°C and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

5. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

6. The EAS data shows Max. rating. The test condition is V_{DS}=50V, V_{GS}=10V, L=0.5mH

7. Guaranteed by design, not subject to production testing

Typical Operating Characteristics

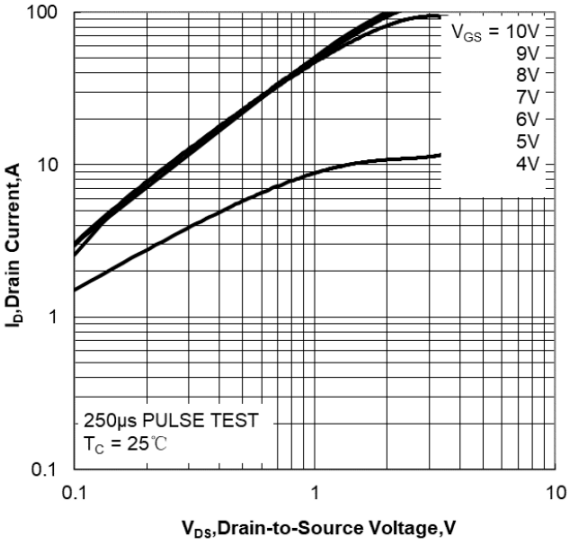


Figure 1. Output Characteristics

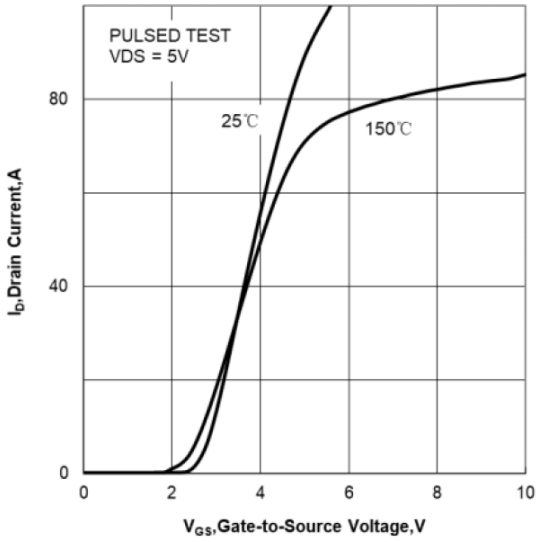


Figure 2. Transfer Characteristics

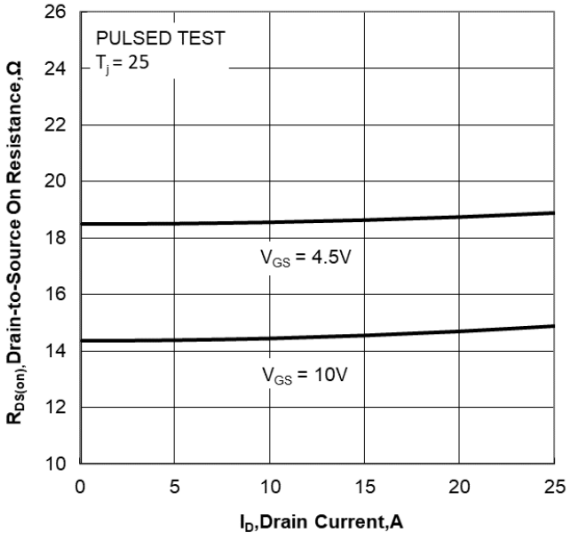


Figure 3. Drain-to-Source On Resistance vs Drain Current

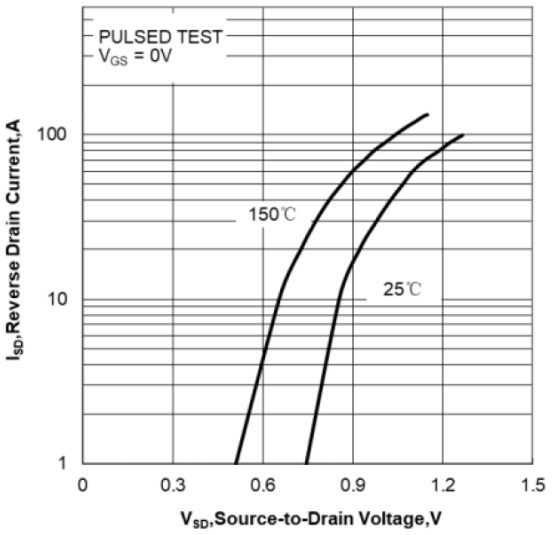


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

Typical Operating Characteristics (Cont.)

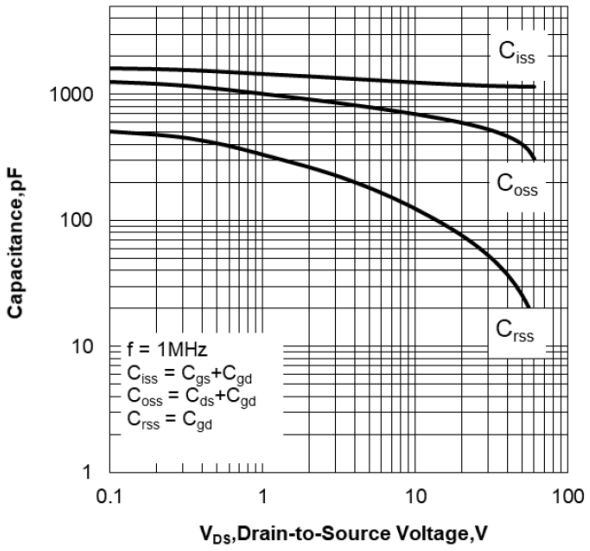


Figure 5. Capacitance Characteristics

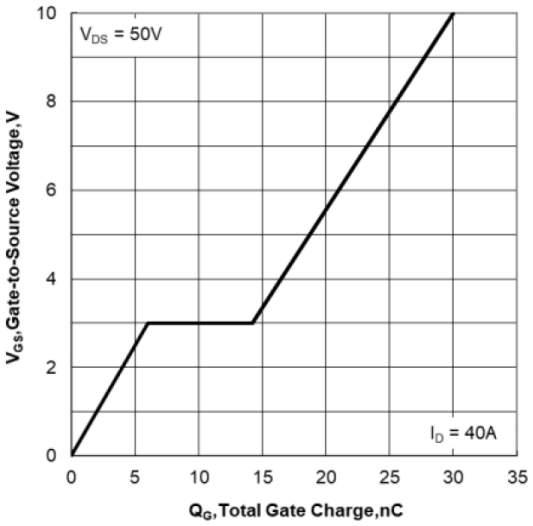


Figure 6. Gate Charge Characteristics

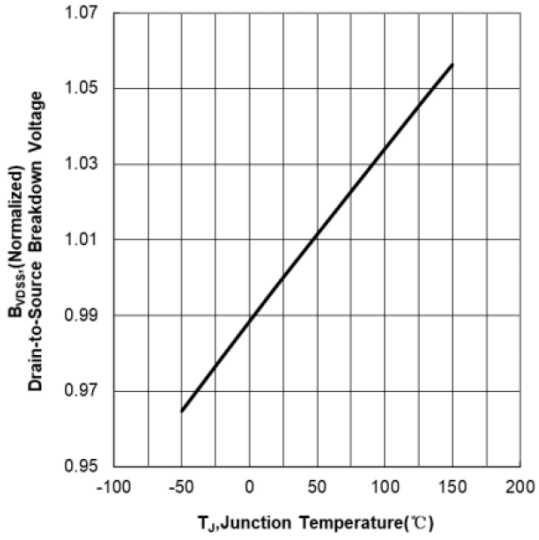


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

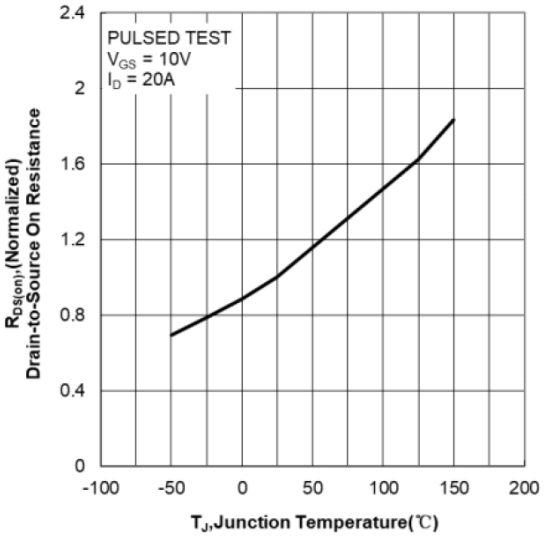


Figure 8. Normalized On Resistance vs Junction Temperature

Typical Operating Characteristics (Cont.)

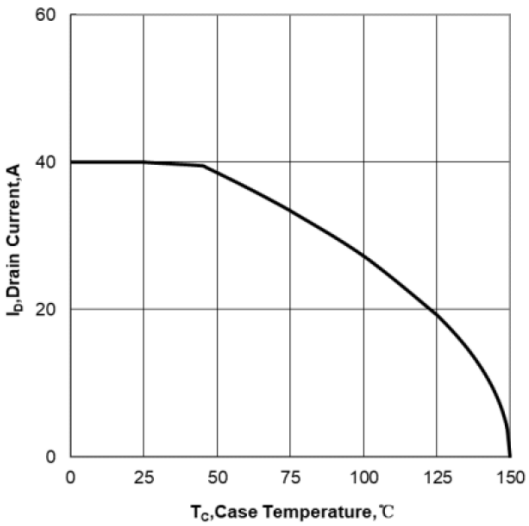


Figure 9. Maximum Continuous Drain Current vs Case Temperature

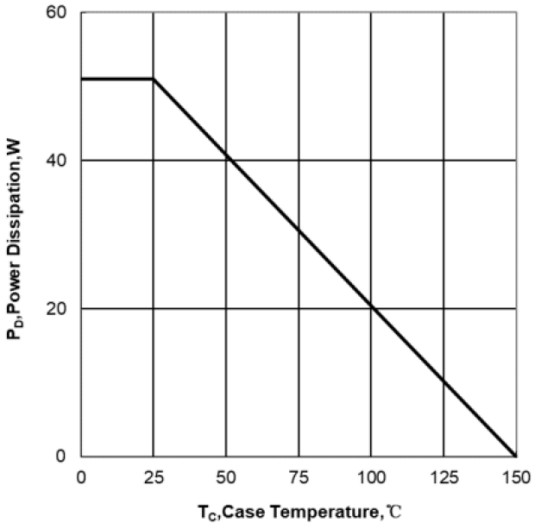


Figure 10. Maximum Power Dissipation vs Case Temperature

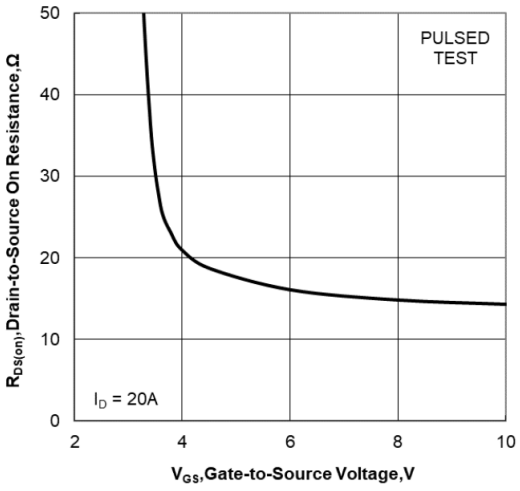


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

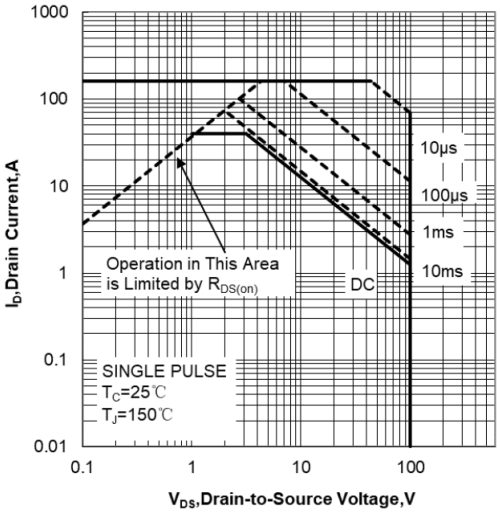


Figure 12. Maximum Safe Operating Area

Typical Operating Characteristics (Cont.)

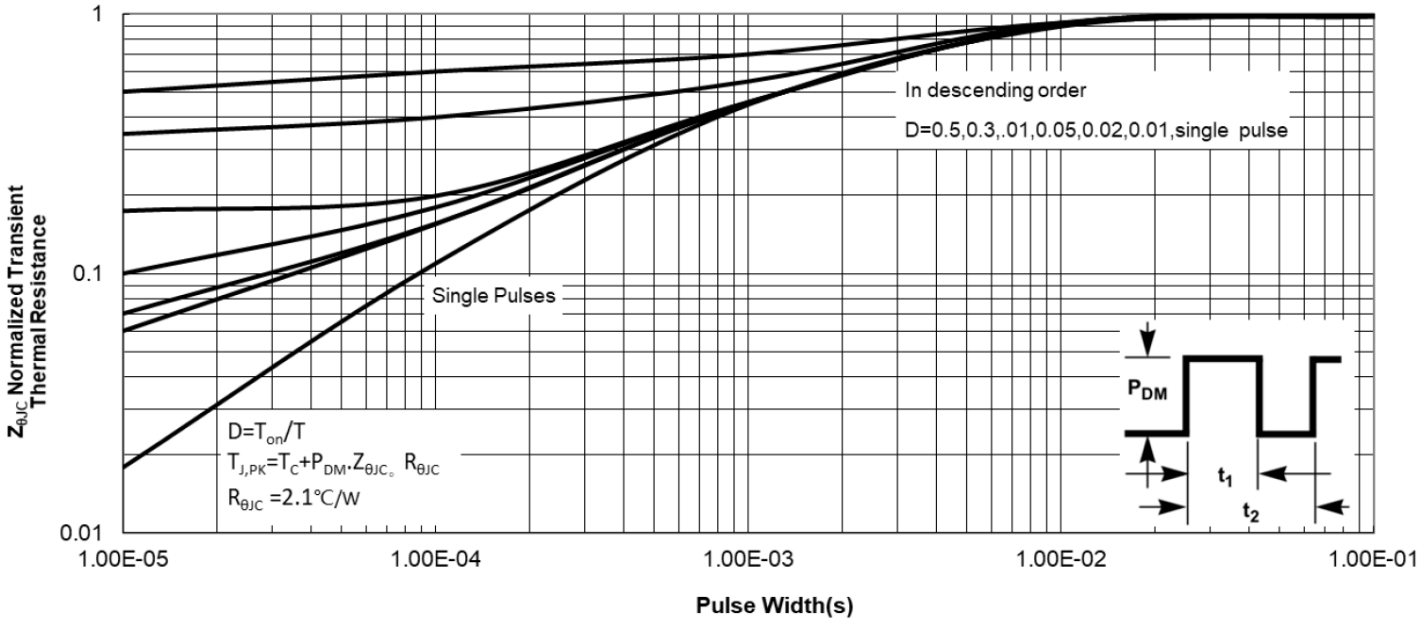
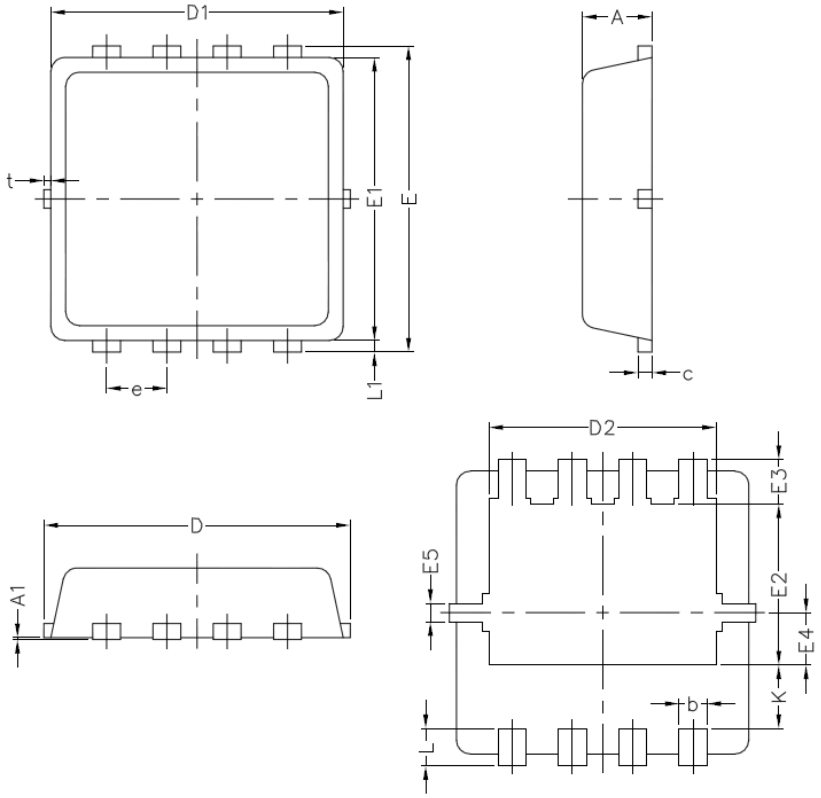


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Information

PPAK-3*3-8 Package



Symbol	PPAK-3*3-8(mm)		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.3	3.45
D1	3.00	3.15	3.30
D2	2.25	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.68
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.49	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	/	/	0.13

Design Notes