

# N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>(BR)DSS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)		
100	0.030 at V <sub>GS</sub> = 10 V	45		
	0.035 at V <sub>GS</sub> = 4.5 V	40		

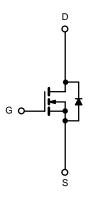
#### **FEATURES**

- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- Low Thermal Resistance Package









N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	10 = 20 °C, driless offi			1	
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	7 v	
Continuous Drain Current (T <sub>.1</sub> = 175 °C)	T <sub>C</sub> = 25 °C	I-	45		
Continuous Diam Current (1) = 173 C)	T <sub>C</sub> = 125 °C	I <sub>D</sub>	30		
Pulsed Drain Current		I <sub>DM</sub>	135	A	
Avalanche Current		I <sub>AR</sub>	35		
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AR</sub>	61	mJ	
	T <sub>C</sub> = 25 °C	В	127 <sup>b</sup>	10/	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C <sup>c</sup>	$P_{D}$	3.75	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>sta</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Limit	Unit	
Junction-to-Ambient	(PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)		R <sub>thJC</sub>	1.4	C/VV	

#### Notes:

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{SS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		3		
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μА	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50		
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250	1	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	75			Α	
		$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		0.030		Ω	
	_	$V_{GS} = 4.5 \text{ V}, I_D = 3 \text{ A}$		0.035			
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A, T <sub>J</sub> = 125 °C		0.050			
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A, T <sub>J</sub> = 175 °C		0.062			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	10			S	
Dynamic <sup>b</sup>	<u> </u>			<b>.</b>			
Input Capacitance	C <sub>iss</sub>			3100		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		410			
Reverse Transfer Capacitance	C <sub>rss</sub>			150			
Total Gate Charge <sup>c</sup>	Qg			35	60	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 40 \text{ A}$		11			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			9			
Gate Resistance	R <sub>G</sub>			1.7		Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			11	20		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V, R}_{1} = 1.25 \Omega$		12	20	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D\cong 40$ A, $V_{GEN}$ = 10 V, $R_G$ = 2.5 $\Omega$		30	45		
Fall Time <sup>c</sup>	t <sub>f</sub>			12	20		
Source-Drain Diode Ratings and Cha	aracteristics 7	C = 25 °C <sup>b</sup>					
Continuous Current	I <sub>S</sub>				40	^	
Pulsed Current	I <sub>SM</sub>				120	Α	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		1.0	1.5	V	
Reverse Recovery Time	t <sub>rr</sub>			60	100	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	$I_F = 30 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		5	8	Α	
Reverse Recovery Charge	Q <sub>rr</sub>	·		0.15	0.4	μC	

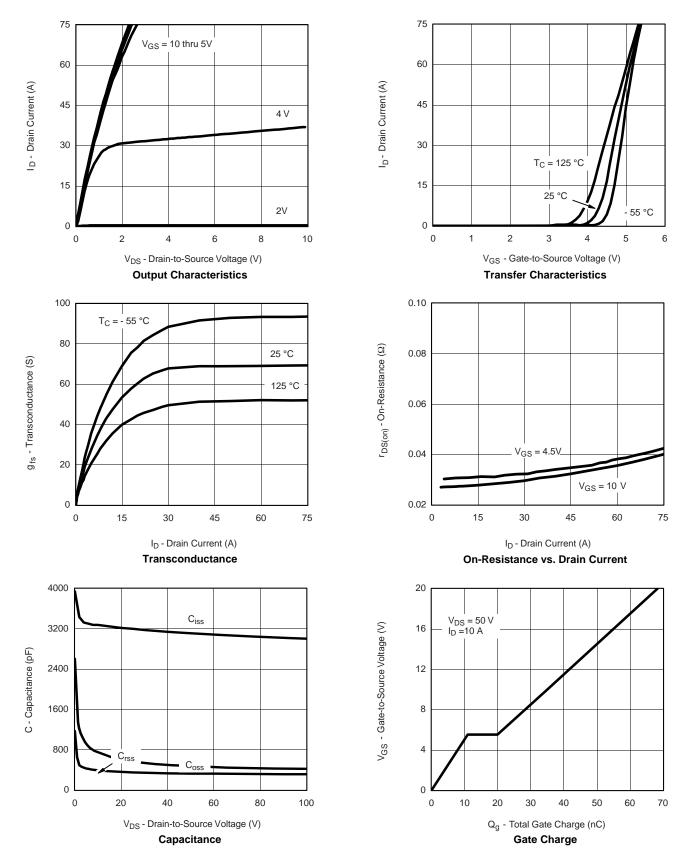
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

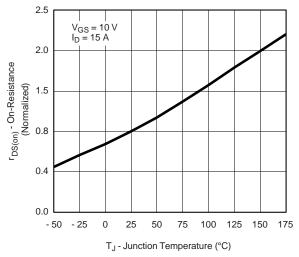


### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

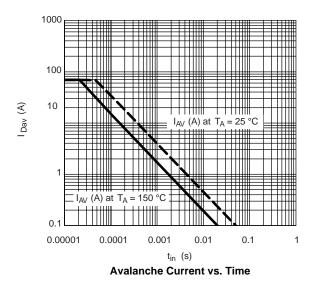




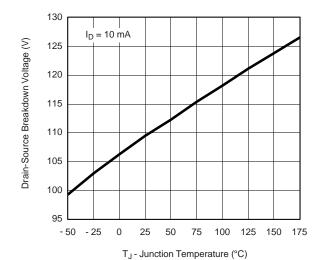
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On-Resistance vs. Junction Temperature



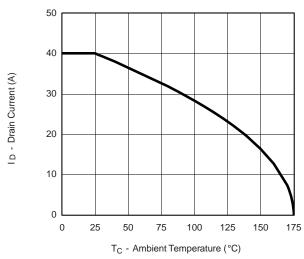
Source-Drain Diode Forward Voltage



Drain-Source Breakdown Voltage vs. Junction Temperature



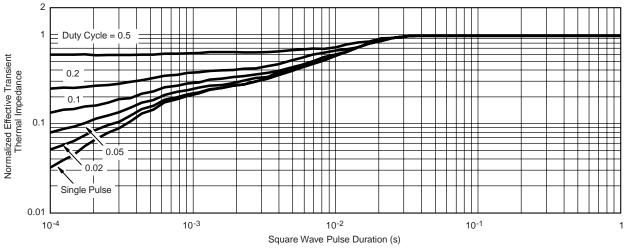
#### THERMAL RATINGS



 $\begin{array}{c} \text{100} \\ \text{Limited} \\ \text{by } r_{DS(on)^*} \\ \text{10} \\ \text{1$ 

1000

Maximum Avalanche and Drain Current vs. Case Temperature

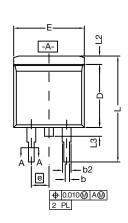


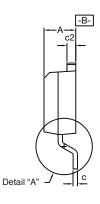
Normalized Thermal Transient Impedance, Junction-to-Case

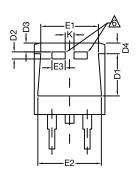
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# **TO-263 (D<sup>2</sup>PAK): 3-LEAD**

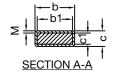








DETAIL A (ROTATED 90°)



		INCHES		MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
	Α	0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
Ci	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
D1		0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100 BSC		2.54 BSC		
	K	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
	L2	0.040	0.055	1.016	1.397	
	L3 0.050 0.07		0.070	1.270	1.778	
L4		0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	

ECN: T13-0707-Rev. K, 30-Sep-13

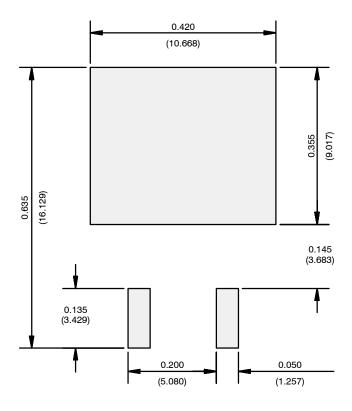
DWG: 5843

#### **Notes**

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement. 6. This feature is for thick lead.



### RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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