LPDDR4X/LPDDR4 SDRAM

ZD512M32Z42MD1DNQ-053BT, ZD1G32Z42MD2DNQ-053BT

Features

This addendum is for LPDDR4X and LPDDR4 unified product based on LPDDR4X information.

- Ultra-low-voltage core and I/O power supplies
  - VDD1 = 1.70-1.95V; 1.80V nominal
  - VDD2 = 1.06-1.17V; 1.10V nominal
  - VDDQ = 0.57-0.65V; 0.60V nominal or VDDQ = 1.06-1.17V; 1.10V nominal
- Frequency range
  - 1866-10 MHz (data rate range per pin: 3732-20Mb/s)
- 16*n* prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 7.46 GB/s per channel (x16)
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- ROHS compliant
- Programmable V_{SS} (ODT) termination
- Single-ended CK and DQS support

Options	Marking
• $V_{DD1}/V_{DD2}/V_{DDQ}$: 1.80V/1.10V/0.60V or 1.10V	
• Array configuration	
- 512 Meg x 32 (2 channels x 16 I/O)	512M32
- 1 Gig x 32 (2 channels x 16 I/O)	1G32
• Device configuration	
- 512M32 x 1 die in package	D1
- 512M32 x 2 die in package	D2
• Green Package	
- 200-ball WFBGA (10mm x 14.5mm, seated height: 0.80mm MAX)	NP
- 200-ball VFBGA (10mm x 14.5mm, seated height: 0.95mm MAX)	NQ
• Speed grade, cycle time	
- 1866MHz / 3732Mbps	-053
• Operating temperature range	
- 0^0C to +70^0C	BT

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate per Pin (Mb/s)	Array Configuration	WRITE Latency		READ Latency	
				Set A	Set B	DBI Disabled	DBI Enabled
-053	1866	3732	512 Meg x 32	16	30	32	36
-053	1866	3732	1 Gig x 32	16	30	32	36