N-Channel 60V(D-S) MOSFET

RC2308A

GENERAL DESCRIPTION

The SS2308 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦100mΩ@V_{GS}=10V
- $R_{DS(ON)}$ ≦130mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

Feature

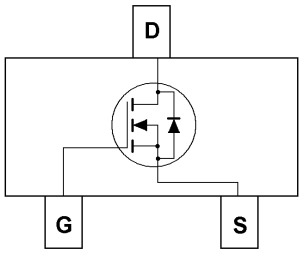
60V/2.6A, $R_{DS(ON)}$ = 80mΩ(MAX) @V_{GS} = 4.5V.

$R_{DS(ON)}$ = 140mΩ(MAX) @V_{GS} =2.5V.

Super High dense cell design for extremely low $R_{DS(ON)}$.

Reliable and Rugged.

SOT-23 for Surface Mount Package.



N-Channel MOSFET

SOT-23

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Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V

Electrical Characteristics (T_j =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
‘$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D= 2.6A		82	100	mΩ
		V_{GS}=4.5V, I_D= 2.1A		96	130	
		V_{GS}=3.3V, I_D= 1.8A		139	200	
V_{SD}	Diode Forward Voltage	I_S=1.0A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_D=2.6A		12		nC
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=4.5V, I_D=2.6A		6.5		
Qgs	Gate-Source Charge			2.2		
Qgd	Gate-Drain Charge			2.7		
Ciss	Input capacitance	V_{DS}=30V, V_{GS}=0V, f=1MHz		350		pF
Coss	Output Capacitance			40		
Crss	Reverse Transfer Capacitance			12		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.7		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=20V, R_L =20Ω I_D=1A, V_{GEN}=10V R_G=1Ω		10		ns
t_r	Turn-On Rise Time			11		
$t_{d(off)}$	Turn-Off Delay Time			29		
t_f	Turn-Off Fall Time			3		

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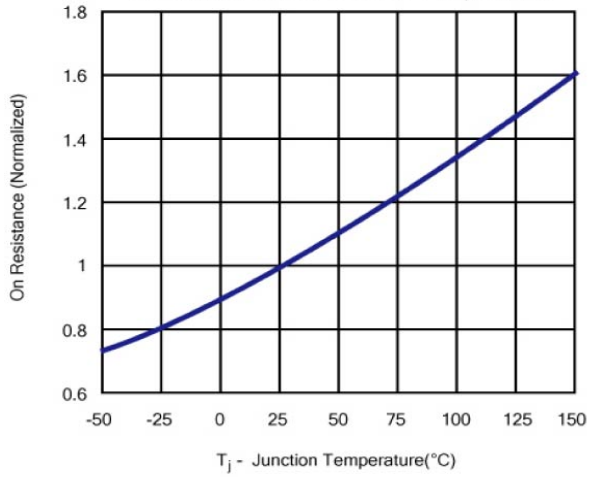
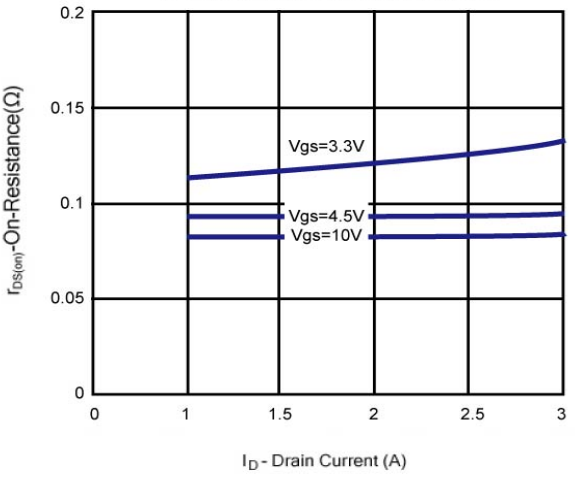
Typical Characteristics (T_J =25℃ Noted)

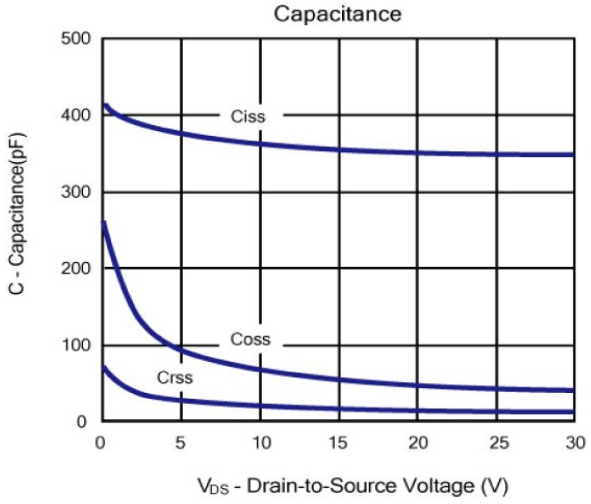
On Resistance vs. Junction Temperature



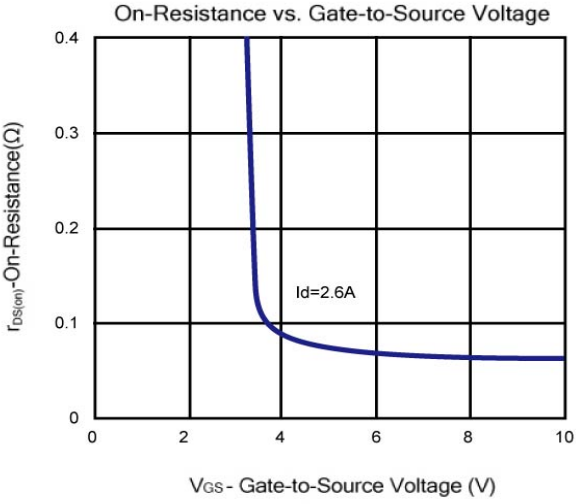
On-Resistance vs. Drain Current



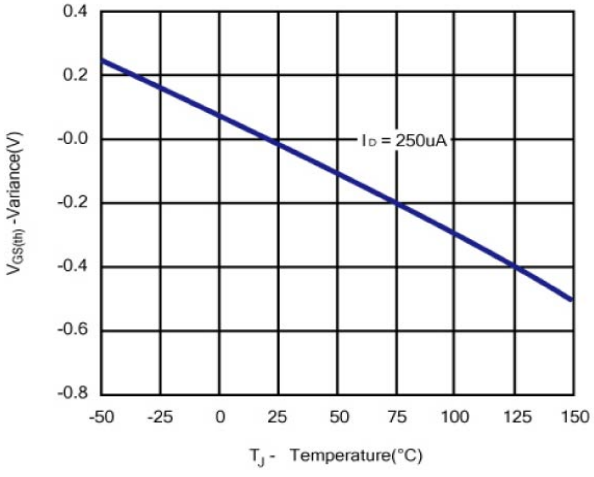
Capacitance



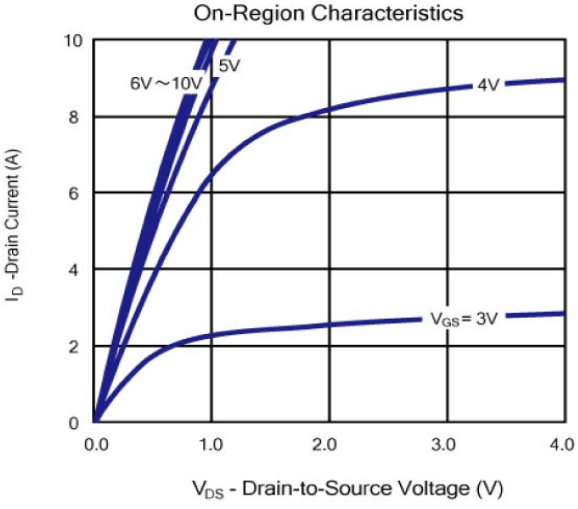
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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