RPC8201F（I）Datasheet

10BASE-T/100BASE-TX
ETHERNET TRANSCEIVER
(CONFIDENTIAL: PARTNERS ONLY)

Revision: 2.0.3

Date: 2021-06-09

RPCOM

Copyright Statement and Disclaimer

CONTENT

- Revision History

Revision	Release Date	Summary
V1.0.0	2019.11.27	First version
V1.1.0	2020.3.27	Add DC Characteristics and Mechanical Dimensions
V2.0.0	2020.10.30	1: Add Functional Description and Characteristics 2: Add EXT Reg Information
V2.0.1	2020.12.18	Table format update for incompletely contents.
V2.0.2	20210205	Add input/output Voltage characters
V2.0.2	20210609	Add ESD Ratings

1 General Description

The RPC8201F is a single-chip/single-port 10/100Mbps Ethernet PHY transceiver that supports:

- MII (Media Independent Interface)
- RMII (Reduced Media Independent Interface)

The RPC8201F implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10Base-TX Encoder/Decoder, and Twisted-Pair Media Access Unit (TPMAU). The RPC8201F support auto MDIX.

The RPC8201F uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT5 twisted-pair cable.

The RPC8201F offers integrated built-in self-test and loopback capabilities for ease of use, and innovative and robust approach for reducing power consumption through EEE and WoL.

2 Features

- Supports MII mode
- Supports RMII mode
- Full/half duplex operation
- Supports Auto-Negotiation
- Supports IEEE 802.3az-2010 (EEE)
- 100Base-TX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- Supports auto MDIX
- Supports Interrupt function
- Supports Wake-On-LAN (WOL)
- Adaptive Equalization
- Automatic Polarity Correction
- LEDs
- Supports 25MHz external crystal or OSC
- Supports 50MHz external OSC Clock input
- Provides 50MHz clock source for MAC
- Low power supply 1.1V and 3.3V; 1.1V is generated by an internal regulator
- 0.11 μ m CMOS process
- Packages QFN32

3 Applications

- DTV (Digital TV)
- MAU (Media Access Unit)
- Game Console
- CNR (Communication and Network Riser)
- IPC
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch

In addition, the RPC8201F can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection .

3 .1 Block Diagram

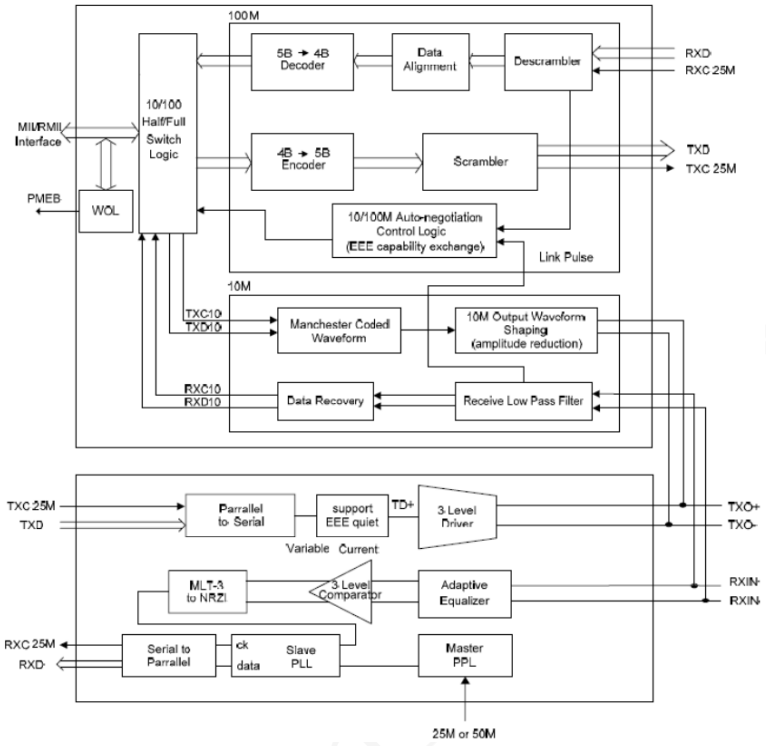


Figure 3-1 Block Diagram

3 .2 Application Diagram

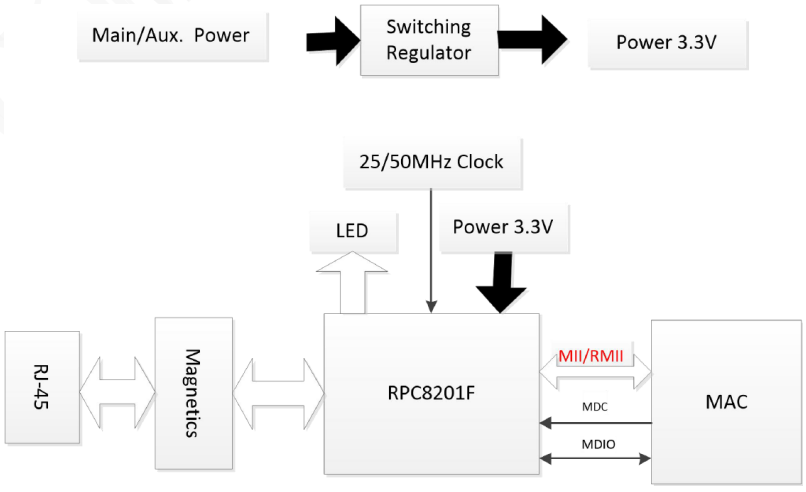


Figure 3-2 Block Diagram

4 Pin Assignment

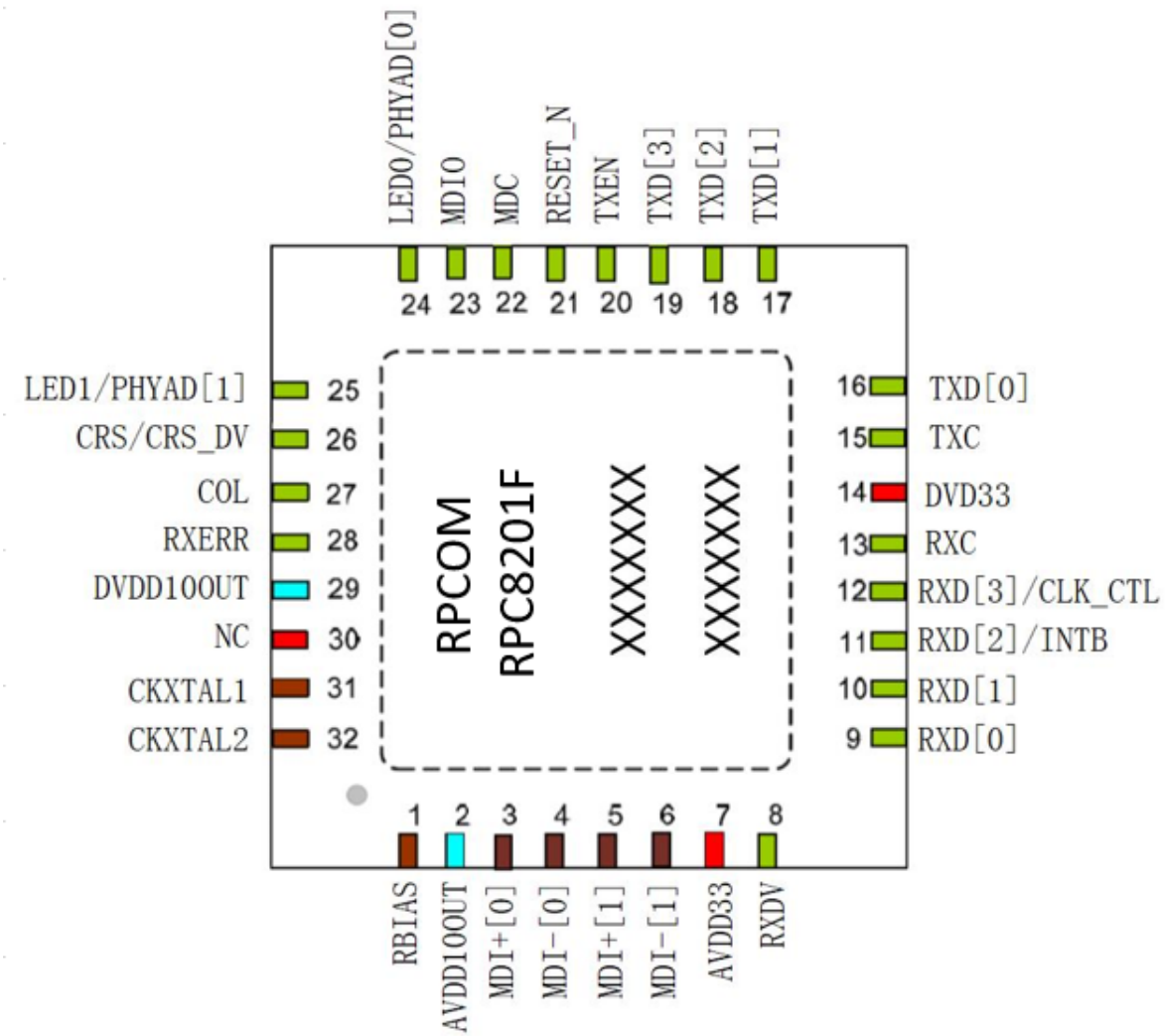


Figure 4-1 RPC8201F Pin Assignment

5 Pin Description

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open-drain output
- OT = Tristateable signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR = Sample on reset
- XT = Crystal inputs/outputs pin type
- PWR= Power related
- B = Bias

Table 1. Pin Description

NO.	NAME	TYPE	DESCRITION
1	RBIAS	I	Bias Resistor. A 2.49 kΩ±1% resistor is connected between the RBIAS pin and GND
2	AVDD10OUT	PWR/O	Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
3 4	MID+[0] MDI-[0]	IO IO	Transmit Output. Differential transmit output pair shared by 100Base-TX and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform.
5 6	MID+[1] MDI-[1]	IO IO	Receive Input. Differential receive input pair shared by 100Base-TX and 10Base-T modes.
7	AVDD33	PWR	3.3V Analog Power Input.
8	RX_DV	O/PD	Receive Data Valid. Power On Strapping for MII/RMII selection. 0: MII mode 1: RMII mode

9	RXD[0]	O/PD	Receive Data [0]
10	RXD[1]	O/PD	Receive Data [1]
11	RXD[2]/INTB	O/PD	Receive Data [2] When in RMII mode, this pin is used for the interrupt function.
12	RXD[3]/CLK_CTL	O/PD	Receive Data [3] RXD[3]/CLK_CTL pin is the Power On Strapping in RMII Mode. 1: REF_CLK input mode, RMII1 mode 0: REF_CLK output mode, RMII2 mode
13	RXC	O/PD	Receive Clock.
14	DVDD33	PWR	3.3V Digital Power Input.
15	TXC	IO/PD	MII Mode Transmit Clock.
16	TXD[0]	I/PD	Transmit Data [0]
17	TXD[1]	I/PD	Transmit Data [1]
18	TXD[2]	I/PD	Transmit Data [2]
19	TXD[3]	I/PD	Transmit Data [3]
20	TX_EN	I/PD	MII/RMII Mode Transmit Enable.
21	RESET_N	I/HZ	RESET. Active-low, reset pin for chip.
22	MDC	I/PU	Management Data Clock. This pin provides a clock
23	MDIO	IO/PU	Management Data Input/Output.
24	LED0/ PHYAD[0]	O/PD	LED 0, Link 10Mpbs On, Active blink. PHY address 0 selection
25	LED1/ PHYAD[1]	O/PD	LED 1, Link 100Mpbs On, Active blink. PHY address 1 selection
26	CRS/CRS_DV	O/PD	MI mode: Carrier Sense. RMII mode: Carrier Sense/Receive Data Valid.
27	COL	O/PD	Collision Detect.
28	RXER	O/PD	Receive Error.
29	DVDDL_REG	PWR/O	DVDDL Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
30	NC		NC
31	XTAL_IN	I/XT	25 MHz Crystal Input Pin.Or tie to GND
32	XTAL_OUT	O/XT	25 MHz Crystal Output Pin, Or Oscillator25M/50MHz Input
EPAD	GND		GND

5.1 RMII Interface

Table 2. RMII Interface

PIN Name	PIN No.	Type	Description
TXC	15	IO/PD	50MHz reference clock for Receive, Transmit . Clock Input/Output Derection is decided by PIN12: RXD[3]/CLK-CTL: 0: Ouput Mode 1: Input Mode
CRS/CRS_DV	26	O/PD	Carrier Sense/Receive data valid CRS_DV ouput will be asserted by the PHY when the receive medium is no-Idle.
TXEN			Transmit Enable
RXER	28		Receive Error(Optional input for MAC)
TXD[0:1]/RXD[0:1]	16,17/9,10		Transmit/Receive Data

NOTE: FOR RMII_REF_CLK SETTING DETAIL, PLEASE REFER TO 'APPNOTE0001-RPC8201F'.

5.2 Power On Strapping

Table 3. Strapping Setting

PIN Name	PIN No.	Default	Description
RX_DV	8	PD	Mode Selection, 0 MII 1 RMII
RXD[3]/CLK_CTL	12	PD	RMII Mode Reference CLK setting For Pin15: 0 output Mode 1 input Mode
RXD[1]	10	PD	Wol_led_sel, determines the PAD LED0 working as LED0 or WOL. 0 LED0 works as LED0. 1 LED0 works as PMEB (WOL interrupt),Pin 24 must external pull up.

5.3 PHY Address Setting

Table 4. PAY Address

PIN Name	PIN No.	Default	Description
LED1/ PHYAD[1] LED0/ PHYAD[0]	25 24	00	Up to 4 PHY device valid, The PHY address are: 00, 0110 and 11

6 Register Description

The RPC8201F transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 2.5 MHz must drive the MDC pin of the RPC8201F. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

Notation	Description
RW	Read and write
SC	Self-clear
RO	Read only
LH	Latch high
RC	Read clear
SWC	Software reset clear

6.1 Mii registers

6.1.1 00h: control register (0x1140h)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	1'b0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	1'b0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback
13	Speed_Selection(LSB)	RW	1'b0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	1'b1	1: to enable auto-negotiation; 0: auto-negotiation is disabled.

11	Power_down	RW SWC	1'b0	=1: Power down =0: Normal operation When the port is switched from power down to normal operation, software reset and Auto- Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW SWC	1'b0	Isolate phy from MII/RMII: PHY will not respond to xMII TXD/TX_EN, and present high impedance on RXD/RX_DV. 1'b0: Normal mode 1'b1: Isolate mode
9	Re_Autoneg	RW SWS SC	1'b0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART. =1: Restart Auto-Negotiation Process =0: Normal operation
8	Duplex_Mode	RW	1'b1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0. =1: Full Duplex =0: Half Duplex

7	Collision_Test	RW SWC	1'b0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. =1: Enable COL signal test =0: Disable COL signal test
6	Speed_ Selection(MSB)	RW	1'b1	See bit13.
5:0	Reserved	RO	5'b0	Reserved. Write as 0, ignore on read

6.1.2 01h: status register

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	1'b0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	1'b1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	1'b1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	1'b1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	1'b1	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	1'b0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	1'b0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	1'b1	Whether support extended status register in 0Fh 0: Not supported 1: Supported

7	Unidirect_Ability	RO	1'b0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1'b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	1'b1	1'b0: PHY will not accept management frames with preamble suppressed 1'b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	1'b0	1'b0: Auto-negotiation process not completed 1'b1: Auto-negotiation process completed
4	Remote_Fault	RO RC SWC LH	1'b0	1'b0: no remote fault condition detected 1'b1: remote fault condition detected
3	Autoneg_Ability	RO	1'b1	1'b0: PHY not able to perform Auto-negotiation 1'b1: PHY able to perform Auto-negotiation
2	Link_Status	RO LL SWC	1'b0	Link status 1'b0: Link is down 1'b1: Link is up
1	Jabber_Detect	RO RC LH SWC	1'b0	10Baset jabber detected 1'b0: no jabber condition detected

				1'b1: Jabber condition detected
0	Extended_Capability	RO	1'b1	To indicate whether support EXTs, to access from address register 1Eh and data register 1Fh 1'b0: Not supported 1'b1: Supported

6.1.3 02h: PHY identification register1 (0x0000h)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	16'b0	Bits 3 to 18 of the Organizationally Unique Identifier

6.1.4 03h: PHY identification register2 (0x0128h)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	6'b0	OUI_LSB, Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	6'h11/6'h12	Model Number
3:0	Revision_No	RO	4'h8	4 bits manufacturer's revision number

6.1.5 04h: Auto-Negotiation advertisement

Bit	Symbol	Access	Default	Description

15	Next_Page	RW	1'b0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed. =1: Advertise =0: Not advertised
14	Reserved	RO	1'b0	Reserved
13	Remote_Fault	RW	1'b0	=1: Set Remote Fault bit =0: Do not set Remote Fault bit
12	Extended_Next_Page	RW	1'b1	Extended next page enable control bit =1: Local device supports transmission of extended next pages

				=0: Local device does not support transmission of extended next pages.
11	Asymmetric_Pause	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Asymmetric Pause =0: No asymmetric Pause
10	Pause	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal

				operation by writing register 0x0 bit[11] • Link goes down =1: MAC PAUSE implemented =0: MAC PAUSE not implemented
9	100BASE-T4	RO	1'b0	=1: Able to perform 100BASE-T4 =0: Not able to perform 100BASE-T4 Always 0
8	100BASE-TX_Full_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
7	100BASE-TX_Half_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:

				• Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
6	10BASE-Te_Full_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
5	10BASE-Te_Half_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does

				not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
4:0	Selector_Field	RW	5'b00001	Selector Field mode. 00001 = IEEE 802.3

6.1.6 05h: Auto-Negotiation link partner ability

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO SWC	1'b0	Received Code Word Bit 15 =1: Link partner is capable of next page =0: Link partner is not capable of next page
14	ACK	RO SWC	1'b0	Acknowledge. Received Code Word Bit 14 =1: Link partner has received link code word =0: Link partner has not received link code word

13	REMOTE_FAULT	RO SWC	1'b0	Remote Fault. Received Code Word Bit 13 =1: Link partner has detected remote fault =0: Link partner has not detected remote fault
12	RESERVED	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 12
11	ASYMMETRIC_PAUSE	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 11 =1: Link partner requests asymmetric pause =0: Link partner does not request asymmetric pause
10	PAUSE	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 10 =1: Link partner supports pause operation =0: Link partner does not support pause operation
9	100BASE-T4	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 9 =1: Link partner supports 100BASE-T4 =0: Link partner does not support100BASE-T4
8	100BASE-TX_FULL_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 8 =1: Link partner supports 100BASE-TX full-duplex =0: Link partner does not support

				100BASE-TX full-duplex
7	100BASE-TX_HALF_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 7 =1: Link partner supports 100BASE-TX half-duplex =0: Link partner does not support 100BASE-TX half-duplex
6	10BASE-Te_FULL_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 6 =1: Link partner supports 10BASE-Te full-duplex =0: Link partner does not support 10BASE-Te full-duplex
5	10BASE-Te_HALF_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 5 =1: Link partner supports 10BASE-Te half-duplex =0: Link partner does not support 10BASE-Te half-duplex
4:0	SELECTOR_FIELD	RO SWC	5'h0	Selector Field Received Code Word Bit 4:0

6.1.7 06h: Auto-Negotiation expansion register

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	11'h0	Always 0
4	Parallel_Detection_fault	RO RC LH SWC	1'b0	=1: Fault is detected =0: No fault is detected
3	Link_partner_next_page able	RO LH	1'b0	=1: Link partner

		SWC		supports Next page =0: Link partner does not support next page
2	Local_Next_Page_able	RO	1'b1	=1: Local Device supports Next Page =0: Local Device does not Next Page
1	Page_received	RO RC LH	1'b0	=1: A new page is received =0: No new page is received
0	Link_Partner_Auto_negotiation_able	RO	1'b0	=1: Link partner supports auto-negotiation =0: Link partner does not support auto-negotiation

6.1.8 07h: Auto-Negotiation Next Page register

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	1'b0	Transmit Code Word Bit 15 =1: The page is not the last page =0: The page is the last page
14	Reserved	RO	1'b0	Transmit Code Word Bit 14
13	Message_page_mode	RW	1'b1	Transmit Code Word Bit 13 =1: Message Page =0: Unformatted Page

12	Ack2	RW	1'b0	Transmit Code Word Bit 12 =1: Comply with message =0: Cannot comply with message
11	Toggle	RO	1'b0	Transmit Code Word Bit 11 =1: This bit in the previously exchanged Code Word is logic 0 =0: The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message_Unformatte D_Field	RW	11'h1	Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.1.9 08h: Auto-Negotiation link partner Received Next Page register

Bit	Symbol	Access	Default	Description
15	Next_Page	RO	1'b0	Received Code Word Bit 15 =1: This page is not the last page =0: This page is the last page
14	Reserved	RO	1'b0	Received Code Word Bit 14
13	Message_page_mode	RO	1'b0	Received Code Word Bit 13 =1: Message Page =0: Unformatted Page
12	Ack2	RO	1'b0	Received Code Word Bit 12 =1: Comply with message =0: Cannot comply with

				message
11	Toggle	RO	1'b0	Received Code Word Bit 11 =1: This bit in the previously exchanged Code Word is logic 0 =0: The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message_Unformatted_Field	RO	11'b0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.1.10 0Ah: MASTER-SLAVE status register

Bit	Symbol	Access	Default	Description
15	Master_Slave_Configuration_Fault	RO RC SWC LH	1'b0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete. =1: Master/Slave configuration fault detected =0: No fault detected
14	Master_Slave_Configuration_Resolution	RO	1'b0	This bit is not valid unless register 0x1 bit5

				is 1. =1: Local PHY configuration resolved to Master =0: Local PHY configuration resolved to Slave
13	Local_Receiver_Status	RO	1'b0	=1: Local Receiver OK =0: Local Receiver not OK Always 0.
12	Remote_Receiver_Status	RO	1'b0	=1: Remote Receiver OK =0: Remote Receiver not OK Always 0.
11	Link Partner_ 1000Base-T_Full_Duplex_Capability	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. =1: Link Partner supports 1000BASE-T half duplex =0: Link Partner does not support

				1000BASE-T half duplex
10	Link_Partner_1000Base-T_Half_Duplex_Capability	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. =1: Link Partner supports 1000Base-T full duplex =0: Link Partner does not support 1000Base-T full duplex
9:8	Reserved	RO	2'b0	Always 0
7:0	Idle_Error_Count	RO SC	8'b0	Always 0.

6.1.11 0Dh: MMD access control register

Bit	Symbol	Access	Default	Description
15:14	Function	RW	2'b0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	9'b0	Always 0
4:0	DEVAD	RW	5'b0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

6.1.12 0Eh: MMD access data register

Bit	Symbol	Access	Default	Description
15:0	Address_data	RW	16'b0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

6.1.13 0Fh: Extended status register

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO	1'b0	PHY not able to support 1000Base-X_Fd
14	1000Base-X_Hd	RO	1'b0	PHY not able to support 1000Base-X_Hd
13	1000Base-T_Fd	RO	1'b0	PHY not able to support 1000Base-T_Fd
12	1000Base-T_Hd	RO	1'b0	PHY not able to support 1000Base-T_Hd
11:8	Reserved	RO	1'b0	Reserved
7	100Base-T1	RO	1'b1	Reserved
6	1000Base-T1	RO	1'b0	Reserved
5:0	Reserved	RO	6'b0	Reserved

6.1.14 10h: PHY specific function control register

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	9'b0	Always 0.
6:5	Cross_md	RW	2'b11	Changes made to these bits disrupt normal operation, thus a software

				reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Int_polar_sel	RW	1'b0	No use.
3	Crs_on_tx	RW	1'b0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: =1: Assert CRS on transmitting or receiving =0: Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	1'b0	=1: SQE test enabled =0: SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.
1	En_pol_inv	RW	1'b1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. =1: Polarity Reversal Enabled =0: Polarity Reversal Disabled
0	Dis_jab	RW	1'b0	Jabber takes effect only in 10BASE-Te half-duplex mode. =1: Disable jabber function =0: Enable jabber function

6.1.15 11h: PHY specific status register

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	2'b00	These status bits are valid only when any bit in bit9:7 and bit3:2 is 1. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	1'b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. =1: Full-duplex =0: Half-duplex
12	Page_Received_real-time	RO	1'b0	=1: Page received =0: Page not received
11	Speed_and_Duplex_Resolved	RO	1'b0	When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode. =1: Resolved =0: Not resolved
10	Link_status_real-time	RO	1'b0	=1: Link up =0: Link down
9	En_fe_100	RO	1'b1	Always 1.
8	En_fe_10	RO	1'b1	Always 1.
7	Lds_en_autoneg	RO	1'b1	Always 1.
6	MDI_Crossover_Status	RO	1'b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-

				Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 "PHY specific function control register" bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. =1: MDIX =0: MDI
5	Wirespeed_downgrade	RO	1'b0	=1: Downgrade =0: No Downgrade
4	Reserved	RO	1'b0	Always 0.
3	En_ae_100	RO	1'b0	Always 0.
2	En_ae_10	RO	1'b0	Always 0.
1	Polarity_Real_Time	RO	1'b0	=1: Reverted polarity =0: Normal polarity
0	Jabber_Real_Time	RO	1'b0	=1: Jabber is asserted. =0: No jabber

6.1.16 12h: Interrupt Mask Register

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation_Error_int _mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
14	Speed_Changed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
13	Duplex_changed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable

12	Page_Received_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
11	Link_Failed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
10	Link_Succeed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
9	Reserved	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
8	Reserved	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
7	Reserved	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
6	WOL_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
5	Wirespeed_downgraded_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
4:2	Reserved	RW	3'b0	No used.
1	Polarity_changed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
0	Jabber_Happened_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable

6.1.17 13h: Interrupt Status Register

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation_Error_INT	RO RC	1'b0	Error can take place when any of the following happens: • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD

				• Link does not come up after negotiation is complete • Selector Field is not equal • flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state =1: Auto-Negotiation Error takes place =0: No Auto-Negotiation Error takes place
14	Speed_Changed_INT	RO RC	1'b0	=1: Speed changed =0: Speed not changed
13	Duplex_changed_INT	RO RC	1'b0	=1: duplex changed =0: duplex not changed
12	Page_Received_INT	RO RC	1'b0	=1: Page received =0: Page not received
11	Link_Failed_INT	RO RC	1'b0	=1: Link down takes place =0: No link down takes place
10	Link_Succeed_INT	RO RC	1'b0	=1: Link up takes place =0: No link up takes place
9	Reserved	RO	1'b0	Always 0.
8	Reserved	RO	1'b0	Always 0.
7	Reserved	RO	1'b0	Always 0.
6	WOL_INT	RO RC	1'b0	=1: PHY received WOL magic frame. =0: PHY didn't receive WOL magic frame.

5	Wirespeed_downgraded_INT	RO RC	1'b0	=1: speed downgraded. =0: Speed didn't downgrade.
4:2	Reserved	RO	3'b0	Always 0.
1	Polarity_changed_INT	RO RC	1'b0	=1: PHY revered MDI polarity =0: PHY didn't revert MDI polarity
0	Jabber_Happened_INT	RO RC	1'b0	=1: 10BaseT TX jabber happened =0: 10BaseT TX jabber didn't happen

6.1.18 14h: Speed Auto Downgrade Control Register

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	4'b0	Always 0.
11	En_mdio_latch	RW	1'b1	=1: To latch MII/MMD register's read out value during MDIO read =0: Do not latch MII/MMD register's read out value during MDIO read
10	Start_autoneg	RW SC	1'b0	Set it to cause PHY to restart auto-negotiation.
9	Reverse_autoneg	RW	1'b0	=1: reverse the autoneg direction, 10Mb/s has 1st priority, then 100Mb/s and at last 1000Mb/s. =0: normal autoneg direction.
8	Dis_giga	RW	1'b0	=1: disable advertise Giga ability in autoneg; =0: don't disable, so PHY advertises Giga ability based on MII register 0x9.
7	Reserved	RW	1'b0	Shall always be written to 0.

				Writing this bit requires a software reset to update.
6	Reserved	RW	1'b0	Shall always be written to 0. Writing this bit requires a software reset to update.
5	En_speed_downgrade	RW	1'b1	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update.
4:2	Autoneg retry limit pre-downgrade	RW	3'b011	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits.
1	Bp_autospd_timer	RW	1'b0	=1: the wirespeed downgrade FSM will bypass the timer used for link stability check; =0: not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1.
0	Reserved	RO	1'b0	Always 0.

6.1.19 15h: Rx Error Counter Register

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	16'b0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over. If speed mode is 2'b01, it counts for

				fe_100 RX_ER; Else, it's 0.

6.1.20 1eh: EXT Register's Address Offset Register

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Address_Offset	RW	16'h0	It's the address offset of the EXT Reg that will be Write or Read.

6.1.21 1fh: EXT Register's Data Register

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Data	RW	16'h0	It's the data to be written or read to the EXT Register, which is indicated by the address offset in register 0x1E register.

6.2 Extended Register

6.2.1 EXT Reg 0x4000h: Extended Combo Control 1

Bit	Symbol	Access	default	Description
15:13	Reserved	RO	3'b000	
12	Reserved	RW	1'b0	Reserved
11	Remote_Loopback	RW	1'b0	Remote loopback control 1'b0: disable 1'b1: enable
10:9	Reserved	RW	2'b0	Reserved

8	Reserved	RW	1'b0	Reserved
7:6	Reserved	RW	2'b00	Reserved
5	Jumbo_Enable	RW	1'b0	Enable Jumbo frame reception up to 18KB frame, when disabled only up to 4.5KB frame supported 0: disable jumbo frame reception 1: enable jumbo frame reception
4	Rmii_RX_DV_sel	RW	1'b0	Drive PAD CRS_DV of RMII by CRS_DV or RX_DV. 0: by CRS_DV 1: by RX_DV
3	Reserved	RW	1'b0	Reserved
2	Wol_en	RW	1'b0	1: enable WOL mechanism. 0: disable WOL.
1	Rmii_en	RW	1'b0	Its default value is determined by power on strapping. 1: enable RMII mode; 0: disable RMII mode.
0x	Clk_sel]]]]	RW	1'b0	Its default value is determined by power on strapping. 1: input TXC/RXC; 0: output TXC/RXC. [rmii_en, clk_sel]: 2'b00: MII mode; 2'b01: REMII mode; 2'b10: RMII2 mode; 2'b11: RMII1 mode.

6.2.2 EXT Reg 0x4001h : Extended Pad Control

Bit	Symbol	Access	default	Description
15	Output_int_or_wol	RW	1'b1	RPC8201F, control to output general INTn or WOL INTn to PAD LED0_INTN_PMEB, when power on strapping value of RXD[1] is 1. 1'b1: output general INTn; 1'b0: output WOL INTn.
14:8	Reserved	RW	7'b0	Reserved
7:6	Reserved	RW	2'b11	Reserved
5:4	Xmii_Dr	RW	2'b10	XMII interface driver strength control in non-scan mode.
3:2	Mdio_Dr	RW	2'b11	MDIO pin driver strength control in non-scan mode.
1:0	Reserved	RW	2'b11	Reserved

6.2.3 EXT Reg 0x4003h: Extended Combo Control 2

Bit	Symbol	Access	default	Description
15	Reserved	RW	1'b0	Reserved
14	Slave_jitter_test	RW	1'b0	Mux clk_dac to rxc in slave jitter test mode 1: enable 0: disable
13:10	Reserved	RW	4'b0	Reserved

9:7	Wol_lth_sel	RW	3'b100	Wol_lth_sel[0] control WOL INTn to be a level or a pulse. 1'b1: a pulse; 1'b0: a level. Wol_lth_sel[2:1] control WOL INTn pulse width when Wol_lth_sel[0] is 1. 2'b00: 10us; 2'b01: 100us; 2'b10: 1ms; 2'b11: 10ms.
6	En_isolate_txc	RW	1'b1	When isolate (mii.0.10) is 1, control to make TXC input or not. 1'b1: input; 1'b0: keep TXC previous direction.
5	En_isolate_rxc	RW	1'b1	When isolate (mii.0.10) is 1, control to make RXC input or not. 1'b1: input; 1'b0: keep RXC previous direction.
4:0	Reserved	RW	5'b01111	Reserved

6.2.4 EXT Reg 0x4004h: WOL MAC ADDRESS

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[47:32]	RW	16'b0	WOL MAC Address

6.2.5 EXT Reg 0x4005h: WOL MAC ADDRESS

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[31:16]	RW	16'b0	WOL MAC Address

6.2.6 EXT Reg 0x4006h: WOL MAC ADDRESS

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[15:0]	RW	16'b0	WOL MAC Address

6.2.7 EXT Reg 0x40A0h: PKG_ SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15	Pkg_chk_en	RW	1'b0	1: to enable RX/TX package checker. RX checker checks the MII data at transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX.
14	Pkg_en_gate	RW	1'b1	1: To enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0; 0: Not gate the clocks.
13	Bp_pkg_gen	RW	1'b1	1: normal mode, to send xMII TX data from PAD; 0: test mode, to send out the MII data generated by pkg_gen module.

12	Pkg_gen_en	RW SC	1'b0	1: To enable pkg_gen generating MII packages. But the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0. If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0; Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared.
11:8	Pkg_prm_lth	RW	4'8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	Pkg_ipg_lth	RW	4'd12	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Xmit_mac_force_gen	RW	1'b0	1: To enable pkg_gen to send out the generated data even when the link is not established.

2	Pkg_corrupt_crc	RW	1'b0	1: to make pkg_gen to send out CRC error packages. 0: pkg_gen sends out CRC good packages.
1:0	Pkg_payload	RW	2'b0	Control the payload of the generated packages. 00: increased Byte payload; 01: random payload; 10: fix pattern 0x5AA55AA5… 11: reserved.

6.2.8 EXT Reg 0x40A1h: PKG_ SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:0	Pkg_length	RW	16'd64	To set the length of the generated

6.2.9 EXT Reg 0x40A2h: PKG_ SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:0	Pkg_burst_size	RW	16'b0	To set the number of packages in a burst of package generation. 0: continuous packages will be generated.

6.2.10 EXT Reg 0x40A3h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description

15:0	Pkg_ib_valid_high	RO	16'b0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.2.11 EXT 40A4H: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_low	RO	16'b0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.2.12 EXT Reg 0x40A5h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_high	RO	16'b0	Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.2.13 EXT Reg 0x40A6h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_low	RO	16'b0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.2.14 EXT 40A7H: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_high	RO	16'b0	Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are<64Byte.

6.2.15 EXT 40A8H: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_low	RO	16'b0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.2.16 EXT 40A9H: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_err	RO	16'b0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.2.17 EXT 40AAH: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_bad	RO	16'b0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte.

6.2.18 EXT Reg 0x40ABh: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_frag	RO	16'b0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

6.2.19 EXT Reg 0x40ACh: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_nosfd	RO	16'b0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

6.2.20 EXT Reg 0x40ADh: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_high	RO	16'b0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.2.21 EXT Reg 0x40AEh: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_low	RO	16'b0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.2.22 EXT Reg 0x40AFh: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_high	RO	16'b0	Pkg_ob_os_good [31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.2.23 EXT Reg 0x40B0h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_low	RO	16'b0	Pkg_ob_os_good [15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.2.24 EXT Reg 0x40B1h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_high	RO	16'b0	Pkg_ob_us_good [31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

6.2.25 EXT 40B2 H: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_low	RO	16'b0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.2.26 EXT Reg 0x40B3h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_err	RO	16'b0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.2.27 EXT Reg 0x40B4h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_bad	RO	16'b0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >=1518Byte.

6.2.28 EXT Reg 0x40B5h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_frag	RO	16'b0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

6.2.29 EXT Reg 0x40B6h: PKG_ SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_nosfd	RO	16'b0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

6.2.30 EXT Reg 0x40B7h: PKG_ SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:1	Reserved	RO	15'b0	Reserved.
1	Pkgchk_txsrc_sel	RW	1'b0	Control the source of packages for pkg checker in TX direction to check. 1'b1: from pkg_gen; 1'b0: from xMII TX interface.
0	Pkgen_en_az	RW	1'b0	To send AZ LPI pattern during IPG of the packages sent by pkg_gen.

6.2.31 EXT Reg 0x40B8h: PKG_ SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5'b0	Reserved
10:0	Pkgen_pre_az_t	RW	11'b0	Control the IDLE time after traffic and before sending LPI_IDLE, in unit us. For Giga mode, only Pkgen_pre_az_t[8:0] is valid.

6.2.32 EXT Reg 0x40B9h: PKG_ SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5'b0	No use.

10:0	Pkgen_in_az_t	RW	11'b0	Control the time sending LPI_IDLE, in unit us. For Giga mode, only Pkgen_in_az_t[8:0] is valid.

6.2.33 EXT Reg 0x40BAh: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5'b0	No use.
10:0	Pkgen_aft_az_t	RW	11'b0	Control the IDLE time from end of LPI_IDLE to the beginning of next package. For Giga mode, only Pkgen_in_az_t[8:0] is valid.

6.2.34 EXT Reg 0x40C0h: LED0 CONTROL

Bit	Symbol	Access	default	Description
15	Led_force_en	RW	1'b0	To enable LED force mode.
14:13	Led_force_mode	RW	2'b0	Valid when bit15 led_force_en is set. 00 = force LED OFF; 01 = force LED ON; 10 = force LED to blink at Blink Mode1; 11 = force LED to blink at Blink Mode2. There are 4 Blink Mode, which are different at blink frequency.

12	Led_act_blk_ind	RW	1'b0	When traffic is present, make LED BLINK no matter the previous LED status is ON or OFF, or make LED blink only when the previous LED is ON. when any *_blk_en in bit9~8 and bit3~1 is set and chip do work at corresponding status, =1: LED will blink, no matter bit11~10 (duplex control) and bit5~4 (speed control) are 1 or 0; =0: LED will not blink, unless one (more) of bit11~10 (duplex control) and bit5~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);.
11	Led_fdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up and duplex mode is full duplex, =1: make LED ON; =0: don't make LED ON;
10	Led_hdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up and duplex mode is half duplex, 1: make LED ON; 0: don't make LED ON;

9	Led_txact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, 1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; 0: don't make LED BLINK.
8	Led_rxact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don't make LED BLINK.
7	Led_txact_on_en	RW	1'b0	=1: If BLINK status is not activated, when PHY link up and TX is active, make LED ON at least 10ms;
6	Led_rxact_on_en	RW	1'b0	=1: If BLINK status is not activated, when PHY link up and RX is active, make LED ON at least 10ms;
5	Led_ht_on_en	RW	1'b0	=1: If BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED ON;
4	Led_bt_on_en	RW	1'b1	1 enable: If BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED ON;
3	Led_col_blk_en	RW	1'b0	1 enable: If PHY link up and collision happen, make LED BLINK at Blink mode 0 or 1 based on 40C1h bit6 col_blk_sel;

2	Led_ht_blk_en	RW	1'b0	1 enable: if PHY link up and speed mode is 100Mbps, make LED blink at blink mode 2;
1	Led_bt_blk_en	RW	1'b0	1 enable: If PHY link up and speed mode is 10Mbps, make LED BLINK at Blink mode 3;
0	Dis_led_an_try	RW	1'b1	when PHY is active and auto-negotiation is at LINK_GOOD_CHECK status, =1: LED will be on; =0: LED will be off.

6.2.35 EXT 40C1 H: LED0/1 CONTROL

Bit	Symbol	Access	default	Description
15:10	Reserved	RO	6'b0	Always 0.
9	Invert_led_duty	RW	1'b0	=1: To invert the duty cycle of ON and OFF, namely make LED ON time short and OFF time long.
8	Lpbk_led_dis	RW	1'b0	1: In internal loopback mode, LED will not blink; 0: In internal loopback mode, LED will still blink if it's configured to blink on activity.
7	Jabber_led_dis	RW	1'b1	1: When 10Mbps Jabber happens, LED will not blink; 0: When 10Mbps Jabber happens, LED will still blink if it's configured to blink on TX.

6	Col_blk_sel	RW	1'b1	1: When collision happens, LED blink at Blink Mode2 with higher frequency; 0: When collision happens, LED blink at Blink Mode1 with lower frequency;
5	En_led_act_level	RW	1'b0	1: To make LED blink at different frequency (Blink mode 0) when traffic weight is high. 0: To make LED blink always at Blink mode 1 no matter what the traffic weight is.
4:0	Led_act_level_th	RW	5'd12	Traffic is heavy or not's threshold. RX/TX traffic is monitored separately. In 1s interval, if RX or TX traffic active time > Led_act_level_th*42ms, then the traffic is heavy; otherwise, traffic is not heavy.

6.2.36 EXT 40C2 H: LED0/1 CONTROL

Bit	Symbol	Access	default	Description
15:12	Freq_sel_c0	RW	4'd14	Control the LED blink frequency in Blink mode 0. ON/OFF duty cycle could be reverted by 40C1h bit9 invert_led_duty. Below description is the default ON/OFF cycle, that is invert_led_duty=0. 4'd0=LED blink once every 10s, 6% OFF; 4'd1=LED blink once every 9.4s, 7% OFF; 4'd2=LED blink once every 8s, 8% OFF; 4'd3=LED blink once every 7.4s, 9% OFF; 4'd4=LED blink once every 6s, 11% OFF; 4'd5=LED blink once every 5s, 6% OFF; 4'd6=LED blink once every 4s, 8% OFF; 4'd7=LED blink once every 3s, 11% OFF; 4'd8=LED blink once every 2s, 16% OFF; 4'd9=LED blink once every 1s, 16% OFF; 4'd10=LED blink at 2Hz, 50% OFF; 4'd11=LED blink at 3Hz, 50% OFF; 4'd12=LED blink at 4Hz, 50% OFF; 4'd13=LED blink at 6Hz, 50% OFF; 4'd14=LED blink at 8Hz, 50% OFF; 4'd15=LED blink at 10Hz, 50% OFF;

11:8	Freq_sel_c1	RW	4'd12	Control the LED blink frequency in Blink mode 1. See description in bit15~12 Freq_sel_c0 for detail.
7:4	Freq_sel_c2	RW	4'd7	Control the LED blink frequency in Blink mode 2. See description in bit15~12 Freq_sel_c0 for detail.
3:0	Freq_sel_c3	RW	4'd5	Control the LED blink frequency in Blink mode 3. See description in bit15~12 Freq_sel_c0 for detail.

6.2.37 EXT 40C3 H: LED1 CONTROL

Bit	Symbol	Access	default	Description
15	Led_force_en	RW	1'b0	To enable LED force mode.
14:13	Led_force_mode	RW	2'b0	Valid when bit15 led_force_en is set. 00 = force LED OFF; 01 = force LED ON; 10 = force LED to blink at Blink Mode1; 11 = force LED to blink at Blink Mode2. There are 4 Blink Mode, which are different at blink frequency.

12	Led_act_blk_ind	RW	1'b0	When traffic is present, make LED BLINK no matter the previous LED status is ON or OFF, or make LED blink only when the previous LED is ON. when any *_blk_en in bit9~8 and bit3~1 is set and chip do work at corresponding status, =1: LED will blink, no matter bit11~10 (duplex control) and bit5~4 (speed control) are 1 or 0; =0: LED will not blink, unless one (more) of bit11~10 (duplex control) and bit5~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);.
11	Led_fdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up at FE and duplex mode is full duplex, =1: make LED ON; =0: don't make LED ON;
10	Led_hdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up at FE and duplex mode is half duplex, =1: make LED ON; =0: don't make LED ON;

9	Led_txact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up at either AE or FE and TX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don't make LED BLINK.
8	Led_rxact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up at either AE or FE and RX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don't make LED BLINK.
7	Led_txact_on_en	RW	1'b0	1: If BLINK status is not activated, when PHY link up at either AE or FE and TX is active, make LED ON at least 10ms;
6	Led_rxact_on_en	RW	1'b0	=1: If BLINK status is not activated, when PHY link up at either AE or FE and RX is active, make LED ON at least 10ms;
5	Led_ht_on_en	RW	1'b1	=1: If BLINK status is not activated, when PHY link up at AE or FE and speed mode is 100Mbps, make LED ON;
4	Led_bt_on_en	RW	1'b0	1: If BLINK status is not activated, when PHY link up at AE or FE and speed mode is 10Mbps, make LED ON;
3	Led_col_blk_en	RW	1'b0	1: If PHY link up at FE and collision happen, make LED BLINK at Blink mode 0 or 1 based on 40C1h bit6 col_blk_sel;

2	Led_ht_blk_en	RW	1'b0	1: If PHY link up at AE or FE and speed mode is 100Mbps, make LED BLINK at Blink mode 2;
1	Led_bt_blk_en	RW	1'b0	1: If PHY link up at AE or FE and speed mode is 10Mbps, make LED BLINK at Blink mode 3;
0	Reserved	RO	1'b0	Always 0.

7 Functional Description

The RPC8201F is a physical layer device that integrates 10Base-T and 100Base-TX functions, and some extra power management features. This device supports the following functions:

- MII interface with MDC/MDIO management interface to communicate with the MAC
- IEEE 802.3u Auto-Negotiation ability
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO
- Power Down mode support
- 4B/5B transform
- Scrambling/De-scrambling
- NRZ to NRZI, NRZI to MLT-3
- Manchester Encode and Decode for 10Base-T operation
- Clock and Data recovery
- Adaptive Equalization
- Automatic Polarity Correction
- Network status LEDs
- Wake-On-LAN (WOL)
- Energy Efficient Ethernet (EEE)
- Spread Spectrum Clock (SSC) for RMII REF_CLK output mode

7.1 MII and Management Interface

7.1.1 Data Transition

The MII (Media Independent Interface) is an 18-signal interface (as described in IEEE 802.3u) supplying a standard interface between the PHY and MAC layer.

This interface operates at two frequencies; 25MHz and 2.5MHz, to support 100Mbps/10Mbps bandwidth for both transmit and receive functions.

Transmission

The MAC asserts the TXEN signal. It then changes byte data into 4-bit nibbles and passes them to the PHY via TXD[3:0]. The PHY will sample TXD[3:0] synchronously with TXC – the transmit clock signal supplied by the PHY – during the interval TXEN is asserted.

Reception

The PHY asserts the RXDV signal. It passes the received nibble data RXD[3:0] clocked by RXC. CRS and COL signals are used for collision detection and handling.

In 100Base-TX mode, when the decoded signal in 5B is not IDLE, the CRS signal will assert. When 5B is recognized as IDLE it will be de-asserted. In 10Base-T mode, CRS will assert when the 10M preamble has been confirmed and will be de-asserted when the IDLE pattern has been confirmed.

The RXDV signal will be asserted when decoded 5B are /J/K/ and will be de-asserted if the 5B are /T/R/ or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as the CRS signal.

The RXER (Receive Error) signal will be asserted if any 5B decode errors occur, e.g., an invalid J/K,invalid T/R, or invalid symbol. This pin will go high for one or more clock periods to indicate to thereconciliation sublayer that an error was detected somewhere in the frame.

7.1.2 Serial Management Interface

The MAC layer device can use the MDC/MDIO management interface to control a maximum of 4(RPC8201F) devices, configured with different PHY addresses (00b to 11b for the RPC8201F; Frames transmitted on the MDC/MDIO Management Interface should have the frame structure shown in

Table 5. Management Frame Format

	Management Frame Fields							
	Preamble	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

During a hardware reset, the logic levels of pins 24and 25 are latched to be set as the PHY address for management communication via the serial interface. The read and write frame structure for the management interface is illustrated in Figure8-1 and Figure8-2 as below:

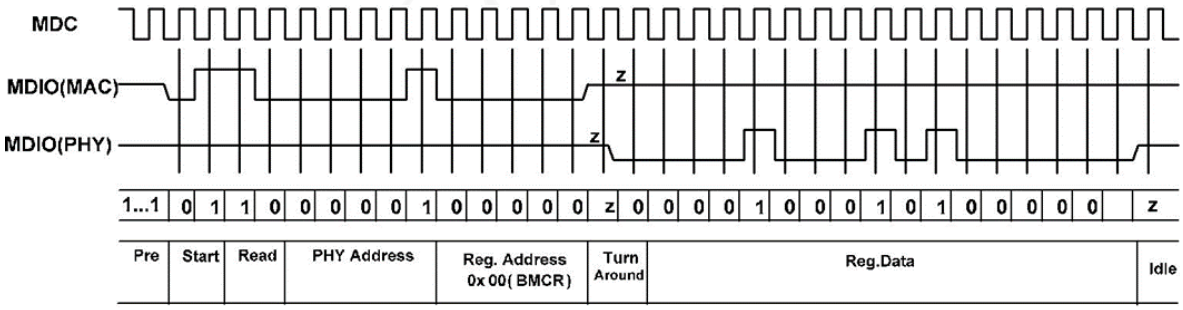


Figure 7-1.Read Cycle

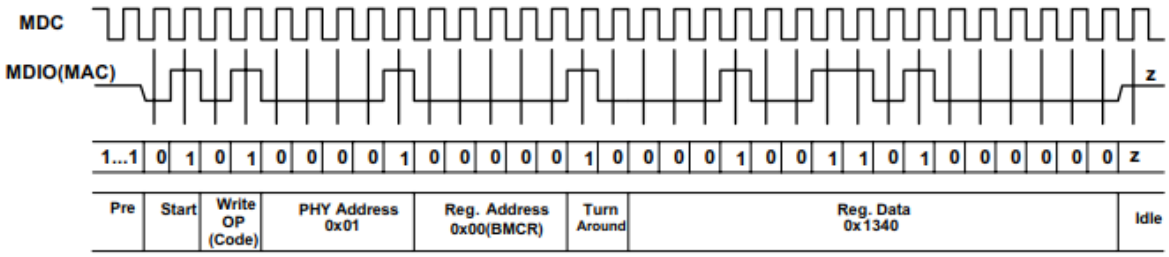


Figure7-2.Write Cycle

Table 6. Serial Management

Name	Description
Preamble	32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

7.2 Interrupt

Whenever there is a status change on the media detected by the RPC8201F, It will drives the interrupt pin (INTB) low to issue an interrupt event. The MAC senses the status change and accesses the Reg 0x13h through the MDC/MDIO interface in response.

Once these status registers Reg0x13 have been read by the MAC through the

MDC/MDIO, the INTB is de-asserted.

Note 1: The RTL8201F RXD[2]/INTB pin (Pin11) is used for the interrupt function only when in the RMII mode.

Note 2: The Interrupt function is disabled by default.

7.3 Auto-Negotiation and Parallel Detection

The RPC8201F supports IEEE 802.3u clause 28 Auto-negotiation for operation with other transceivers supporting auto-negotiation. The RPC8201F can auto-detect the link partner's abilities and determine the highest speed/duplex configuration possible between the two devices. If the link partner does not support auto-negotiation, then the RPC8201F will enable half-duplex mode and enter parallel detection mode. The RPC8201F will default to transmitting FLP (Fast Link Pulse) and wait for the link partner to respond. If the RPC8201F receives a FLP, then the auto-negotiation process will continue. If it receives an NLP (Normal Link Pulse), then the RPC8201F will change to 10Mbps and half-duplex mode. If it receives a 100Mbps IDLE pattern, it will change to 100Mbps and half-duplex mode.

7.3.1 Setting the Medium Type and Interface Mode to MAC

Table 7. Setting the Medium Type and Interface Mode to MAC

FXEN	RXDV	Operation Mode
H	L	Reserved
H	H	Reserved
H	X	Reserved
L	L	UTP Mode and MII Mode
L	H	UTP Mode and RMII Mode
L	X	UTP Mode and MII Mode

7.4 LED Functions

The RPC8201F support two LED signals, in four configurable operation modes. The following sections describe the various LED actions.

7.4.1 LED and PHY Address

As the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example, as Figure 8(left-side) shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g.,4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.

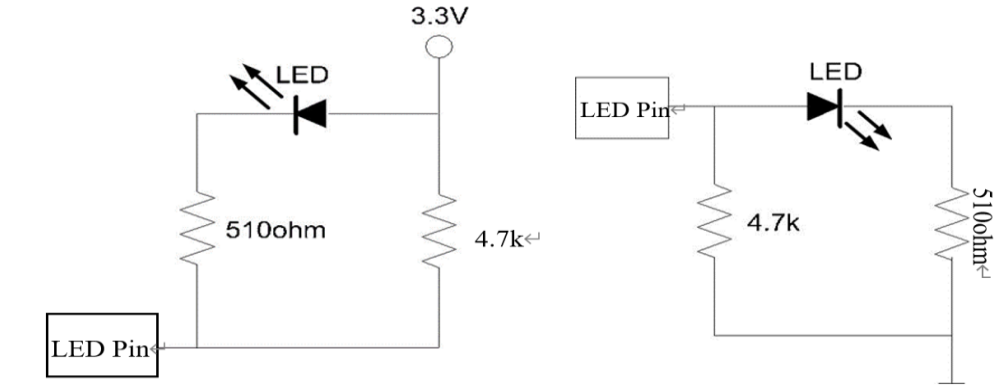


Figure 7-3. LED and PHY Address Configuration

Note: Please strictly follow the LED Logic design showed in Figure8-3.

7.5 Power Down Power Saving Modes

Power Down Power Saving mode operation is supported. This section describes how to implement each mode through software.

Table 8. Power Saving Mode Pin Settings

Mode	Description
PWD	Setting bit 11 of register 0 to 1 puts the RPC8201F into Power Down Mode (PWD). This is the maximum power saving mode while the RPC8201F is still 'live'. In PWD mode, the RPC8201F will turn off all analog/digital functions except the MDC/MDIO management interface. Therefore, if the RPC8201F is put into PWD mode and the MAC wants to recall the PHY, it must create the MDC/MDIO timing by itself (this is done by software).

7.6 10M/100M Transmit and Receive

7.6.1 100Base-TX Transmit and Receive Operation

100Base-TX Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 25MHz (TXC) is transformed into 5B symbol code(4B/5B encoding). Scrambling, serializing, and conversion to 125MHz, and NRZ to NRZI then takes place. After this process, the NRZI signal is passed to the MLT-3 encoder, then to the transmit line driver.

The transmitter will first assert TXEN. Before transmitting the data pattern, it will send a /J/K/ symbol (Start-of-frame delimiter), the data symbol, and finally a /T/R/ symbol known as the End-Of-Frame delimiter. For better EMI performance, the seed of the scrambler is based on the PHY address. In a hub/switch environment, each RPC8201F will have different scrambler seeds and so spread the output of the MLT-3 signals.

100Base-TX Receive

The received signal is compensated by the adaptive equalizer to make up for signal loss due to cable attenuation and Inter Symbol Interference (ISI). Baseline Wander Correction monitors the process and dynamically applies corrections to the process of signal equalization. The Phase Locked Loop (PLL) then recovers the timing information from the signals and from the receive clock. With this, the received signal is sampled to form NRZI (Non-Return-to-Zero Inverted) data. The next steps are the NRZI to NRZ (Non-Return-to-Zero) process, unscrambling of the data, serial to parallel and 5B to 4B conversion, and passing of the 4B nibble to the MII interface.

7.6.2 10Base-T Transmit and Receive Operation

10Base-T Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 2.5MHz (TXC) is first fed to a parallel-to-serial converter, then the 10Mbps NRZ signal is sent to a Manchester encoder. The Manchester encoder converts the 10Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a Start of Idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Finally, the encoded data stream is shaped by a band-limited filter embedded in the RPC8201F and then transmitted.

10Base-T Receive

In 10Base-T receive mode, the Manchester decoder in the RPC8201F converts the Manchester encoded data stream into NRZ data by decoding the data and stripping off the SOI pulse. The serial NRZ data stream is then converted to a parallel 4-bit nibble signal (RXD[0:3]).

7.7 Reset and Transmit Bias

There are two RPC8201F reset types:

Hardware Reset: Pull the PHYRSTB pin high for at least 10ms to access the RPC8201F registers. Pull the PHYRSTB pin low for at least 10ms and then pull high. All registers will return to default values after a hardware reset. The media interface will disconnect and restart the auto-negotiation/parallel detection process.

Software Reset: Set register 0 bit 15 to 1 for at least 20ms to access the RPC8201F registers. A Software reset will only partially reset the registers, and will reset the chip status to 'initializing'.

The RSET pin must be pulled low by a 2.49KΩ resistor with 1% accuracy to establish an accurate transmit bias. This will affect the signal quality of the transmit waveform. Keep its circuitry away from other clock traces and transmit/receive paths to avoid signal interference.

7.8 3.3V Power Supply and Voltage Conversion Circuit

The RPC8201F is fabricated in a 0.11μm process. The core circuit needs to be powered by 1.1V, however, the digital IO and DAC circuits need a 3.3V power supply. Regulators are embedded in the RPC8201F to convert 3.3V to 1.1V.

Note: The internal linear regulator output voltage is 1.1V. The external 1.05V power supply is not suggested for the RPC8201F as the internal regulators cannot be disabled (the RPC8201F does not have an EN_LDO_OUT pin to disable the internal 1.1Vpower supply), and the internal and external power sources may conflict.

As with many commercial voltage conversion devices, the 1.1V output pin of this circuit requires the use of an output capacitor (0.1μF X5R low-ESR ceramic capacitor,1uF +0.1uF capacitor will be better) as part of the device frequency compensation.

The analog and digital ground planes should be as large and intact as possible. If the ground plane is large enough, the analog and digital grounds can be separated, which is the ideal configuration. However, if the total ground plane is not sufficiently large, partition of the ground plane is not a good idea. In this case, all the ground pins can be connected together to a larger single and intact ground plane.
Note: The embedded 1.1V LDO is designed for PHYceiver device internal use only. Do not provide this power to other devices.

7.9 Automatic Polarity Correction

The RPC8201F automatically corrects polarity errors on the receive pairs in 10Base-T mode(polarity is irrelevant in 100Base-TX mode). In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. Detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link goes down.

7.10 Wake-On-LAN (WOL)

The RPC8201F supports automatic detection of a specific frame and notification via dedicated hardware interrupt pin or general PHY interrupt pin. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waked up. The 48-bit MAC address is written in EXT 0x4004, 0x4005, 0x4006 registers.
For example, to write a specific MAC address (0xAABBCCDDEEFF) to PHY, write EXT 0x4004 = 0xAABB, 0x4005 = 0xCCDD, and 0x4006 = 0xEEFF. The PHY internal MAC address can be set to any value.

- NOTE: The MAC address is not a real MAC address and is only a symbol to indicate the content of the frame.

The WOL mechanism is enabled via EXT 0x4000 bit2. POS RXD[1] can't control enable or disable the WOL mechanism but only control pad LED0 working as WOL interrupt.

7.10.1 WOL Interrupt

RPC8201F support dedicated WOL interrupt pin, when the pad RXD[1] is externally PULL UP, pad LED0(pin-24) will work as WOL interrupt.

If EXT 0x4003 bit7 is 0, the dedicated WOL interrupt is programmed to a level, otherwise, it's programed to a pulse; either is active low. When it's programmed to a pulse, the pulse width can be programmed via EXT 0x4003 bit9:8.

WOL interrupt is also wire-and to general PHY interrupt RXD[2]_INTN (pin-11) when the bit6 INT_WOL in Interrupt enable register (MII Register 0x12) is set to 1. If the general PHY interrupt is triggered by WOL, it can be cleared by reading MII register 0x13 bit6.

- NOTE: When general PHY interrupt is used to monitor WOL interrupt, EXT 0x4003 bit7 should be 1, otherwise, the general PHY interrupt can't be read cleared.

8 Characteristics

8.1 DC Characteristics

8.1.1 Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
DVDD33, AVDD33	Supply Voltage 3.3V	-0.4	+3.7	V
DVDD10, DVDD10OUT, AVDD10OUT	Supply Voltage 1.05V*	-0.1	+1.26	V
DC Input	Input Voltage	-0.3	Corresponding Supply Voltage +0.5V	V
DC Output	Output Voltage	-0.3	Corresponding Supply Voltage +0.5V	V
Ts	Storage Temperature	-45	+85	℃

Note: The internal linear regulator output voltage is 1.1V.

8.1.2 Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	DVDD33, AVDD33	3.14	3.30	3.46	V
	DVDD10, DVDD10OUT, AVDD10OUT	1.00	1.05*	1.16	V
Ambient Operating Temperature	-	0	-	70	℃
Maximum Junction Temperature	-	-	-	100	℃

Note: The internal linear regulator output voltage is 1.1V.

8.1.3 Power On and PHY Reset Sequence

The RPC8201F needs 150ms power on time. After 150ms it can access the PHY register from MDC/MDIO.

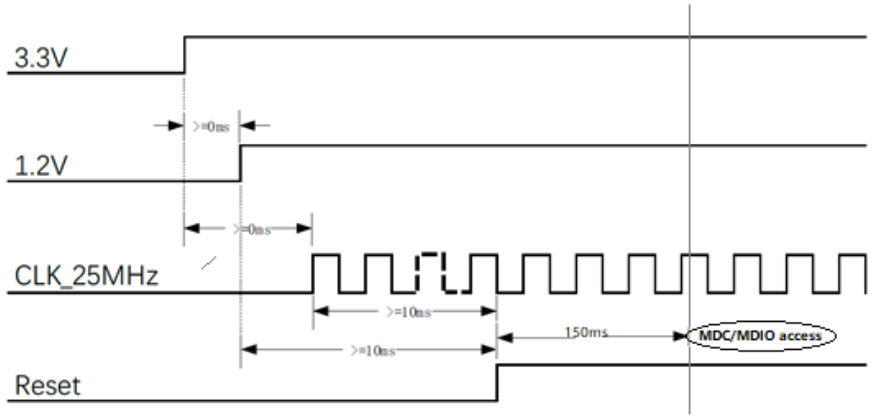


Figure 8-1. Power On and PHY Reset Sequence

Note: 1: 3.3V Power rise time should be at least 100us.

2: For No 25M-Xtal application, PHYRESET must be de-assert at least 10ms after CLOCK signal is stable.

8.1.4 Power Dissipation

The whole system power dissipation (including Internal regulator loss) is shown in table 9:

Table 9. Power Dissipation (Whole System)

Condition	MII	RMII	Unit
RESET	16.5	16.5	mW
PWR Down Mode	18.1	18.1	mW
Active	145.1	144.8	mW
LINK10	79.5	77.6	mW
LINK 100	214.5	199.65	mW
Data Trans 10M	133.7	130.4	mW
Data Trans 100M	214.7	201.5	mW

8.1.5 IO Volatage Level

Table 10. IO Voltage Level

Symbol	Description	Min	Type	Max
Voh 3.3V	High Level Voltage Output	2.4	--	3.6
Vol 3.3V	Low Level Voltage Output	-0.3	--	0.4
Vih 3.3V	High Level Input Voltage	2	--	--
Vil 3.3V	Low Level Input Voltage	--	--	0.8

8.2 AC Characteristics

All output timing assumes equivalent loading between 10pF and 25pF that includes PCB layout traces and other connected devices (e.g., MAC).

8.2.1 MII Transmission Cycle Timing

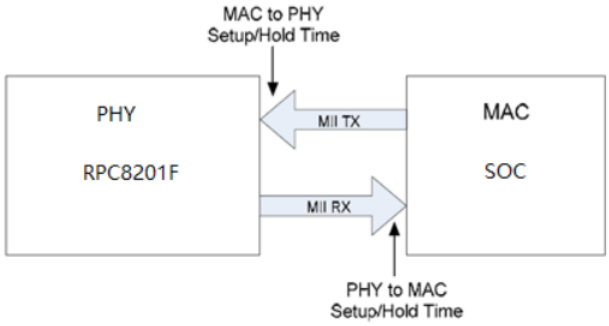


Figure 8-2. MII Interface Setup/Hold Time Definitions

Figure9-3and Figure9-4 show an example of a packet transfer from MAC to PHY on the MII interface.

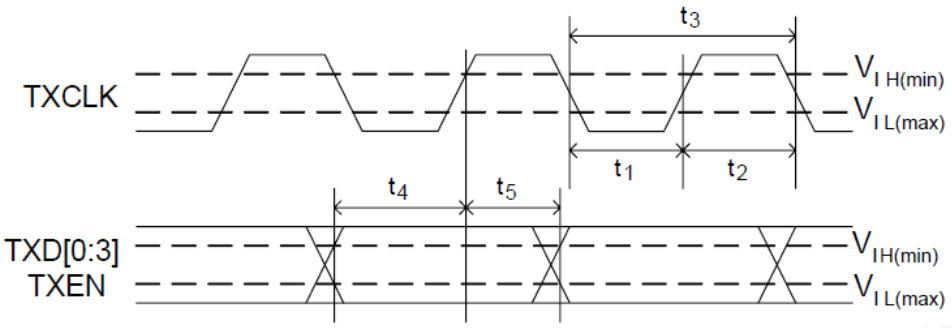


Figure 8-3. MII Transmission Cycle Timing-1

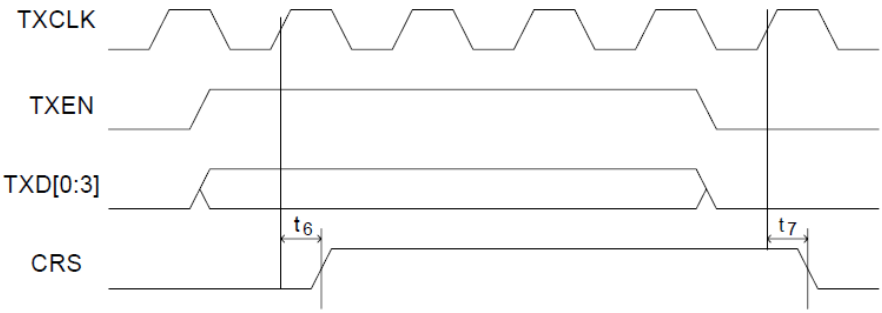


Figure 8-4. MII Transmission Cycle Timing-2

Table 11. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	5	-	-	ns
t_5	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0	-	-	ns
		10Mbps	0	-	-	ns
t_6	TXEN Sampled to CRS High	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t_7	TXEN Sampled to CRS Low	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns

8.2.2 MII Reception Cycle Timing

Figure9-5 and Figure9-6 show an example of a packet transfer from PHY to MAC on the MII interface.

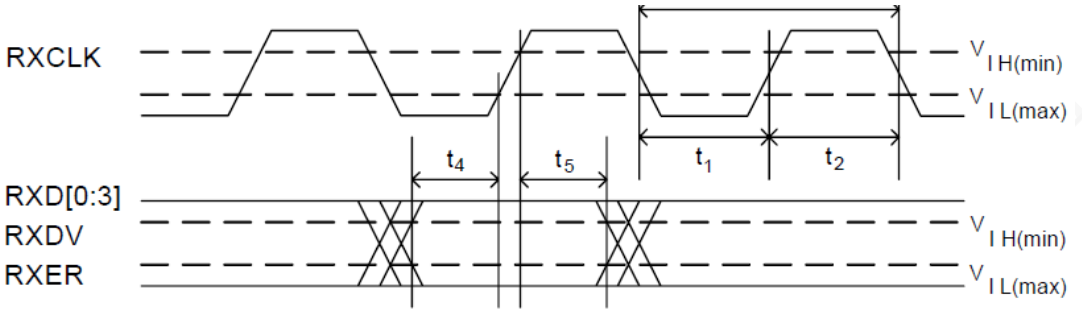


Figure 8-5. MII Reception Cycle Timing-1

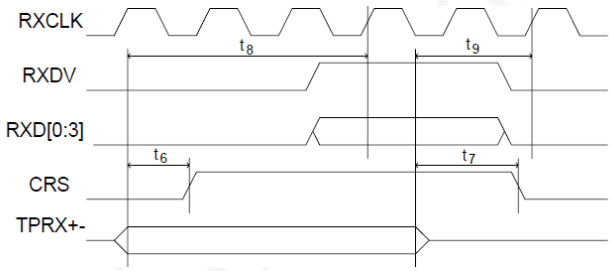


Figure 8-6. MII Reception Cycle Timing-2

Table 12. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	RXER, RXDV, RXD[0:3]	100Mbps	10	-	-	ns
	Setup to RXCLK Rising Edge	10Mbps	10	-	-	ns
t_5	RXER, RXDV, RXD[0:3]	100Mbps	10	-	-	ns

	Hold After RXCLK Rising Edge	10Mbps	10	-	-	ns
t_6	Receive Frame to CRS High	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t_7	End of Receive Frame to CRS Low	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t_8	Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t_9	End of Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

8.2.3 RMII Transmission and Reception Cycle Timing

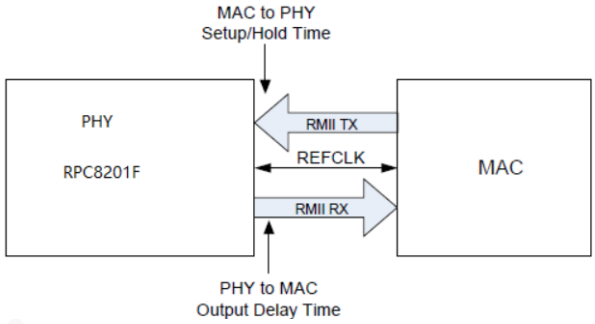


Figure 8-7. RMII Interface Setup, Hold Time, and Output Delay Time Definitions

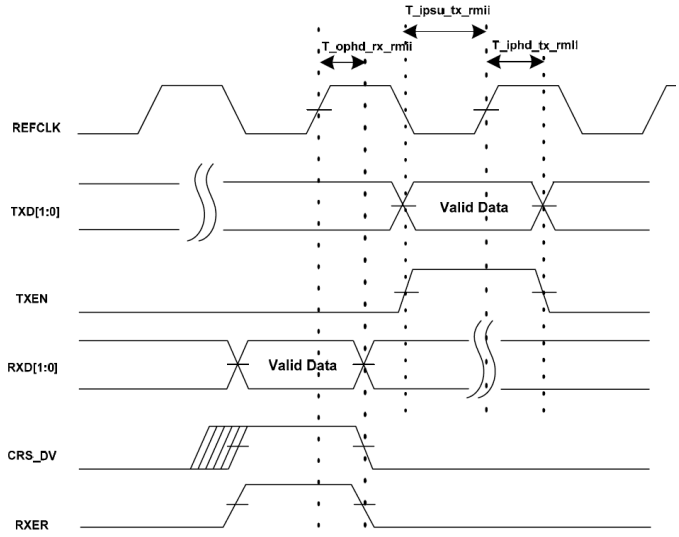


Figure 8-8. RMII Transmission and Reception Cycle Timing

Table 13. RMII Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	2	-	-	ns

8.2.4 MDC/MDIO Timing

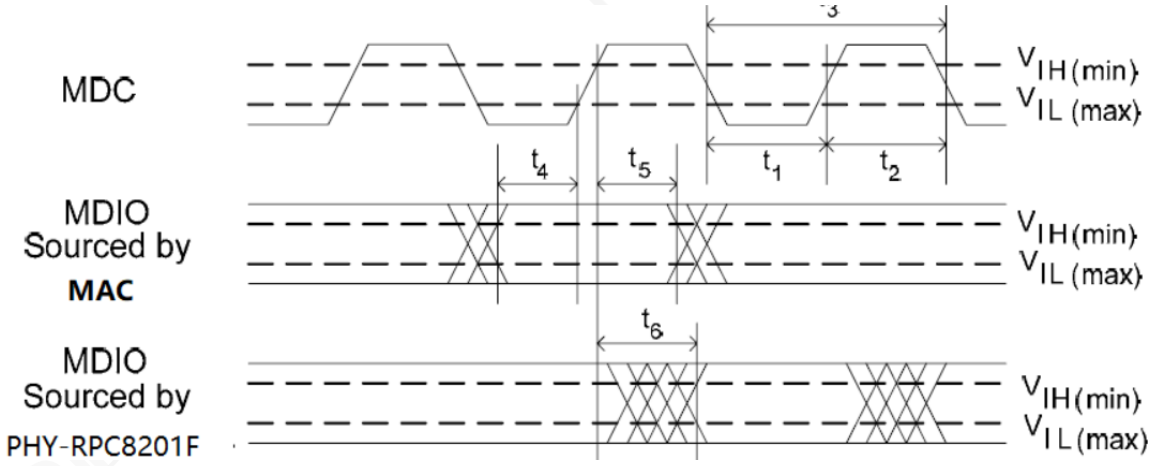


Figure 8-9. MDC/MDIO Timing

Table 14. MDC/MDIO Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC High Pulse Width	160	-	ns
t_2	MDC Low Pulse Width	160	-	ns
t_3	MDC Period	400	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

8.3 Crystal Characteristics

Table 15. Crystal Characteristics

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
DL	Drive Level.	-	-	0.3	mW
Jitter	Broadband Peak-to-Peak Jitter[1, 2]	-	-	500	ps

Note 1: 25KHz to 25MHz RMS < 3ps.

Note 2: Broadband RMS < 9ps.

8.4 Oscillator Requirements

Table 16. Oscillator Requirements

arameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25 or 50 [3]	-	MHz
Frequency Stability	Ta = 0°C~+70°C	-30	-	30	ppm
Frequency Tolerance	Ta = 25°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[1, 2]	-	-	-	500	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	0	-	70	°C

Note 1: 25KHz to 25MHz RMS < 3ps.

Note 2: Broadband RMS < 9ps.

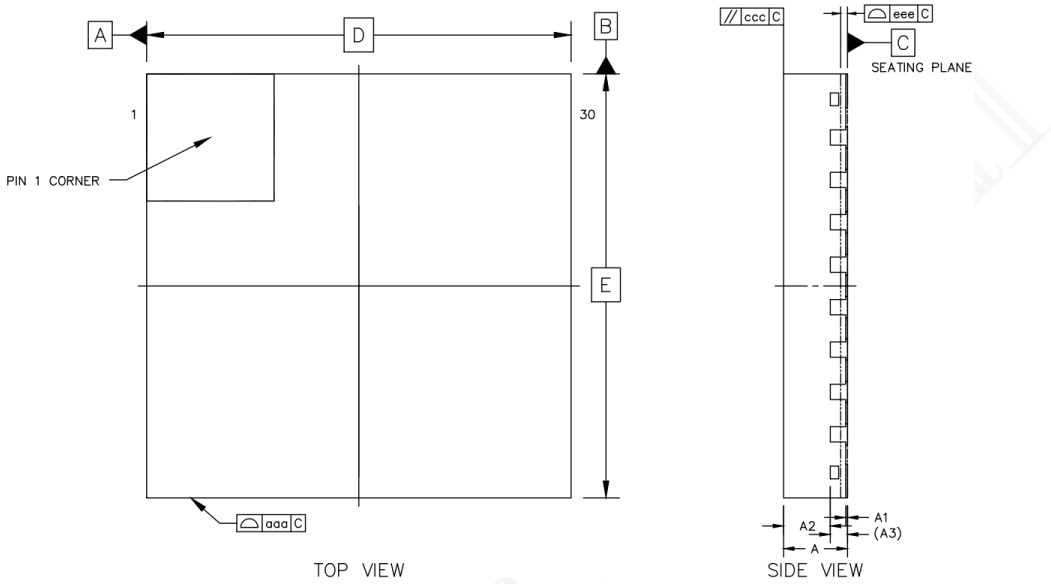
Note3: For Clock setting, please refer to" APPNOTE0001-RPC8201F"

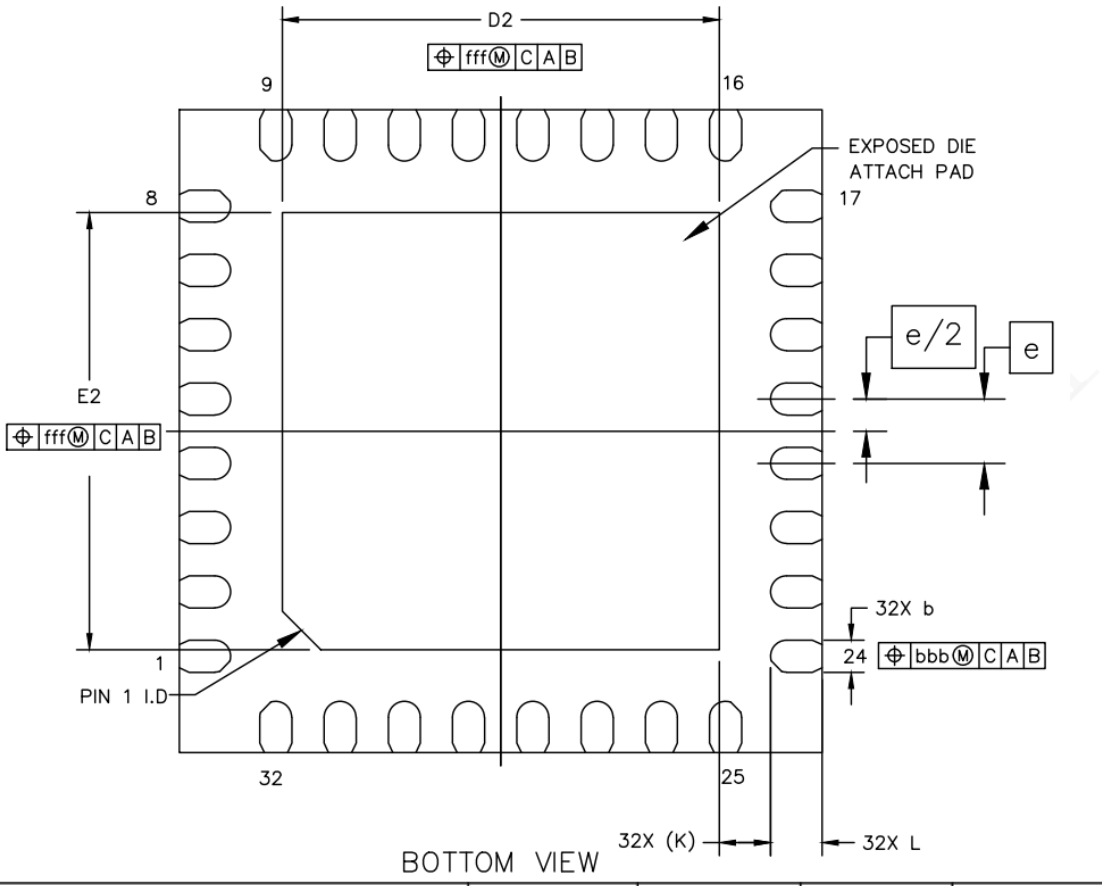
8.5 ESD Ratings

Table 17. ESD Ratings

Mode	Reference	Voltage	Unit	Note
HBM	ESDA/JEDEC JS-001-2017	±8	KV	MDI PINs
		±4	KV	
CDM	ESDA/JEDEC JS-002-2018	±1	KV	

9 Mechanical Dimensions





BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

10 Ordering Information

PN	PKG	Operation temp (℃)	Status
RPC8201F	QFN 32 5x5mm	0 to 70 ℃	Mass Production
RPC8201FI	QFN 32 5x5mm	-40 to 85 ℃	Mass Production