

N-Channel Enhancement Mode Field Effect Transistor

RCP0112

Product Summary

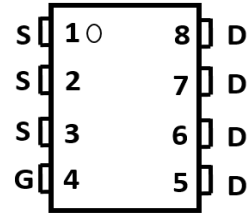
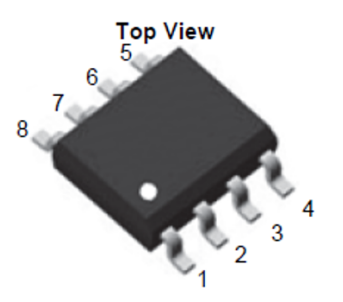
- V_{DS} 100V
- I_D 12A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 17 mohm

General Description

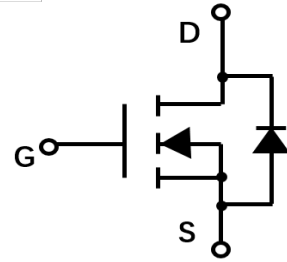
- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC/DC Primary Side Switch
- Telecom/Server
- Synchronous Rectification



SOP-8



■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	12	A
	$T_A=100^\circ\text{C}$		7.5	
Pulsed Drain Current ^A		I_{DM}	70	A
Avalanche Energy, Single Pulse(L=0.5mH)		E_{AS}	80	mJ
Total Power Dissipation ^B		P_D	3.1	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^C	$t \leq 10S$	$R_{\theta JA}$	31	40	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient ^C	Steady-State		59	75	
Thermal Resistance Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
RCP0112	F2		3000	9000	90000	13" reel

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■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _J =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.7	3.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A		14.5	17	mΩ
Diode Forward Voltage	V _{SD}	I _S =12A, V _{GS} =0V			1.3	V
Maximum Body-Diode Continuous Current	I _S				12	A
Gate resistance	R _G	f=1MHz, Open drain		1		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		1135		pF
Output Capacitance	C _{oss}			399		
Reverse Transfer Capacitance	C _{rss}			18		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =10A		16		nC
Gate-Source Charge	Q _{gs}			5.6		
Gate-Drain Charge	Q _{gd}			2.4		
Reverse Recovery Charge	Q _{rr}	I _F =10A, di/dt=100A/us		42		ns
Reverse Recovery Time	t _{rr}			39.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =10A R _{GEN} =2.2Ω		39.2		ns
Turn-on Rise Time	t _r			11		
Turn-off Delay Time	t _{D(off)}			53.2		
Turn-off fall Time	t _f			15.8		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. Pd is based on max. junction temperature, using ≤10s junction-ambient thermal resistance.

C. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

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■ Typical Performance Characteristics

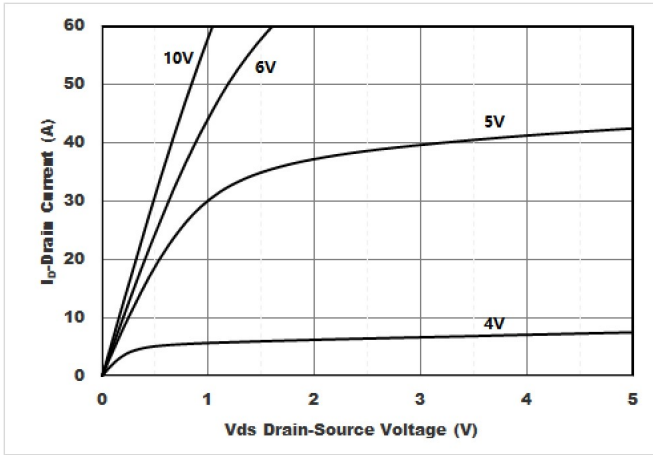


Figure1. Output Characteristics

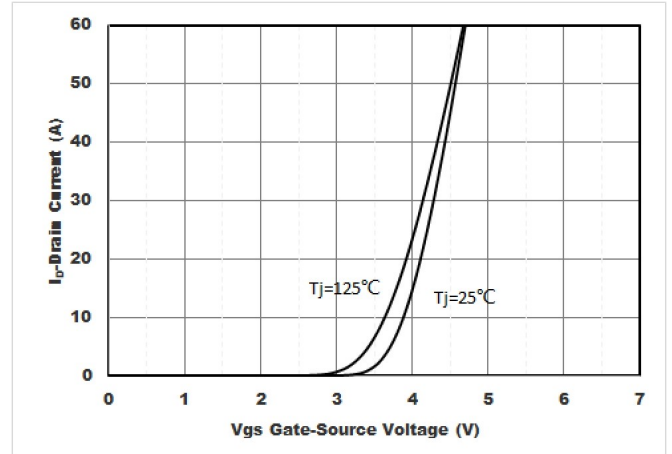


Figure2. Transfer Characteristics

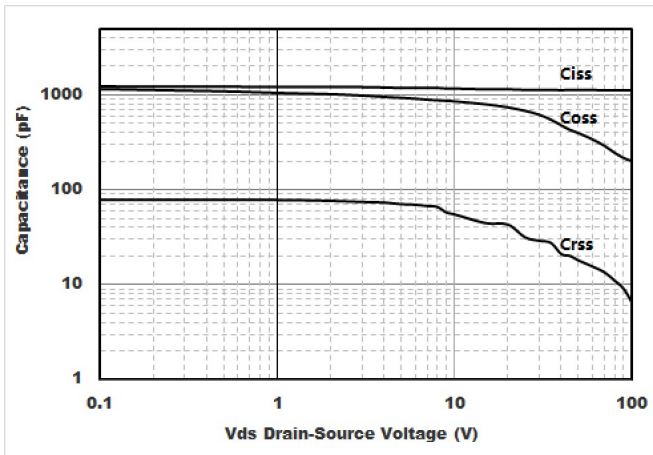


Figure3. Capacitance Characteristics

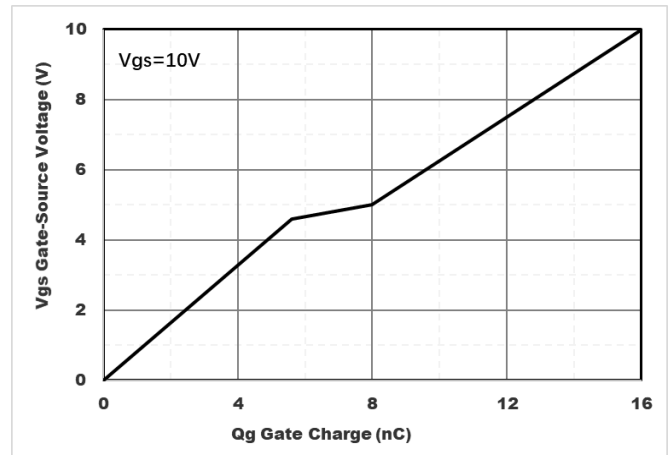


Figure4. Gate Charge

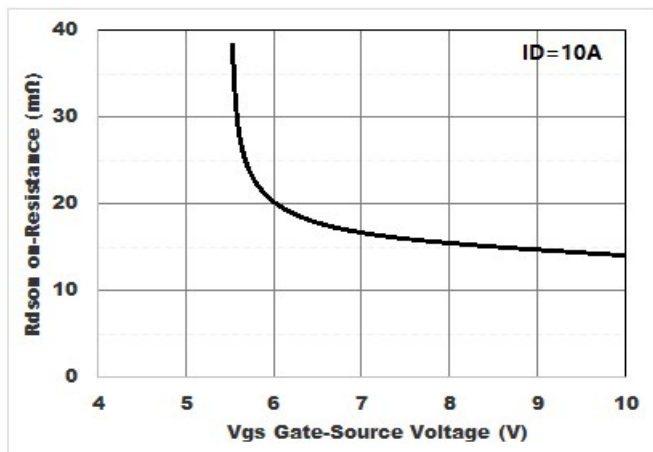


Figure5. Drain-Source on Resistance

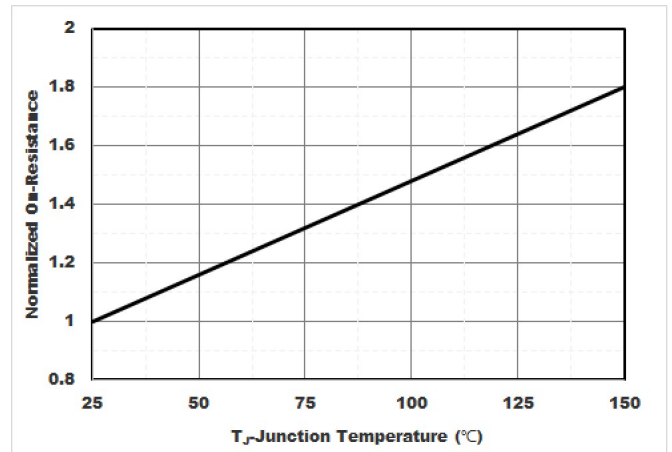


Figure6. Drain Current

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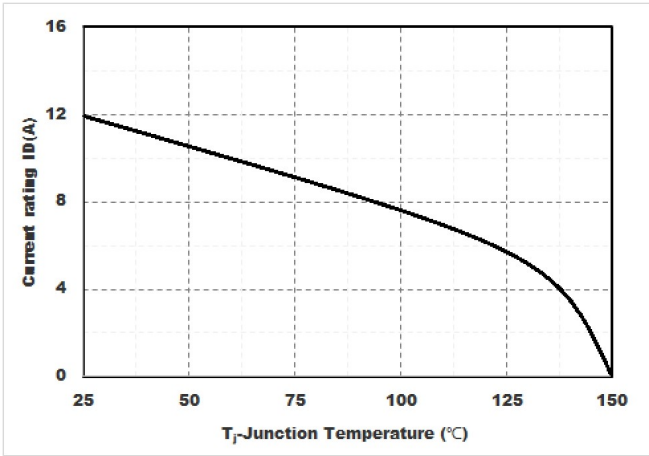


Figure7. Drain current

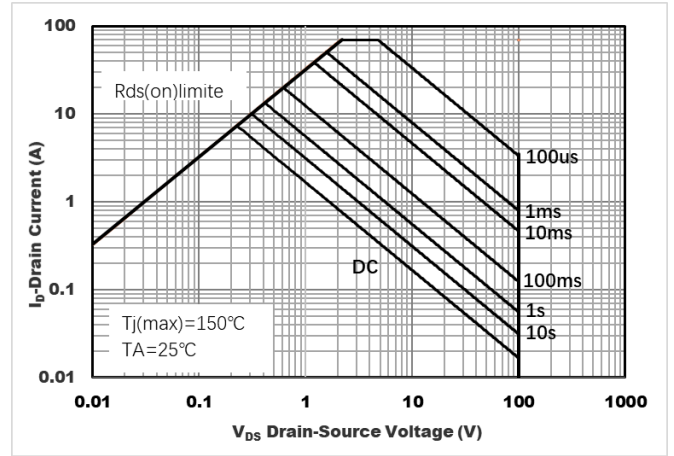


Figure8. Safe Operation Area

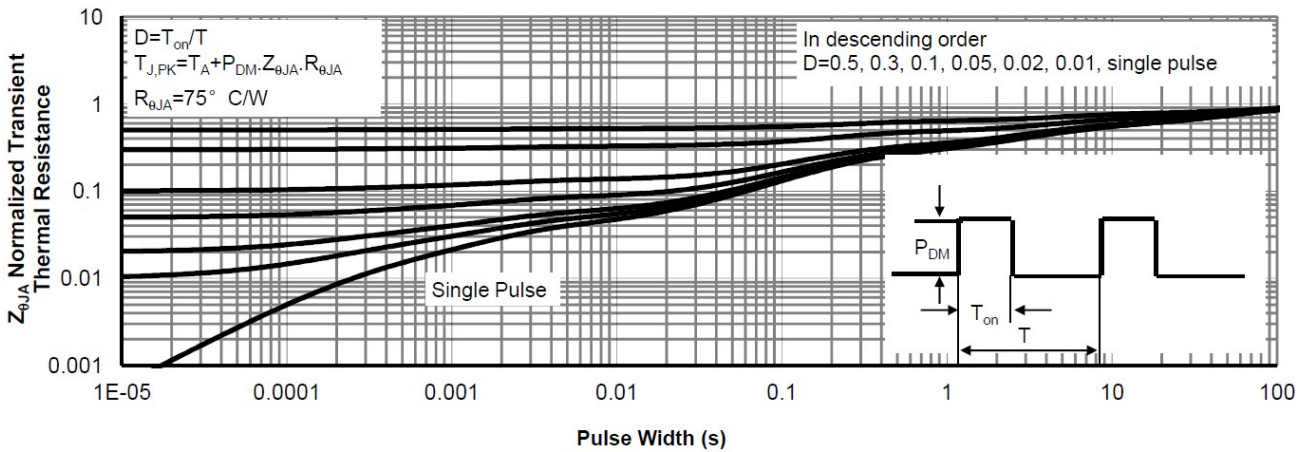
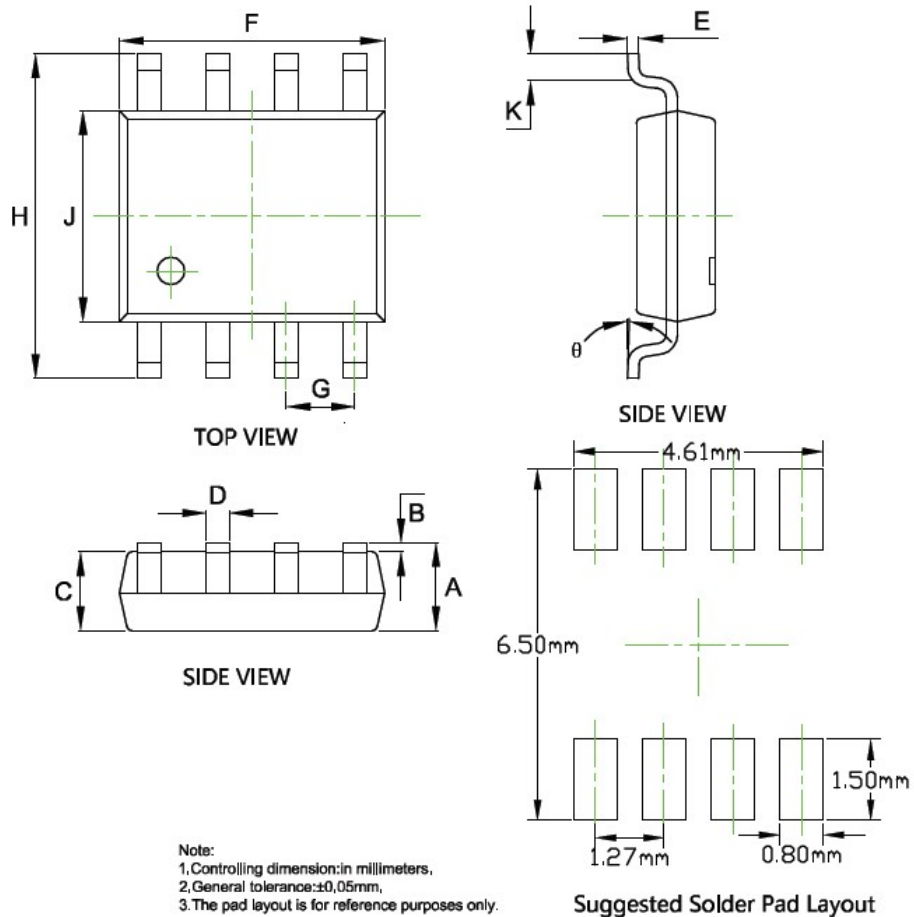


Figure9. Normalized Maximum Transient Thermal Impedance

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■ SOP-8 Package information



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°