DDR4 SDRAM

RS256M16ZADD-75DT– 32 Meg x 16 x 8 Banks

RS512M8ZADD-75DT– 64 Meg x 8 x 8 Banks

Features

- $V_{DD} = V_{DDQ}$ = 1.2V ±60mV
- V_{PP} = 2.5V, –125mV/+250mV
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- TC of 0°C to 95°C
  - 64ms, 8192-cycle refresh at 0°C to 85°C
  - 32ms at 85°C to 95°C
- TC of 0°C to 95°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test (x16)
- Post package repair (PPR) and soft post package repair (sPPR) modes
- JEDEC JESD-79-4 compliant

Options

- RaysonMemory

- Configuration
  - 1 Gig x 4
  - 512 Meg x 8
  - 256 Meg x 16
- Product Code
  - DDR4
- Density
  - 4 Gigabyte
- Voltage/Refresh
  - 1.5V/8k refresh
- FBGA package (Pb-free) - x4, x8
  - 78-ball (7.5mm x 11mm)
  - 78-ball (8mm x 12mm)
  - 78-ball (9mm x 10.5mm)
  - 78-ball (9mm x 11.5mm)
  - 78-ball (9mm x 13.2mm)
- FBGA package (Pb-free) - x16
  - 96-ball (9mm x 14mm), rev A
  - 96-ball (9mm x 14mm), rev B
  - 96-ball (7.5mm x 13.5mm) – rev E, F
- Timing - cycle time
  - 0.750ns @ CL = 18 (DDR4-2666)
  - 0.833ns @ CL = 16 (DDR4-2400)
  - 0.833ns @ CL = 17 (DDR4-2400)
  - 0.937ns @ CL = 15 (DDR4-2133)
  - 0.937ns @ CL = 16 (DDR4-2133)
  - 0.937ns @ CL = 16 (DDR4-2133)
  - 0.937ns @ CL = 16 (DDR4-2133)
- Operating temperature
  - Commercial (0° ≤ T_C ≤ 95°C)

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^tRCD-^tRP-CL	^tRCD (ns)	^tRP (ns)	CL (ns)
-075E[1, 2, 3, 4]	2666	18-18-18	13.5	13.5	13.5
-083E[1, 2, 3, 4]	2400	16-16-16	13.32	13.32	13.32
-083[1, 2, 3, 4]	2400	17-17-17	14.16	14.16	14.16
-093F[1, 2, 3]	2133	14-14-14	13.13	13.13	13.13
-093E[1, 2]	2133	15-15-15	14.06	14.06	14.06
-093[1, 2]	2133	16-16-16	15	15	15
-107E[1]	1866	13-13-13	13.92	13.92	13.92

Notes: 1. Backward compatible to 1600, CL = 11 (-125E).
2. Backward compatible to 1866, CL = 13 (-107E).
3. Backward compatible to 2133, CL = 15 (-2133).
4. Backward compatible to 2133, CL = 14 (-2133).

Table 2: Addressing

Parameter	1 Gig × 4	512 Meg × 8	256 Meg × 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	64K (A[15:0])	32K (A[15:0])	32K (A[14:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size[1]	512B / 1KB[2]	1KB	2KB

Notes: 1. Page size is per bank, calculated as follows:
Page size = $2^{COLBITS}$ x ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.
2. Die revision dependent.

Ordering Information

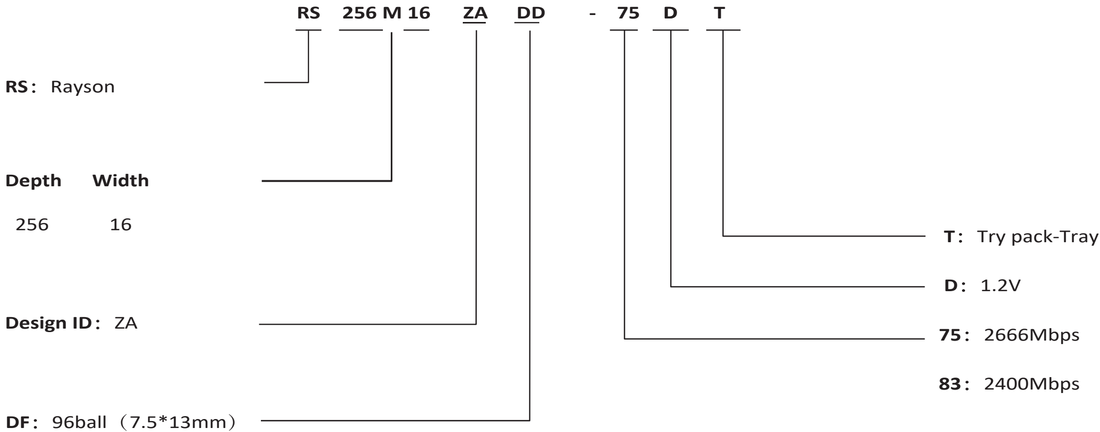


Table of Contents

Features . . . 1
General Notes and Description . . . 14
Description . . . 14
General Notes . . . 14
Definitions of the Device-Pin Signal Level . . . 15
Definitions of the Bus Signal Level . . . 15
Ball Assignments . . . 16
Ball Descriptions . . . 18
Package Dimensions . . . 21
State Diagram . . . 23
Functional Description . . . 25
RESET and Initialization Procedure . . . 26
- Power-Up and Initialization Sequence . . . 26
- RESET Initialization with Stable Power Sequence . . . 29
- Uncontrolled Power-Down Sequence . . . 30

Programming Mode Registers . . . 30
Mode Register 0 . . . 33
- Burst, Length, Type, and Order . . . 34
- CAS Latency . . . 35
- Test Mode . . . 35
- Write Recovery(WR)/READ-to-PRECHARGE . . . 36
- DLL RESET . . . 36

Mode Register 1 . . . 37
- DLL Enable/DLL Disable . . . 38
- Output Driver Impedance Control . . . 38
- ODT R TT(NOM) Values . . . 39
- Additive Latency . . . 39
- Write Leveling . . . 39
- Output Disable . . . 39
- Termination Data Strobe . . . 39

Mode Register 2 . . . 41
- CAS WRITE Latency . . . 42
- Low-Power Auto Self Refresh . . . 42
- Dynamic ODT . . . 43
- Write Cyclic Redundancy Check Data Bus . . . 43
- Target Row Refresh Mode . . . 43

Mode Register 3 . . . 44
- Multipurpose Register . . . 45
- WRITE Command Latency When CRC/DM is Enabled . . . 45
- Fine Granularity Refresh Mode . . . 46
- Temperature Sensor Status . . . 46
- Per-DRAM Addressability . . . 46
- Gear-Down Mode . . . 46

Mode Register 4 . . . 47
- Post Package Repair Mode . . . 48
- Soft Post Package Repair Mode . . . 48
- WRITE Preamble . . . 48
- READ Preamble . . . 49
- READ Preamble Training . . . 49
- Temperature-Controlled Refresh . . . 49
- Command Address Latency . . . 49

Internal V_{REF} Monitor . . . 49
Maximum Power Savings Mode . . . 49
Mode Register 5 . . . 50
Data Bus Inversion . . . 51
Data Mask . . . 51
CA Parity Persistent Error Mode . . . 52
ODT Input Buffer for Power-Down . . . 52
CA Parity Error Status . . . 52
CRC Error Status . . . 52
CA Parity Latency Mode . . . 52
Mode Register 6 . . . 53
^{t}CCD_L Programming . . . 54
V_{REFDQ} Calibration Enable . . . 54
V_{REFDQ} Calibration Range . . . 54
V REFDQ Calibration Value . . . 54
Truth Tables . . . 55
NOP Command . . . 58
DESELECT Command . . . 58
DLL-Off Mode . . . 58
DLL-On/Off Switching Procedures . . . 60
DLL Switch Sequence from DLL-On to DLL-Off . . . 60
DLL-Off to DLL-On Procedure . . . 61
Input Clock Frequency Change . . . 62
Write Leveling . . . 64
DRAM Setting for Write Leveling and DRAM TERMINATION Function in that Mode . . . 65
Procedure Description . . . 66
Write-Leveling Mode Exit . . . 67
Command Address Latency . . . 69
Low-Power Auto Self Refresh Mode . . . 73
Manual Self Refresh Mode . . . 73
Multipurpose Register . . . 75
MPR Reads . . . 76
MPR Readout Format . . . 78
MPR Readout Serial Format . . . 78
MPR Readout Parallel Format . . . 79
MPR Readout Staggered Format . . . 80
MPR READ Waveforms . . . 81
MPR Writes . . . 83
MPR WRITE Waveforms . . . 83
MPR REFRESH Waveforms . . . 85
Gear-Down Mode . . . 87
Maximum Power-Saving Mode . . . 90
Maximum Power-Saving Mode Entry . . . 90
Maximum Power-Saving Mode Entry in PDA . . . 91
CKE Transition During Maximum Power-Saving Mode . . . 91
Maximum Power-Saving Mode Exit . . . 92
Command/Address Parity . . . 93
Per-DRAM Addressability . . . 101
V_{REFDQ} Calibration . . . 103
V_{REFDQ} Range and Levels . . . 104
V_{REFDQ} Step Size . . . 104
V_{REFDQ} Increment and Decrement Timing . . . 105
V_{REFDQ} Target Settings . . . 109

Connectivity Test Mode . . . 110
Pin Mapping . . . 110
Minimum Terms Definition for Logic Equations . . . 111
Logic Equations for a x4 Device, When Supported . . . 111
Logic Equations for a x8 Device, When Supported . . . 111
Logic Equations for a x16 Device . . . 112
CT Input Timing Requirements . . . 112
Post Package Repair and Soft Post Package Repair . . . 114
Post Package Repair . . . 114
PPR Row Repair . . . 114
PPR Row Repair - Entry . . . 114
PR Row Repair – WRA Initiated (REF Commands Allowed) . . . 115
PPR Row Repair – WR Initiated (REF Commands NOT Allowed) . . . 116
sPPR Row Repair . . . 118
PPR/sPPR Support Identifier . . . 119
Target Row Refresh Mode . . . 120
ACTIVATE command . . . 121
PRECHARGE Command . . . 122
REFRESH Command . . . 122
Temperature-Controlled Refresh Mode . . . 124
TCR Mode – Normal Temperature Range . . . 124
TCR Mode – Extended Temperature Range . . . 124
Fine Granularity Refresh Mode . . . 126
Mode Register and Command Truth Table . . . 126
^{t}REFI and ^{t}RFC Parameters . . . 126
Changing Refresh Rate . . . 129
Usage with TCR Mode . . . 129
Self Refresh Entry and Exit . . . 129
SELF REFRESH Operation . . . 131
Self Refresh Abort . . . 133
Self Refresh Exit with NOP Command . . . 134
Power-Down Mode . . . 136
Power-Down Clarifications – Case 1 . . . 141
Power-Down Entry, Exit Timing with CAL . . . 142
ODT Input Buffer Disable Mode for Power-Down . . . 145
CRC Write Data Feature . . . 147
CRC Write Data . . . 147
WRITE CRC DATA Operation . . . 147
DBI_n and CRC Both Enabled . . . 148
DM_n and CRC Both Enabled . . . 148
DM_n and DBI_n Conflict During Writes with CRC Enabled . . . 148
CRC and Write Preamble Restrictions . . . 148
CRC Simultaneous Operation Restrictions . . . 148
CRC Polynomial . . . 148
CRC Combinatorial Logic Equations . . . 149
Burst Ordering for BL8 . . . 150
CRC Data Bit Mapping . . . 150
CRC Enabled With BC4 . . . 151
CRC with BC4 Data Bit Mapping . . . 151
CRC Equations for x8 Device in BC4 Mode with A2 = 0 and A2 = 1 . . . 153
CRC Error Handling . . . 155
CRC Write Data Flow Diagram . . . 156
Data Bus Inversion . . . 157

DBI During a WRITE Operation 157
DBI During a READ Operation 158
Data Mask 159
Programmable Preamble Modes and DQS Postambles 160
WRITE Preamble Mode 160
READ Preamble Mode 163
READ Preamble Training 163
WRITE Postamble 164
READ Postamble 164
Bank Access Operation 166
READ Operation 170
Read Timing Definitions 170
Read Timing – Clock-to-Data Strobe Relationship 171
Read Timing – Data Strobe-to-Data Relationship 172
^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) Calculations 173
^{t}RPRE Calculation 175
^{t}RPST Calculation 176
READ Burst Operation 177
READ Operation Followed by Another READ Operation 179
READ Operation Followed by WRITE Operation 184
READ Operation Followed by PRECHARGE Operation 190
READ Operation with Read Data Bus Inversion (DBI) 193
READ Operation with Command/Address Parity (CA Parity) 194
READ Followed by WRITE with CRC Enabled 195
READ Operation with Command/Address Latency (CAL) Enabled 196
WRITE Operation 198
Write Timing Definitions 198
Write Timing – Clock-to-Data Strobe Relationship 198
Write Timing – Data Strobe-to-Data Relationship 199
WRITE Burst Operation 203
WRITE Operation Followed by Another WRITE Operation 205
WRITE Operation Followed by READ Operation 210
WRITE Operation Followed by PRECHARGE Operation 213
WRITE Operation with WRITE DBI Enabled 216
WRITE Operation with CA Parity Enabled 217
WRITE Operation with Write CRC Enabled 218
Write Timing Violations 222
Motivation 222
Data Setup and Hold Violations 222
Strobe-to-Strobe and Strobe-to-Clock Violations 222
ZQ CALIBRATION Commands 223
On-Die Termination 225
ODT Mode Register and ODT State Table 225
ODT Read Disable State Table 226
Synchronous ODT Mode 227
ODT Latency and Posted ODT 227
Timing Parameters 227
ODT During Reads 229
Dynamic ODT 230
Functional Description 230
Asynchronous ODT Mode 233
Electrical Specifications 234
Absolute Ratings 234

DRAM Component Operating Temperature Range 234
Electrical Characteristics – AC and DC Operating Conditions 235
Supply Operating Conditions 235
Leakages 235
V_{REFCA} Supply 236
V_{REFDQ} Supply and Calibration Ranges. 236
V_{REFDQ} Ranges 237

List of Figures

Figure 1: 78-Ball – x4, x8 Ball Assignments . . . 16
Figure 2: 96-Ball FBGA – x16 Ball Assignments . . . 17
Figure 3: 78-Ball FBGA – x4, x8; "RAF" . . . 21
Figure 4: 96-Ball FBGA – x16; "REF". . . 22
Figure 5: Simplified State Diagram . . . 23
Figure 6: RESET and initialization Sequence at Power-On Ramping . . . 28
Figure 7: RESET Procedure at Power Stable Ramping . . . 29
Figure 8: ^{t}MRD Timing . . . 31
Figure 9: ^{t}MOD Timing . . . 31
Figure 10: DLL-Off Mode Read Timing Operation . . . 59
Figure 11: DLL Switch Sequence from DLL-On to DLL-Off . . . 61
Figure 12: DLL Switch Sequence from DLL-Off to DLL-On . . . 62
Figure 13: Write-Leveling Concept, Example 1 . . . 64
Figure 14: Write-Leveling Concept, Example 2 . . . 65
Figure 15: Write-Leveling Sequence (DQS Capturing CK LOW at T1 and CK HIGH at T2) . . . 67
Figure 16: Write-Leveling Exit . . . 68
Figure 17: CAL Timing Definition. . . 69
Figure 18: CAL Timing Example (Consecutive CS_n = LOW) . . . 69
Figure 19: CAL Enable Timing – ^{t}MOD_CAL . . . 70
Figure 20: ^{t}MOD_CAL, MRS to Valid Command Timing with CAL Enabled. . . 70
Figure 21: CAL Enabling MRS to Next MRS Command, ^{t}MRD_CAL. . . 71
Figure 22: ^{t}MRD_CAL, Mode Register Cycle Time with CAL Enabled . . . 71
Figure 23: Consecutive READ BL8, CAL3, 1^{t}CK Preamable, Different Bank Group. . . 72
Figure 24: Consecutive READ BL8, CAL4, 1^{t}CK Preamable, Different Bank Group. . . 72
Figure 25: Auto Self Refresh Ranges. . . 74
Figure 26: MPR Block Diagram . . . 75
Figure 27: MPR READ Timing . . . 81
Figure 28: MPR Back-to-Back READ Timing . . . 82
Figure 29: MPR READ-to-WRITE Timing . . . 82
Figure 30: MPR WRITE and WRITE-to-READ Timing . . . 84
Figure 31: MPR Bank-to-Back WRITE Timing . . . 84
Figure 32: REFRESH Timing . . . 85
Figure 33: READ-to-REFRESH Timing . . . 85
Figure 34: WRITE-to-REFRESH Timing . . . 86
Figure 35: Clock Mode Change from 1/2 Rate to 1/4 Rate (Initialization) . . . 88
Figure 36: Clock Mode Change After Exiting Self Refresh . . . 88
Figure 37: Comparison Between Gear-Down Disable and Gear-Down Enable . . . 89
Figure 38: Maximum Power-Saving Mode Entry . . . 90
Figure 39: Maximum Power-Saving Mode Entry with PDA . . . 91
Figure 40: Maintaining Maximum Power-Saving Mode with CKE Transition . . . 91
Figure 41: Maximum Power-Saving Mode Exit . . . 92
Figure 42: Command/Address Parity Operation . . . 93
Figure 43: Command/Address Parity During Normal Operation . . . 95
Figure 44: Persistent CA Parity Error Checking Operation . . . 96
Figure 45: CA Parity Error Checking – SRE Attempt . . . 96
Figure 46: CA Parity Error Checking – SRX Attempt . . . 97
Figure 47: CA Parity Error Checking – PDE/PDX . . . 97
Figure 48: Parity Entry Timing Example – ^{t}MRD_PAR . . . 98
Figure 49: Parity Entry Timing Example – ^{t}MOD_PAR . . . 98
Figure 50: Parity Exit Timing Example – ^{t}MRD_PAR . . . 98
Figure 51: Parity Exit Timing Example – ^{t}MOD_PAR . . . 99
Figure 52: CA Parity Flow Diagram . . . 100
Figure 53: PDA Operation Enabled, BL8 . . . 102
Figure 54: PDA Operation Enabled, BC4 . . . 102
Figure 55: MRS PDA Exit. . . 102
Figure 56: V_{REFDQ} Voltage Range . . . 103

Figure 57: Example of V_{REF} Set Tolerance and Step Size. 105
Figure 58: V_{REFDQ} Timing Diagram for $V_{REF,time}$ Parameter 106
Figure 59: V_{REFDQ} Training Mode Entry and Exit Timing Diagram 107
Figure 60: V_{REF} Step: Single Step Size Increment Case 107
Figure 61: V_{REF} Step: Single Step Size Decrement Case. 108
Figure 62: V_{REF} Full Step: From $V_{REF,min}$ to $V_{REF,max}$Case 108
Figure 63: V_{REF} Full Step: From $V_{REF,max}$ to $V_{REF,min}$Case 108
Figure 64: V_{REFDQ} Equivalent Circuit 109
Figure 65: Connectivity Test Mode Entry 113
Figure 66: PPR WRA – Entry. 116
Figure 67: PPR WRA – Repair and Exit. 116
Figure 68: PPR WR – Entry 117
Figure 69: PPR WR – Repair and Exit 117
Figure 70: sPPR – Entry, Repair, and Exit 119
Figure 71: ^{t}RRD Timing. 121
Figure 72: ^{t}FAW Timing 121
Figure 73: REFRESH Command Timing 123
Figure 74: Postponing REFRESH Commands (Example) 123
Figure 75: Pulling In REFRESH Commands (Example) 123
Figure 76: TCR Mode Example[1] 125
Figure 77: 4Gb with Fine Granularity Refresh Mode Example. 128
Figure 78: OFT REFRESH Command Timing 129
Figure 79: Self Refresh Entry/Exit Timing. 132
Figure 80: Self Refresh Entry/Exit Timing with CAL Mode 133
Figure 81: Self Refresh Abort 134
Figure 82: Self Refresh Exit with NOP Command 135
Figure 83: Active Power-Down Entry and Exit. 137
Figure 84: Power-Down Entry After Read and Read with Auto Precharge 138
Figure 85: Power-Down Entry After Write and Write with Auto Precharge. 138
Figure 86: Power-Down Entry After Write 139
Figure 87: Precharge Power-Down Entry and Exit 139
Figure 88: REFRESH Command to Power-Down Entry. 140
Figure 89: Active Command to Power-Down Entry 140
Figure 90: PRECHARGE/PRECHARGE ALL Command to Power-Down Entry 141
Figure 91: MRS Command to Power-Down Entry 141
Figure 92: Power-Down Entry/Exit Clarifications – Case 1. 142
Figure 93: Active Power-Down Entry and Exit Timing with CAL. 143
Figure 94: REFRESH Command to Power-Down Entry with CAL. 144
Figure 95: ODT Power-Down Entry with ODT Buffer Disable Mode 145
Figure 96: ODT Power-Down Exit with ODT Buffer Disable Mode. 146
Figure 97: CRC Write Data Operation 147
Figure 98: CRC Error Reporting 155
Figure 99: ^{t}CK vs. 2^{t}CK WRITE Preamble Mode 160
Figure 100:^{t}CK vs. 2^{t}CK WRITE Preamble Mode, ^{t}CCD = 4 161
Figure 101:1^{t}CK vs. 2^{t}CK WRITE Preamble Mode, ^{t}CCD = 5 162
Figure 102:1^{t}CK vs. 2^{t}CK WRITE Preamble Mode, ^{t}CCD = 6 162
Figure 103:1^{t}CK vs. 2^{t}CK READ Preamble Mode 163
Figure 104:READ Preamble Training 164
Figure 105:WRITE Postamble 164
Figure 106:READ Postamble 165
Figure 107:Bank Group x4/x8 Block Diagram 166
Figure 108:READ Burst ^{t}CCD_S and ^{t}CCD_L Examples. 167
Figure 109:Write Burst ^{t}CCD_S and ^{t}CCD_L Examples 168
Figure 110:^{t}RRD Timing 168
Figure 111:^{t}WTR_S Timing (WRITE-to-READ, Different Bank Group, CRC and DM Disabled) 169
Figure 112:^{t}WTR_L Timing (WRITE-to-READ, Same Bank Group, CRC and DM Disabled) 169
Figure 113:Read Timing Definition 171

Figure 114:Clock-to-Data Strobe Relationship . . . 172
Figure 115:Data Strobe-to-Data Relationship . . . 173
Figure 116:^{t}LZ and ^{t}HZ Method for Calculating Transitions and Endpoints . . . 174
Figure 117:^{t}RPRE Method for Calculating Transitions and Endpoints. . . 175
Figure 118:^{t}RPST Method for Calculating Transitions and Endpoints . . . 176
Figure 119:READ Burst Operation, RL = 11 (AL = 0, CL = 11, BL8) . . . 177
Figure 120:READ Burst Operation, RL = 21 (AL = 10, CL = 11, BL8). . . 178
Figure 121:Consecutive READ (BL8) with 1^{t}CK Preamble in Different Bank Group . . . 179
Figure 122:Consecutive READ (BL8) with 2^{t}CK Preamble in Different Bank Group . . . 179
Figure 123:Nonconsecutive READ (BL8) with 1^{t}CK Preamble in Same or Different Bank Group . . . 180
Figure 124:Nonconsecutive READ (BL8) with 2^{t}CK Preamble in Same or Different Bank Group . . . 180
Figure 125:READ (BC4) to READ (BC4) with 1^{t}CK Preamble in Different Bank Group. . . 181
Figure 126:READ (BC4) to READ (BC4) with 2^{t}CK Preamble in Different Bank Group. . . 181
Figure 127:READ (BL8) to READ (BC4) OTF with 1^{t}CK Preamble in Different Bank Group . . . 182
Figure 128:READ (BL8) to READ (BC4) OTF with 2^{t}CK Preamble in Different Bank Group . . . 182
Figure 129:READ (BC4) to READ (BL8) OTF with 1^{t}CK Preamble in Different Bank Group . . . 183
Figure 130:READ (BC4) to READ (BL8) OTF with 2^{t}CK Preamble in Different Bank Group . . . 183
Figure 131:READ (BL8) to WRITE (BL8) with 1^{t}CK Preamble in Same or Different Bank Group . . . 184
Figure 132:READ (BL8) to WRITE (BL8) with 2^{t}CK Preamble in Same or Different Bank Group . . . 184
Figure 133:READ (BC4) OTF to WRITE (BC4) OTF with 1^{t}CK Preamble in Same or Different Bank Group. . . 185
Figure 134:READ (BC4) OTF to WRITE (BC4) OTF with 2^{t}CK Preamble in Same or Different Bank Group. . . 186
Figure 135:READ (BC4) Fixed to WRITE (BC4) Fixed with 1^{t}CK Preamble in Same or Different Bank Group. . 186
Figure 136:READ (BC4) Fixed to WRITE (BC4) Fixed with 2^{t}CK Preamble in Same or Different Bank Group. . 187
Figure 137:READ (BC4) to WRITE (BL8) OTF with 1^{t}CK Preamble in Same or Different Bank Group . . . 187
Figure 138:READ (BC4) to WRITE (BL8) OTF with 2^{t}CK Preamble in Same or Different Bank Group . . . 188
Figure 139:READ (BL8) to WRITE (BC4) OTF with 1^{t}CK Preamble in Same or Different Bank Group . . . 189
Figure 140:READ (BL8) to WRITE (BC4) OTF with 2^{t}CK Preamble in Same or Different Bank Group . . . 189
Figure 141:READ to PRECHARGE with 1^{t}CK Preamble . . . 190
Figure 142:READ to PRECHARGE with 2^{t}CK Preamble . . . 191
Figure 143:READ to PRECHARGE with Additive Latency and 1^{t}CK Preamble . . . 191
Figure 144:READ with Auto Precharge and 1^{t}CK Preamble . . . 192
Figure 145:READ with Auto Precharge, Additive Latency, and 1^{t}CK Preamble . . . 192
Figure 146:Consecutive READ (BL8) with 1^{t}CK Preamble and DBI in Different Bank Group . . . 193
Figure 147:Consecutive READ (BL8) with 1^{t}CK Preamble and CA Parity in Different Bank Group . . . 194
Figure 148:READ (BL8) to WRITE (BL8) with 1^{t}CK Preamble and CA Parity in Same or Different Bank Group 194
Figure 149:READ (BL8) to WRITE (BL8 or BC4: OTF) with 1^{t}CK Preamble and Write CRC in Same or Different Bank Group . . . 195
Figure 150:READ (BC4: Fixed) to WRITE (BC4: Fixed) with 1^{t}CK Preamble and Write CRC in Same or Different Bank Group . . . 196
Figure 151:Consecutive READ (BL8) with CAL (3^{t}CK) and 1^{t}CK Preamble in Different Bank Group . . . 196
Figure 152:Consecutive READ (BL8) with CAL (4^{t}CK) and 1^{t}CK Preamble in Different Bank Group . . . 197
Figure 153:Write Timing Definition . . . 199
Figure 154:Rx Compliance Mask. . . 200
Figure 155:V_{CENT_DQ} V_{REFDQ} Voltage Variation . . . 200
Figure 156:Rx Mask DQ-to-DQS Timings . . . 201
Figure 157:Rx Mask DQ-to-DQS DRAM-Based Timings . . . 202
Figure 158:Example of Data Input Requirements Without Training . . . 203
Figure 159:WRITE Burst Operation, WL = 9 (AL = 0, CWL = 9, BL8) . . . 204
Figure 160:WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8) . . . 204
Figure 161:Consecutive WRITE (BL8) with 1^{t}CK Preamble in Different Bank Group . . . 205
Figure 162:Consecutive WRITE (BL8) with 2^{t}CK Preamble in Different Bank Group . . . 205
Figure 163:Nonconsecutive WRITE (BL8) with 1^{t}CK Preamble in Same or Different Bank Group . . . 206
Figure 164:Nonconsecutive WRITE (BL8) with 2^{t}CK Preamble in Same or Different Bank Group . . . 207
Figure 165:WRITE (BC4) OTF to WRITE (BC4) OTF with 1^{t}CK Preamble in Different Bank Group. . . 207
Figure 166:WRITE (BC4) OTF to WRITE (BC4) OTF with 2^{t}CK Preamble in Different Bank Group. . . 208
Figure 167:WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1^{t}CK Preamble in Different Bank Group. . . 209
Figure 168:WRITE (BL8) to WRITE (BC4) OTF with 1^{t}CK Preamble in Different Bank Group . . . 209

Figure 169:WRITE (BC4) OTF to WRITE (BL8) with 1^{t}CK Preamble in Different Bank Group 210
Figure 170:WRITE (BL8) to READ (BL8) with 1^{t}CK Preamble in Different Bank Group 210
Figure 171:WRITE (BL8) to READ (BL8) with 1^{t}CK Preamble in Same Bank Group 211
Figure 172:WRITE (BC4) OTF to READ (BC4) OTF with 1^{t}CK Preamble in Different Bank Group. 211
Figure 173:WRITE (BC4) OTF to READ (BC4) OTF with 1^{t}CK Preamble in Same Bank Group 212
Figure 174:WRITE (BC4) Fixed to READ (BC4) Fixed with 1^{t}CK Preamble in Different Bank Group. 212
Figure 175:WRITE (BC4) Fixed to READ (BC4) Fixed with 1^{t}CK Preamble in Same Bank Group 213
Figure 176:WRITE (BL8/BC4-OTF) to PRECHARGE with 1^{t}CK Preamble 214
Figure 177:WRITE (BC4-Fixed) to PRECHARGE with 1^{t}CK Preamble 214
Figure 178:WRITE (BL8/BC4-OTF) to Auto PRECHARGE with 1^{t}CK Preamble 215
Figure 179:WRITE (BC4-Fixed) to Auto PRECHARGE with 1^{t}CK Preamble. 215
Figure 180:WRITE (BL8/BC4-OTF) with 1^{t}CK Preamble and DBI 216
Figure 181:WRITE (BC4-Fixed) with 1^{t}CK Preamble and DBI 216
Figure 182:Consecutive Write (BL8) with 1^{t}CK Preamble and CA Parity in Different Bank Group 217
Figure 183:Consecutive WRITE (BL8/BC4-OTF) with 1^{t}CK Preamble and Write CRC in Same or Different Bank Group 218
Figure 184:Consecutive WRITE (BC4-Fixed) with 1^{t}CK Preamble and Write CRC in Same or Different Bank Group 219
Figure 185:Nonconsecutive WRITE (BL8/BC4-OTF) with 1^{t}CK Preamble and Write CRC in Same or Different Bank Group 219
Figure 186:Nonconsecutive WRITE (BL8/BC4-OTF) with 2^{t}CK Preamble and Write CRC in Same or Different Bank Group 220
Figure 187:WRITE (BL8/BC4-OTF/Fixed) with 1^{t}CK Preamble and Write CRC in Same or Different Bank Group 221
Figure 188:ZQ Calibration Timing 224
Figure 189:Functional Representation of ODT 225
Figure 190:Synchronous ODT Timing with BL8 228
Figure 191:Synchronous ODT with BC4 228
Figure 192:ODT During Reads. 229
Figure 193:Dynamic ODT (1^{t}CK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled). 231
Figure 194:Dynamic ODT Overlapped with $R_{TT(NOM)}$ (CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled). 232
Figure 195:Asynchronous ODT Timings with DLL Off. 233
Figure 196:V_{REFDQ} Voltage Range 236

List of Tables

Table 1: Key Timing Parameters . . . 2
Table 2: Addressing . . . 2
Table 3: Ball Descriptions . . . 18
Table 4: State Diagram Command Definitions . . . 24
Table 5: Address Pin Mapping . . . 33
Table 6: MR0 Register Definition . . . 33
Table 7: Burst Type and Burst Order . . . 35
Table 8: Address Pin Mapping . . . 37
Table 9: MR1 Register Definition . . . 37
Table 10: Addictive Latency (AL) Settings . . . 39
Table 11: TDQS Function Matrix . . . 40
Table 12: Address Pin Mapping . . . 41
Table 13: MR2 Register Definition . . . 41
Table 14: Address Pin Mapping . . . 44
Table 15: MR3 Register Definition . . . 44
Table 16: Address Pin Mapping . . . 47
Table 17: MR4 Register Definition . . . 47
Table 18: Address Pin Mapping . . . 50
Table 19: MR5 Register Definition . . . 50
Table 20: Address Pin Mapping . . . 53
Table 21: MR5 Register Definition . . . 53
Table 22: Truth Table – Command . . . 55
Table 23: Truth Table – CKE . . . 57
Table 24: MR Settings for Leveling Procedures . . . 65
Table 25: DRAM TERMINATION Function in Leveling Mode . . . 66
Table 26: Auto Self Refresh Mode . . . 73
Table 27: MR3 Setting for the MPR Access Mode . . . 75
Table 28: DRAM Address to MPR UI Translation . . . 76
Table 29: MPR Page and MPRx Definitions . . . 76
Table 30: MPR Readout Serial Format . . . 78
Table 31: MPR Readout – Parallel Format . . . 79
Table 32: MPR Readout Staggered Format, x4 . . . 80
Table 33: MPR Readout Staggered Format, x4 – Consecutive READs . . . 80
Table 34: MPR Readout Staggered Format, x8 and x16 . . . 80
Table 35: Mode Register setting for CA Parity . . . 95
Table 36: Timing Parameter . . . 101
Table 37: V_{REFDQ} Range and Levels . . . 104
Table 38: V_{REFDQ} Settings (V_{DDQ} = 1.2V) . . . 109
Table 39: Connectivity Mode Pin Description and Switching Levels . . . 110
Table 40: PPR MR0 Guard Key Settings . . . 115
Table 41: DDR4 PPR Timing Parameters . . . 118
Table 42: DDR4 sPPR Timing Parameters . . . 119
Table 43: DDR4 Repair Mode Support Identifier . . . 119
Table 44: MAC Encoding of MPR Page 3 MPR3 . . . 120
Table 45: Normal ^{t}REFI Refresh (TCR Disabled) . . . 124
Table 46: Normal ^{t}REFI Refresh (TCR Enabled) . . . 125
Table 47: MRS Definition . . . 126
Table 48: REFRESH Command Truth table . . . 126
Table 49: ^{t}REFI and ^{t}RFC Parameters . . . 127
Table 50: Power-Down Entry Definitions . . . 136
Table 51: CRC Error Detection Coverage . . . 148

Table 52: CRC Data Mapping for x4 Devices, BL8 . . . 150
Table 53: CRC Data Mapping for x8 Devices, BL8 . . . 150
Table 54: CRC Data Mapping for x16 Devices, BL8 . . . 150
Table 55: CRC Data Mapping for x4 Devices, BC4 . . . 151
Table 56: CRC Data Mapping for x8 Devices, BC4 . . . 152
Table 57: CRC Data Mapping for x16 Devices, BC4 . . . 152
Table 58: DBI vs. DM vs. TDQS Function Matrix . . . 157
Table 59: DBI Write, DQ Frame Format (x8) . . . 157
Table 60: DBI Write, DQ Frame Format (x16) . . . 157
Table 61: DBI Read, DQ Frame Format (x8) . . . 158
Table 62: DBI Read, DQ Frame Format (x16) . . . 158
Table 63: DM vs. TDQS vs. DBI Function Matrix . . . 159
Table 64: Data Mask, DQ Frame Format (x8) . . . 159
Table 65: Data Mask, DQ Frame Format (x16) . . . 159
Table 66: CWL Selection . . . 161
Table 67: DDR4 Bank Group Timings . . . 167
Table 68: Termination State Table . . . 226
Table 69: Read Termination Disable Window . . . 226
Table 70: ODT Latency at DDR4-1600/-1866/-2133/-2666/-3200 . . . 227
Table 71: Dynamic ODT Latencies and Timing (1^{t}CK Preamble Mode and CRC Disabled) . . . 230
Table 72: Dynamic ODT Latencies and Timing with Preamble Mode and CRC Mode Matrix . . . 231
Table 73: Absolute Maximum Ratings . . . 234
Table 74: Temperature Range . . . 234
Table 75: Recommended Supply Operating Conditions . . . 235
Table 76: V_{DD} Slew Rate . . . 235
Table 77: Leakages . . . 235
Table 78: V_{REFDQ} Specification . . . 236
Table 79: V_{REFDQ} Range and Levels . . . 237

General Notes and Description

Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the x4 and x8 configurations. The DDR4 SDRAM uses an 8n-prefetch architecture to achieve high-speed operation. The 8n-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8n-bit wide, four-clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or overbar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS_n.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[*n*] for bank group, BA[*n*] for bank address, and A[*n*] for row/col address.
- The NOP command is not allowed, except when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.
- Not all features described within this document may be available on the Rev. A (first) version.
- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached the stable power-on level and is achieved by toggling CKE at least once every $8192 \times {}^{t}REFI$. In the event CKE is fixed HIGH, toggling CS_n at least once every $8192 \times {}^{t}REFI$ is acceptable.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tri-state depending on the mode register setting.

Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.

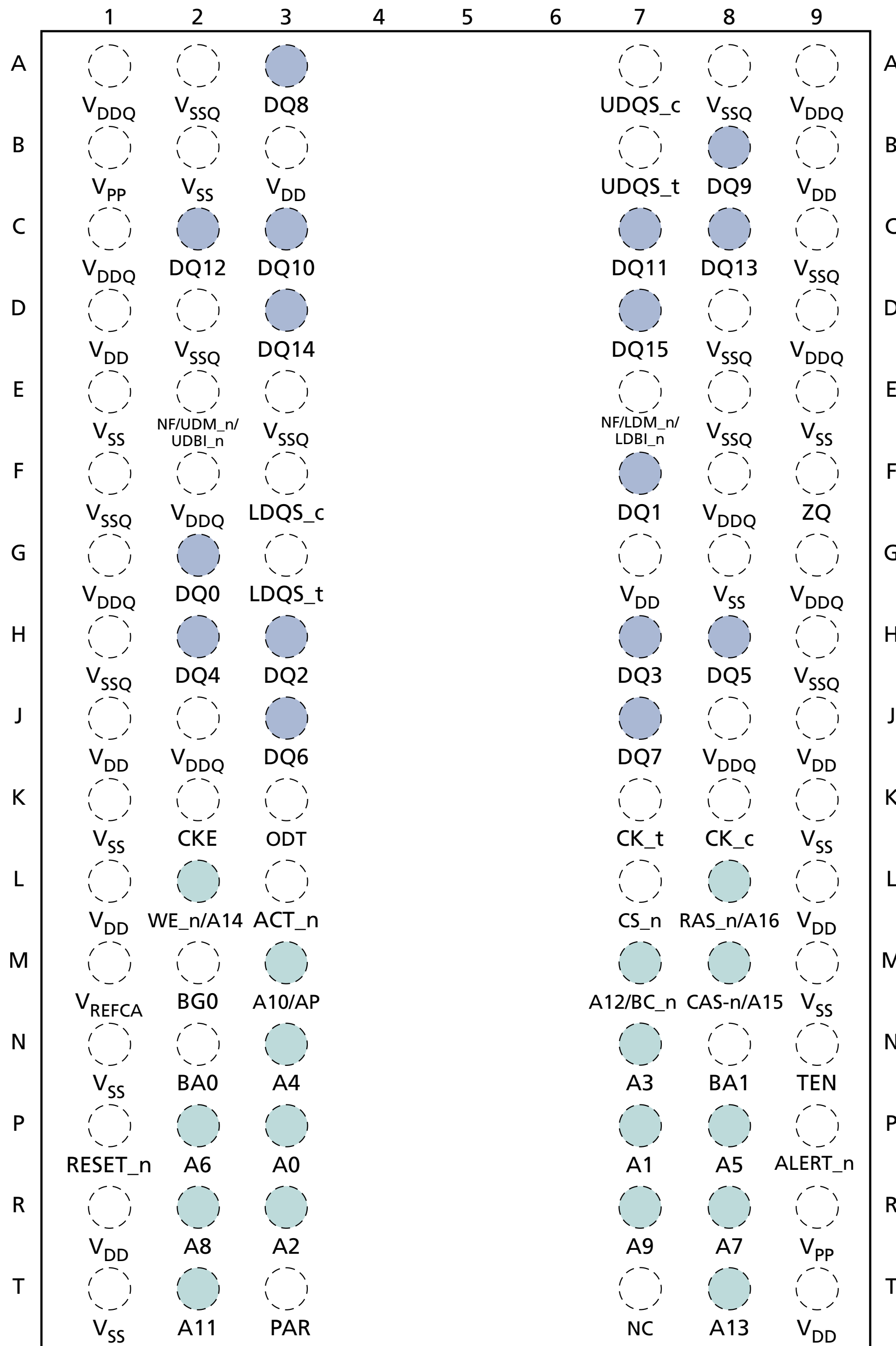
Ball Assignments

Figure 1: 78-Ball – x4, x8 Ball Assignments

	1	2	3	4	5	6	7	8	9	
A	V_{DD}	V_{SSQ}	NF, NF/ TDQS_c				NF, NF/DM_n/ DBI_n/TDQS_t	V_{SSQ}	V_{SS}	A
B	V_{PP}	V_{DDQ}	DQS_c				DQ1	V_{DDQ}	ZQ	B
C	V_{DDQ}	DQ0	DQS_t				V_{DD}	V_{SS}	V_{DDQ}	C
D	V_{SSQ}	DQ4/NC	DQ2				DQ3	DQ5/NC	V_{SSQ}	D
E	V_{SS}	V_{DDQ}	DQ6/NC				DQ7/NC	V_{DDQ}	V_{SS}	E
F	V_{DD}	C2/ODT1	ODT				CK_t	CK_c	V_{DD}	F
G	V_{SS}	C0/CKE1	CKE				CS_n	C1/CS1_n	RFU/TEN	G
H	V_{DD}	WE_n/A14	ACT_n				CAS_n/ A15	RAS_n/A16	V_{SS}	H
J	V_{REFCA}	BG0	A10/AP				A12/BC_n	BG1	V_{DD}	J
K	V_{SS}	BA0	A4				A3	BA1	V_{SS}	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	V_{DD}	A8	A2				A9	A7	V_{PP}	M
N	V_{SS}	A11	PAR				A17/NC	A13	V_{DD}	N

Notes: 1. See Ball descriptions.
2. A comma "," separates the configuration; a slash "/" defines a selectable function. For example: Ball A7 = NF, NF/DM_n/DBI_n/TDQS_t where NF applies to the x4 configuration only. NF/DM_n/DBI_n/TDQS_t applies to the x8 configuration only and is selectable between NF, DM_n, DBI_n, or TDQS_t via MRS.
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).
4. G9 may be RFU and not assigned as TEN on some die revisions as TEN is not required on 4Gb x4 and x8 offerings.

Figure 2: 96-Ball FBGA – x16 Ball Assignments



Notes:
1. See Ball Descriptions.
2. A slash "/" defines a selectable function. For example: Ball E7 = NF/LDM_n. If data mask is enabled via the MRS, ball E7 = LDM_n. If data mask is disabled in the MRS, E7 = NF (no function).
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Ball Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 devices. All pins listed may not be supported on the device defined in this data sheet. See the Ball Assignments section to review all pins used on this device.

Table 3: Ball Descriptions

Symbol	Type	Description
A[17:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts, and A17 is only used on some 16Gb parts
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
ACT_n	Input	**Command input:** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	**Bank address inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	**Stack address inputs:** These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKE	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.

Table 3: Ball Descriptions

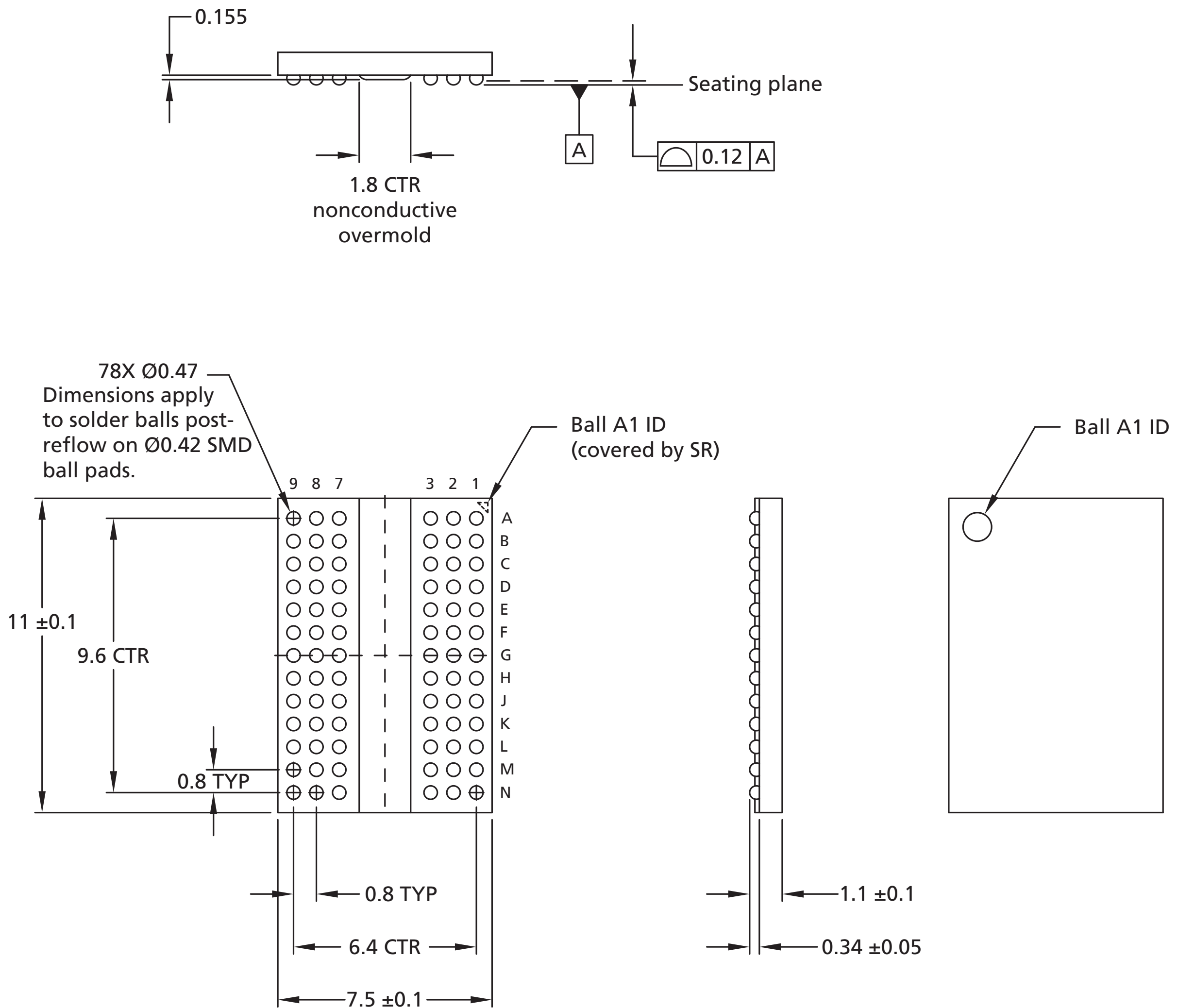
Symbol	Type	Description
CS_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_n, UDM_n LDM_n	Input	**Input data mask:** DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported on x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration: UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask section.
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for the x4 and x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PAR	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960 mV for DC HIGH and 240 mV for DC LOW).
TEN	Input	**Connectivity test mode:** TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW).
DQ	I/O	**Data input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If write CRC is enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal V REF level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, the R_{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DBI_n, UDBI_n, LDBI_n	I/O	**DBI input/output:** Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[15:8], and LDBI_n is associated with DQ[7:0]. The DBI feature is not supported on the x4 configuration. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion section.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	I/O	**Data strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, DQSL corresponds to the data on DQ[7:0]; DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.

Table 3: Ball Descriptions

Symbol	Type	Description
ALERT_n	Output	**Alert output:** This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/address parity error and the CRC data error when either of these functions is enabled in the mode register.
TDQS_t, TDQS_c	Output	**Termination data strobe:** TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the DATA MASK (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
V_{DD}	Supply	**Power supply:** 1.2V ±0.060V.
V_{DDQ}	Supply	**DQ power supply:** 1.2V ±0.060V.
V_{PP}	Supply	**DRAM activating power supply:** 2.5V –0.125V/+0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground.
ZQ	Reference	**Reference ball for ZQ calibration:** This ball is tied to an external 24Ω resistor (RZQ), which is tied to V_{SSQ}.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** May have internal connection present but has no function.

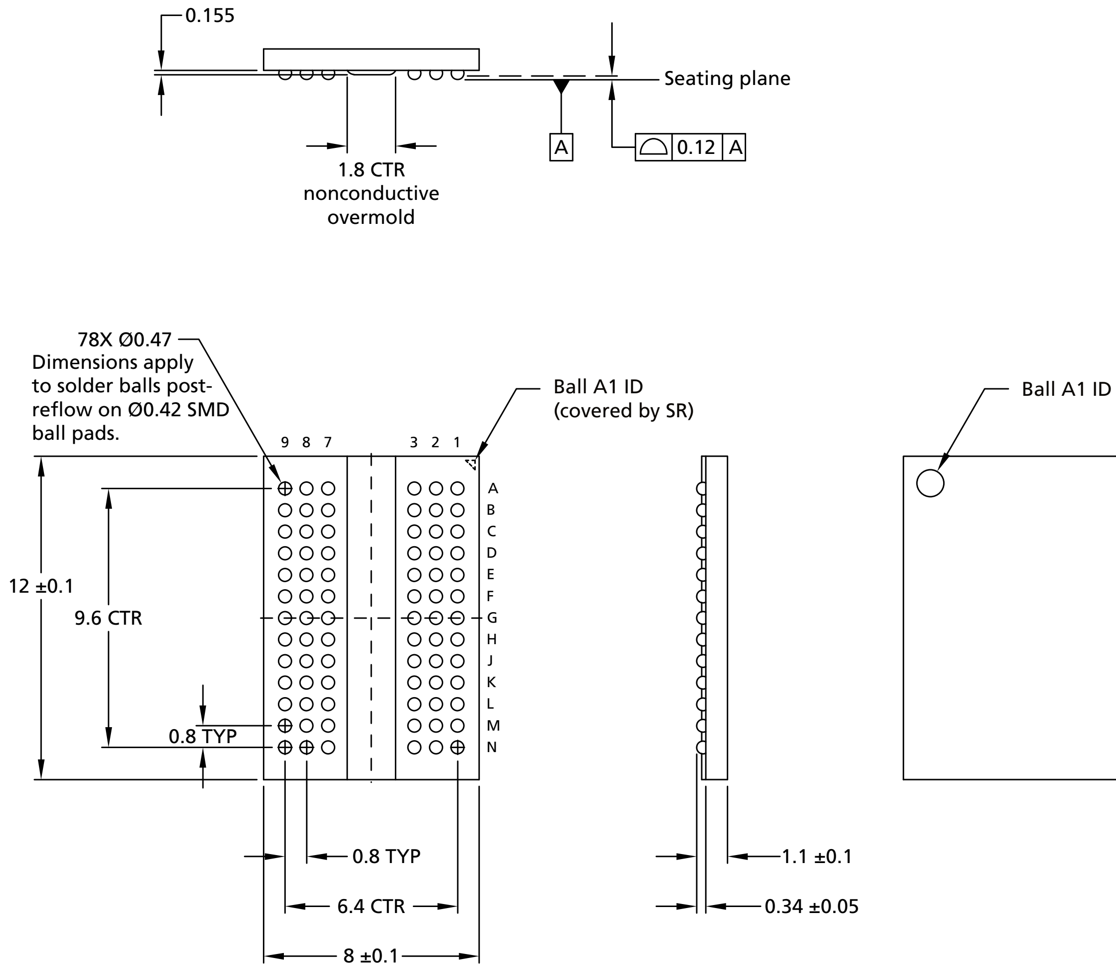
Package Dimensions

Figure 3: 78-Ball FBGA – x4, x8; "SAF"



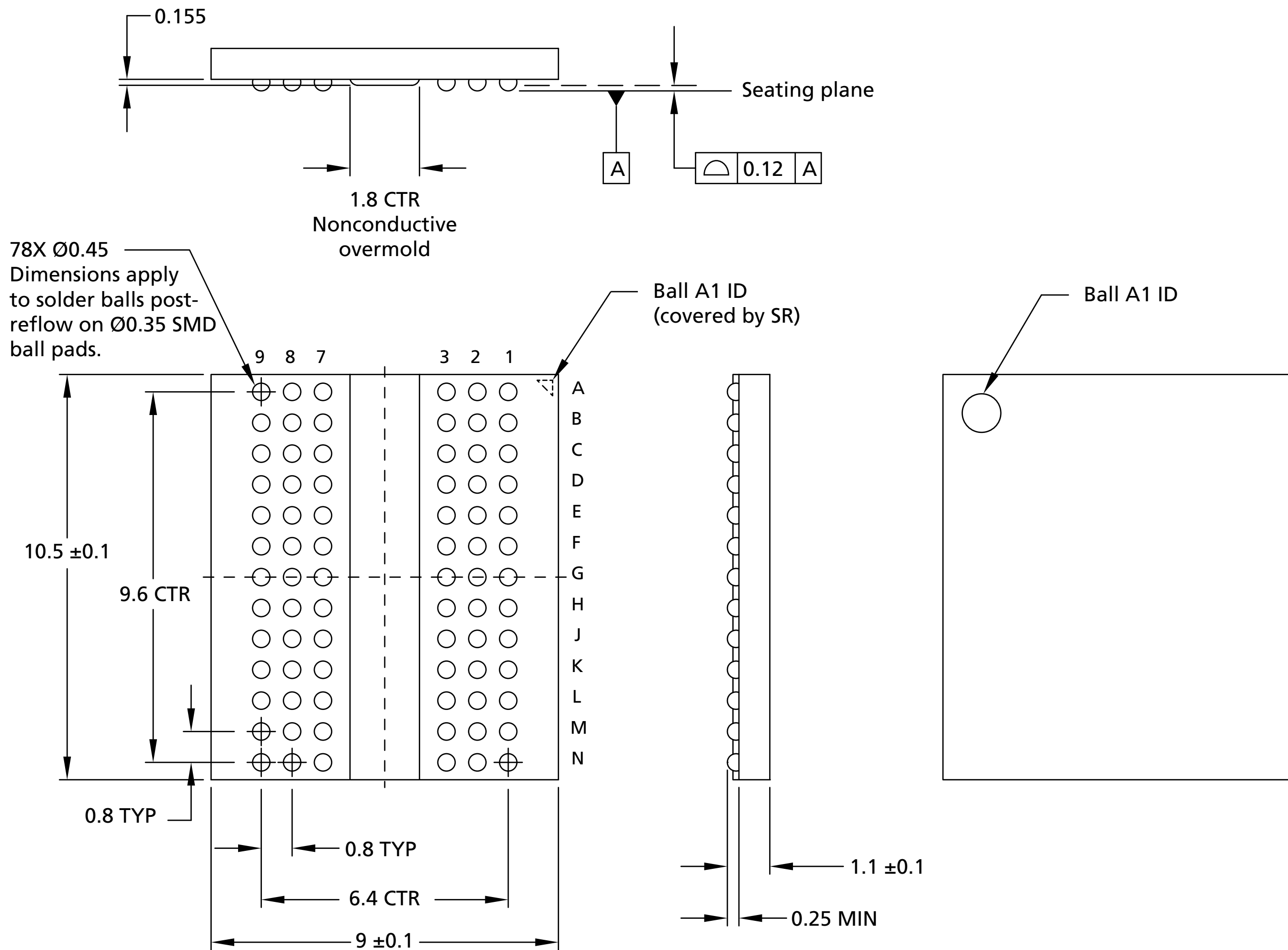
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (Pb-free 96.5%, Sn, 3% Ag, 0.2% Cu).

Figure 4: 78-Ball FBGA – x4, x8; "WEF"



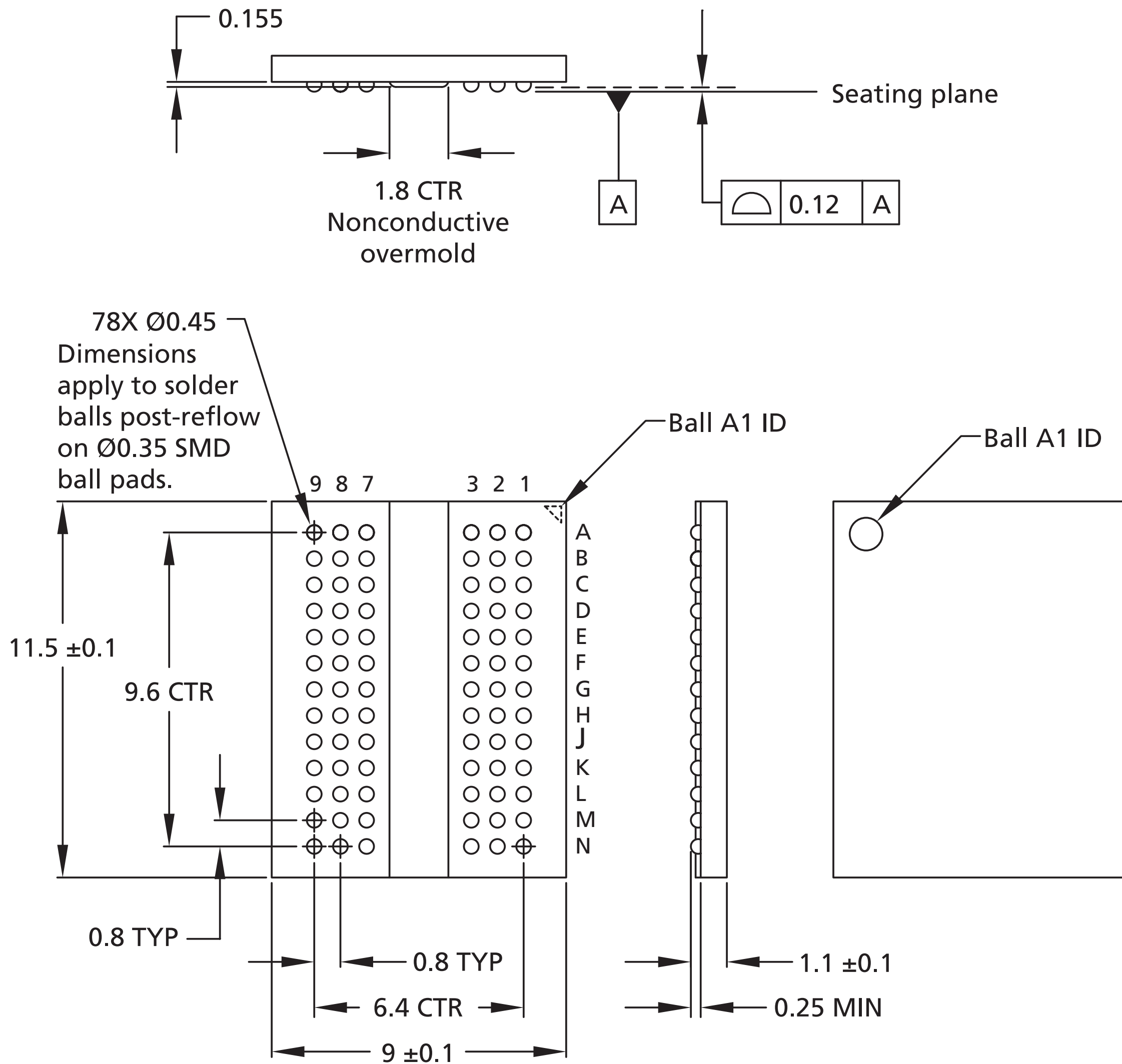
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (Pb-free 96.5%, Sn, 3% Ag, 0.2% Cu).

Figure 5: 78-Ball FBGA – x4, x8; “RHF”



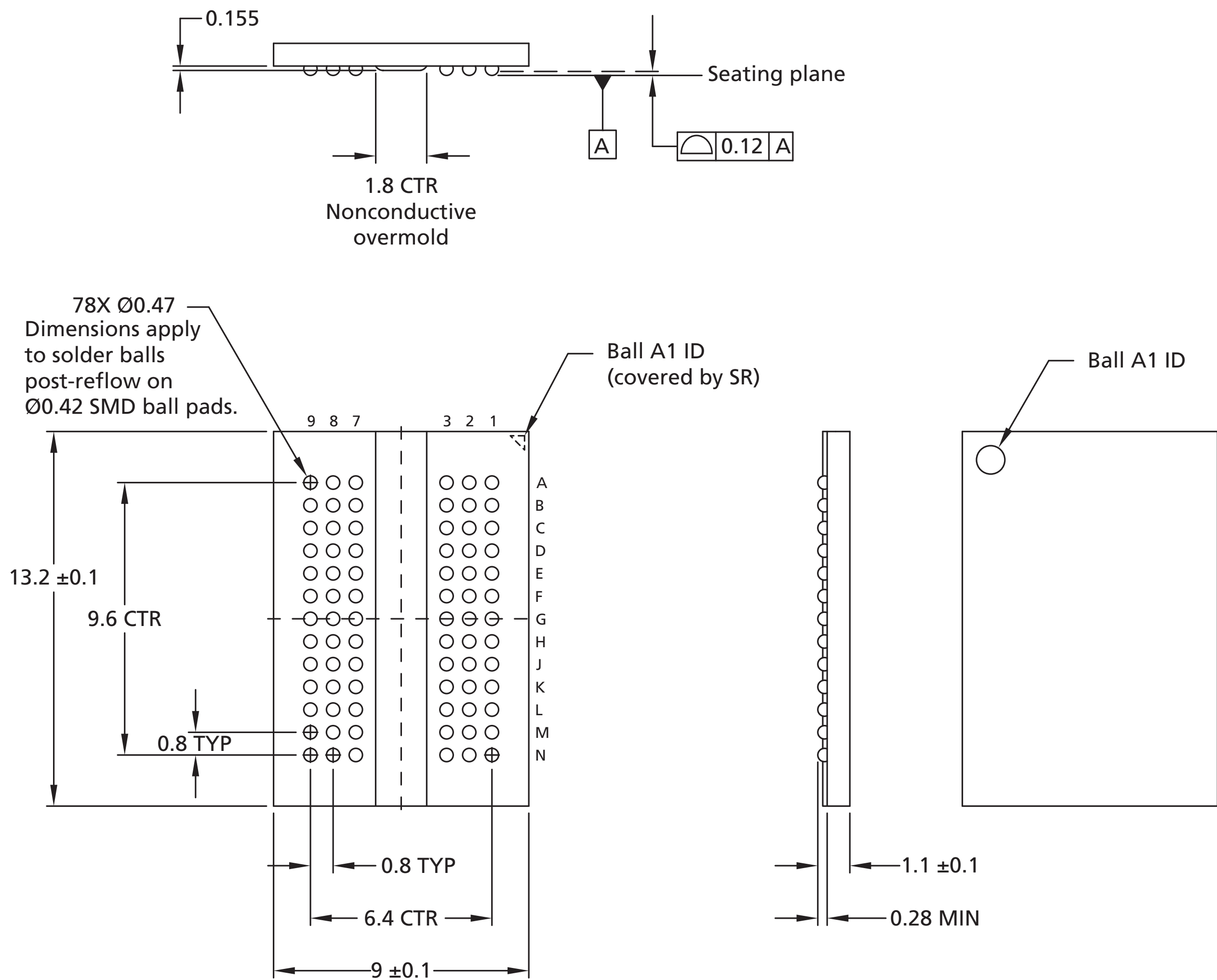
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (Pb-free 96.5% Sn, 3% Ag, 0.2% Cu).

Figure 6: 78-Ball FBGA – x4, x8; "GKF"



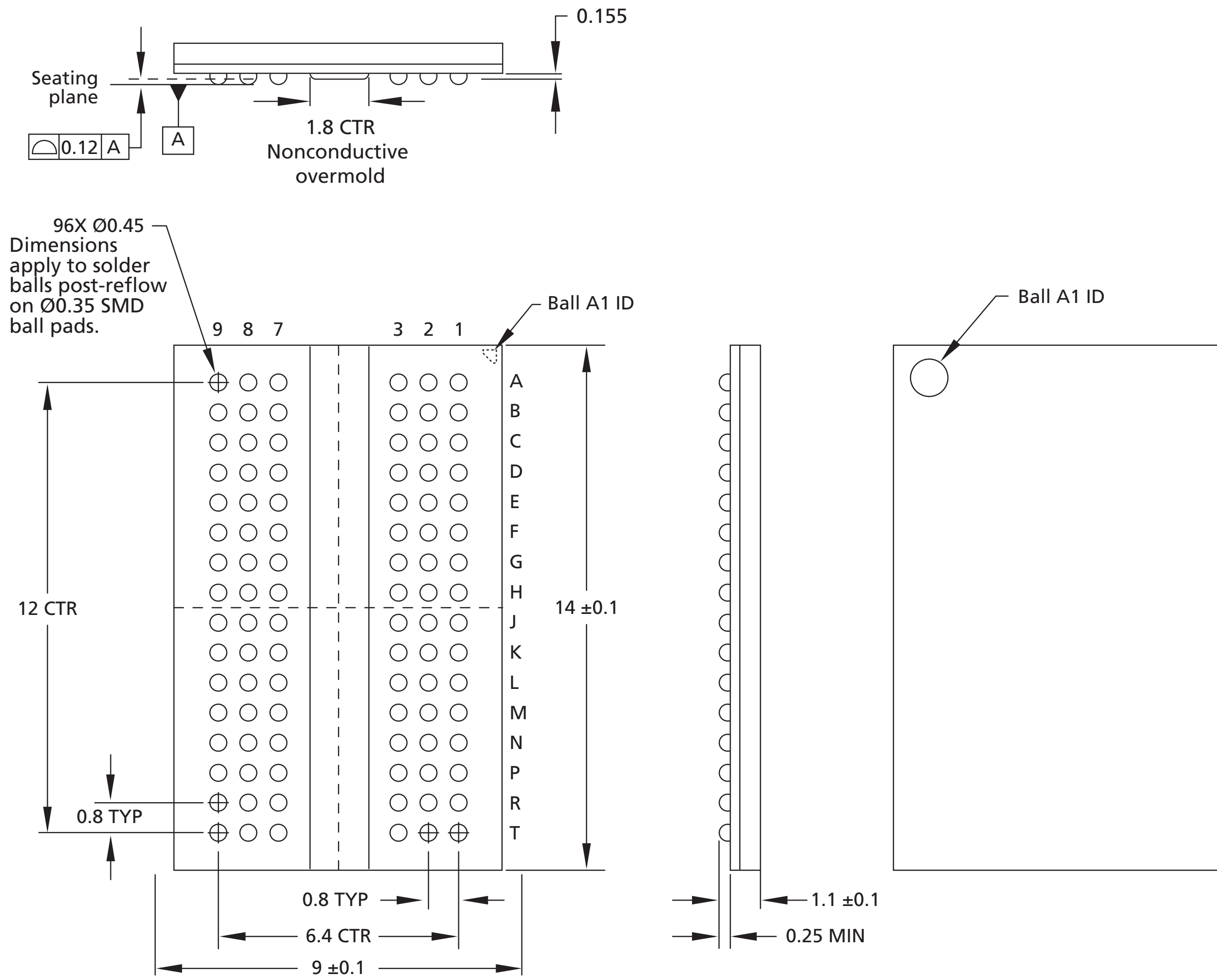
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (Pb-free 96.5% Sn, 3% Ag, 0.5% Cu).

Figure 7: 78-Ball FBGA – x4, x8; “PMF”



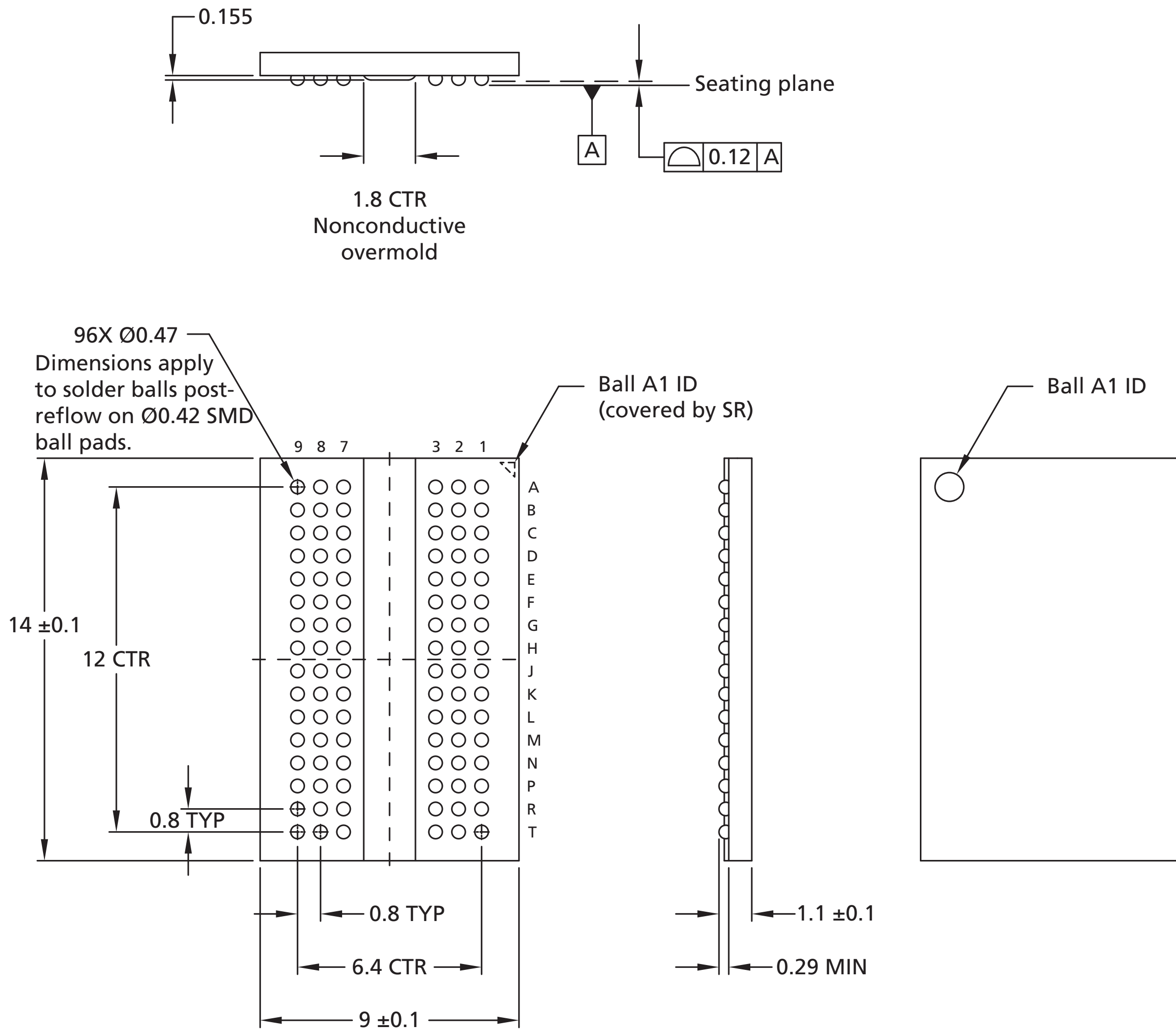
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (Pb-free 96.5% Sn, 3% Ag, 0.5% Cu).

Figure 8: 96-Ball FBGA – x16; “HAF“



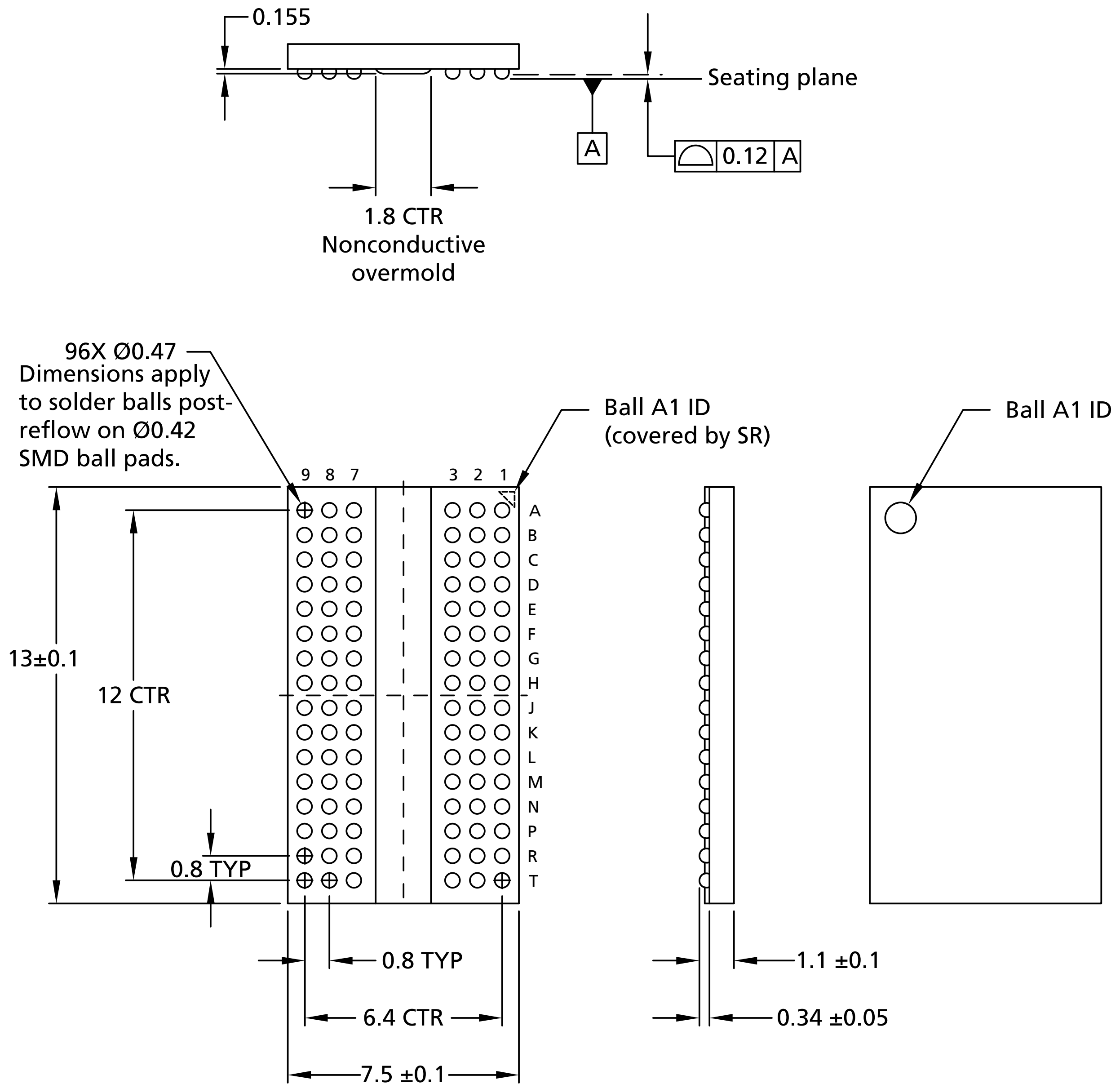
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (Pb-free 96.5% Sn, 3% Ag, 0.5% Cu).

Figure 9: 96-Ball FBGA – x16; "GEF"



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (Pb-free 96.5% Sn, 3% Ag, 0.3% Cu).

Figure 10: 96-Ball FBGA – x16; "DD"



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (Pb-free 96.5% Sn, 3% Ag, 0.2% Cu)

State Diagram

This simplified state diagram provides an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Figure 11: Simplified State Diagram

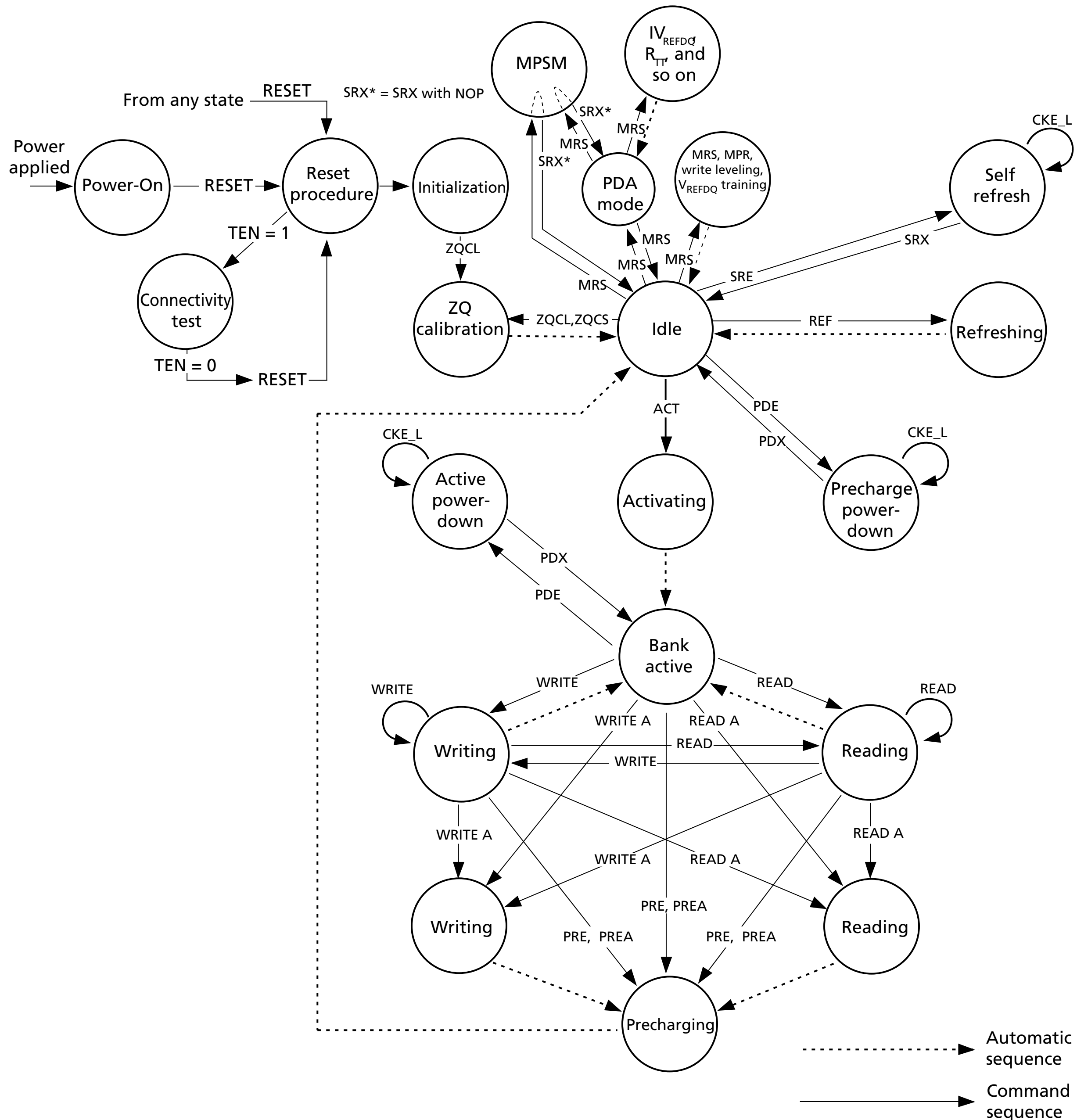


Table 4: State Diagram Command Definitions

Command	Description
ACT	Active
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REF	Refresh, fine granularity refresh
RESET	Start reset procedure
SRE	Self refresh entry
SRX	Self refresh exit
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8 with/without CRC
WRITE A	WRA, WRAS4, WRAS8 with/without CRC
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short

Note: 1. See the Command Truth Table for more details.

Functional Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen banks (4 bank groups with 4 banks for each bank group) for x4/x8 devices, and as eight banks for each bank group (2 bank groups with 4 banks each) for x16 devices. The device uses double data rate (DDR) architecture to achieve high-speed operation. DDR4 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for a device module effectively consists of a single 8*n*-bit-wide, four-clock-cycle-data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected location and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BG[1:0] select the bank group for x4/x8, and BG0 selects the bank group for x16; BA[1:0] select the bank, and A[17:0] select the row. See the Addressing section for more details). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst operation, determine if the auto PRECHARGE command is to be issued (via A10), and select BC4 or BL8 mode on-the-fly (OTF) (via A12) if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

NOTE: The use of the NOP command is allowed only when exiting maximum power saving mode or when entering gear-down mode.

RESET and Initialization Procedure

To ensure proper device function, the power-up and reset initialization default values for the following mode register (MR) settings are defined as:

- Gear-down mode (MR3 A[3]): 0 = 1/2 rate
- Per-DRAM addressability (MR3 A[4]): 0 = disable
- Maximum power-saving mode (MR4 A[1]): 0 = disable
- CS to command/address latency (MR4 A[8:6]): 000 = disable
- CA parity latency mode (MR5 A[2:0]): 000 = disable

Power-Up and Initialization Sequence

The following sequence is required for power-up and initialization:

1. Apply power (RESET_n is to be maintained below 0.2 × V_{DD}; all other inputs may be undefined). RESET_n needs to be maintained for minimum ^{t}PW_RESET_L with stable power. CKE is pulled LOW anytime before RESET_n is being de-asserted (minimum time of 10ns). The power voltage ramp time between 300mV to $V_{DD,min}$ must be no greater than 200ms, and, during the ramp, V_{DD} must be greater than or equal to V_{DDQ} and (V_{DD} - V_{DDQ}) < 0.3V. V_{PP} must ramp at the same time or earlier than V_{DD}, and V_{PP} must be equal to or higher than V_{DD} at all times. After V_{DD} has ramped and reached the stable level, the initialization sequence must be started within 64ms.

   During power-up, either of the following conditions may exist and must be met:

- Condition A:
  - Apply V_{PP} without any slope reversal before or at the same time as V_{DD} and V_{DDQ}.
  - V_{DD} and V_{DDQ} are driven from a single-power converter output and apply V_{DD}/ V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
  - The voltage levels on all balls other than V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
  - V_{TT} is limited to 0.76V MAX when the power ramp is complete.
  - V_{REFCA} tracks V_{DD}/2.
- Condition B:
  - Apply V_{PP} without any slope reversal before or at the same time as V_{DD}.
  - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
  - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
  - The voltage levels on all pins other than V_{PP}, V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

2. After RESET_n is de-asserted, wait for another 500μs until CKE becomes active. During this time, the device will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to power up with the following default MR settings: gear-down mode (MR3 A[3]): 0 = 1/2 rate; per-DRAM addressability (MR3 A[4]): 0 = disable; maximum power-down (MR4 A[1]): 0 = disable; CS to command/address latency (MR4 A[8:6]): 000 = disable; CA parity latency mode (MR5 A[2:0]): 000 = disable. However, it should be assumed that at power up the MR settings are undefined and should be programmed as shown below.
3. Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5 ^{t}CK (whichever is larger) before CKE goes active. Because CKE is a synchronous signal, the corresponding setup time to clock (^{t}IS) must be met. Also, a DESELECT command must be

registered (with ^tIS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of ^tDLLK and ^tZQ INIT.

4. The device keeps its ODT in High-Z state as long as RESET_n is asserted. Further, the SDRAM keeps its ODT in High-Z state after RESET_n de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until ^tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held either LOW or HIGH. If $R_{TT(NOM)}$ is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of ^tDLLK and $^tZQ_{INIT}$.
5. After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, ^tXPR, before issuing the first MRS command to load mode register (^tXPR = MAX (^tXS; 5 x ^tCK).
6. Issue MRS command to load MR3 with all application settings, wait ^tMRD.
7. Issue MRS command to load MR6 with all application settings, wait ^tMRD.
8. Issue MRS command to load MR5 with all application settings, wait ^tMRD.
9. Issue MRS command to load MR4 with all application settings, wait ^tMRD.
10. Issue MRS command to load MR2 with all application settings, wait ^tMRD.
11. Issue MRS command to load MR1 with all application settings, wait ^tMRD.
12. Issue MRS command to load MR0 with all application settings, wait ^tMRD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for ^tDLLK and $^tZQ_{INIT}$ to complete.
15. The device will be ready for normal operation.