

## Features

- Thin small outline package (TSOP-I) configurable as 1 M × 16 or as 2 M × 8 SRAM
- Wide voltage range: 2.2 V–3.6 V
- Ultra-low active power:  
Typical active current: 2 mA at f = 1 MHz
- Ultra-low standby power
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed / power
- Available in Pb-free and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 48-pin TSOP I package

## Functional Description

The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16-bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an

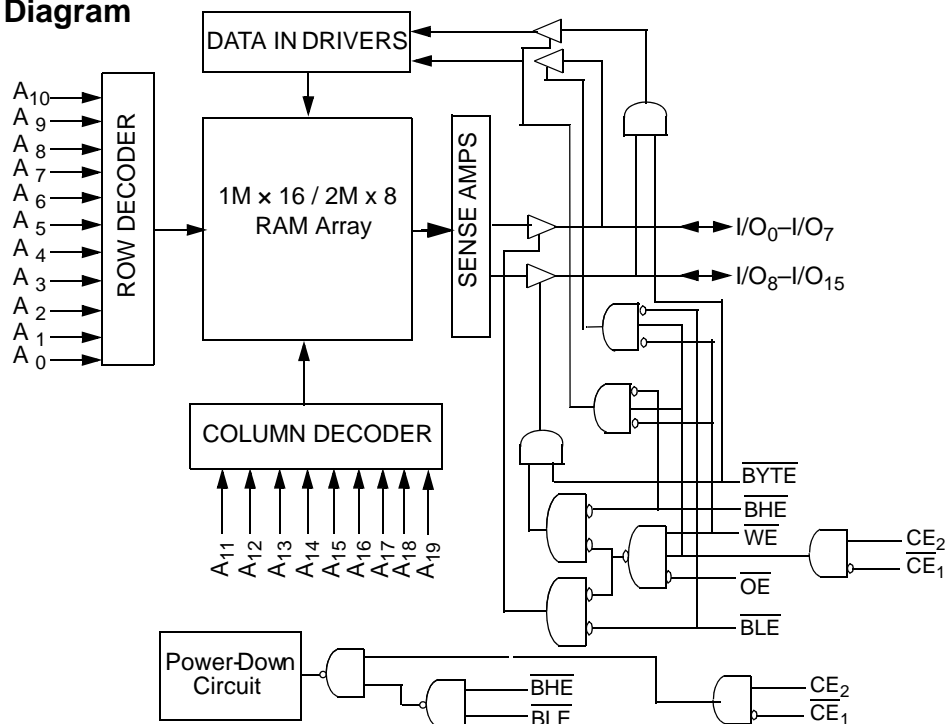
automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

Reading from the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



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## Product Portfolio

| Product       | V <sub>CC</sub> Range (V) |                    |                      | Speed (ns) | Power Dissipation              |     |                    |     |                                     |     |
|---------------|---------------------------|--------------------|----------------------|------------|--------------------------------|-----|--------------------|-----|-------------------------------------|-----|
|               |                           |                    |                      |            | Operating I <sub>CC</sub> (mA) |     |                    |     | Standby I <sub>SB2</sub> ( $\mu$ A) |     |
|               | f = 1 MHz                 |                    | f = f <sub>Max</sub> |            |                                |     |                    |     |                                     |     |
|               | Min                       | Typ <sup>[1]</sup> | Max                  |            | Typ <sup>[1]</sup>             | Max | Typ <sup>[1]</sup> | Max | Typ <sup>[1]</sup>                  | Max |
| CY62167DV30LL | 2.2                       | 3.0                | 3.6                  | 55         | 2                              | 4   | 15                 | 30  | 2.5                                 | 22  |
|               |                           |                    |                      | 70         |                                |     | 12                 | 25  |                                     |     |

## Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [2, 3]

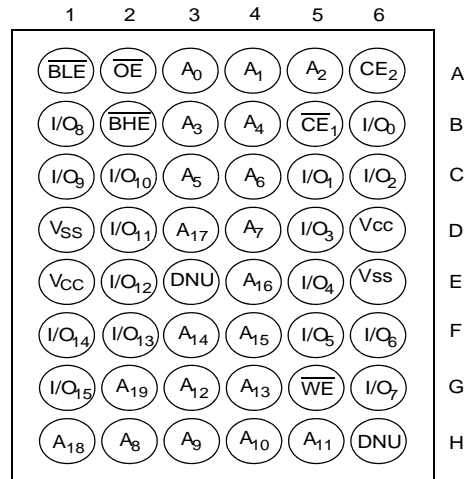
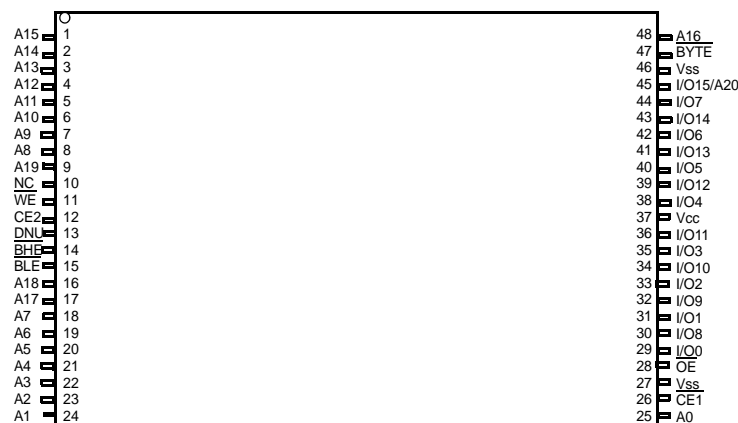


Figure 2. 48-pin TSOP I pinout (Top View) [4]



### Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ.), T<sub>A</sub> = 25 °C.
2. NC pins are not connected on the die.
3. DNU pins have to be left floating.
4. The BYTE pin in the 48-TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 1M X 16 SRAM. The 48-TSOP I package can also be used as a 2 M x 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 2 M x 8 configuration, Pin 45 is A20, while BHE, BLE and I/O8 to I/O14 pins are not used (DNU).

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage to ground potential ..... -0.2 V to  $V_{CC} + 0.3$  V  
 DC voltage applied to outputs in High-Z state <sup>[5, 6]</sup> ..... -0.2 V to  $V_{CC} + 0.3$  V  
 DC input voltage <sup>[5, 6]</sup> ..... -0.2 V to  $V_{CC} + 0.3$  V  
 Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Device        | Range      | Ambient Temperature | $V_{CC}$ <sup>[7]</sup> |
|---------------|------------|---------------------|-------------------------|
| CY62167DV30LL | Industrial | -40 °C to +85 °C    | 2.20 V to 3.60 V        |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description                                | Test Conditions  | CY62167DV30-55 |                    |                | CY62167DV30-70 |                    |                | Unit    |
|-----------|--|--|----------------|--------------------|----------------|----------------|--------------------|----------------|---------|
|           |  |  | Min            | Typ <sup>[8]</sup> | Max            | Min            | Typ <sup>[8]</sup> | Max            |         |
| $V_{OH}$  | Output HIGH voltage                        | $I_{OH} = -0.1$ mA, $V_{CC} = 2.20$ V  | 2.0            | –                  | –              | 2.0            | –                  | –              | V       |
|           |  | $I_{OH} = -1.0$ mA, $V_{CC} = 2.70$ V  | 2.4            |                    |                | 2.4            |                    |                |         |
| $V_{OL}$  | Output LOW voltage                         | $I_{OL} = 0.1$ mA, $V_{CC} = 2.20$ V   | –              | –                  | 0.4            | –              | –                  | 0.4            | V       |
|           |  | $I_{OL} = 2.1$ mA, $V_{CC} = 2.70$ V   |                |                    |                |                |                    |                |         |
| $V_{IH}$  | Input HIGH voltage                         | $V_{CC} = 2.2$ V to 2.7 V  | 1.8            | –                  | $V_{CC} + 0.3$ | 1.8            | –                  | $V_{CC} + 0.3$ | V       |
|           |  | $V_{CC} = 2.7$ V to 3.6 V  | 2.2            |                    |                | 2.2            |                    |                |         |
| $V_{IL}$  | Input LOW voltage                          | $V_{CC} = 2.2$ V to 2.7 V  | -0.3           | –                  | 0.6            | -0.3           | –                  | 0.6            | V       |
|           |  | $V_{CC} = 2.7$ V to 3.6 V  |                |                    | 0.8            |                |                    | 0.8            |         |
| $I_{IX}$  | Input leakage current                      | $GND \leq V_I \leq V_{CC}$   | -1             | –                  | +1             | -1             | –                  | +1             | $\mu$ A |
| $I_{OZ}$  | Output leakage current                     | $GND \leq V_O \leq V_{CC}$ , output disabled   | -1             | –                  | +1             | -1             | –                  | +1             | $\mu$ A |
| $I_{CC}$  | $V_{CC}$ operating supply current          | $V_{CC} = V_{CC(max)}$ , $I_{OUT} = 0$ mA, CMOS levels   | –              | 15                 | 30             | –              | 12                 | 25             | mA      |
|           |  | $f = f_{Max} = 1/t_{RC}$ , $f = 1$ MHz   |                | 2                  | 4              |                | 2                  | 4              |         |
| $I_{SB1}$ | Automatic power-down current – CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{Max}$ (address and data only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ ), $V_{CC} = 3.60$ V | –              | 2.5                | 22             | –              | 2.5                | 22             | $\mu$ A |
| $I_{SB2}$ | Automatic power-down current – CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = 3.60$ V   | –              | 2.5                | 22             | –              | 2.5                | 22             | $\mu$ A |

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full Device AC operation requires linear  $V_{CC}$  ramp from 0 to  $V_{CC(min)}$  and  $V_{CC}$  must be stable at  $V_{CC(min)}$  for 500  $\mu$ s.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.

### Capacitance

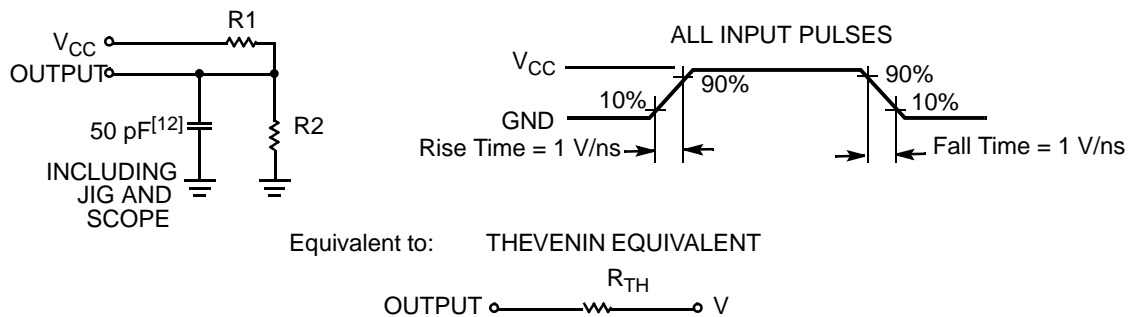
| Parameter <sup>[10]</sup> | Description        | Test Conditions   | Max | Unit |
|---------------------------|--------------------|---|-----|------|
| C <sub>IN</sub>           | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub> | 8   | pF   |
| C <sub>OUT</sub>          | Output capacitance |   | 10  | pF   |

### Thermal Resistance

| Parameter <sup>[10]</sup> | Description                              | Test Conditions  | VFBGA | TSOP I | Unit |
|---------------------------|--|--|-------|--------|------|
| θ <sub>JA</sub>           | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board | 55    | 60     | °C/W |
| θ <sub>JC</sub>           | Thermal resistance (junction to case)    |  | 16    | 4.3    | °C/W |

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



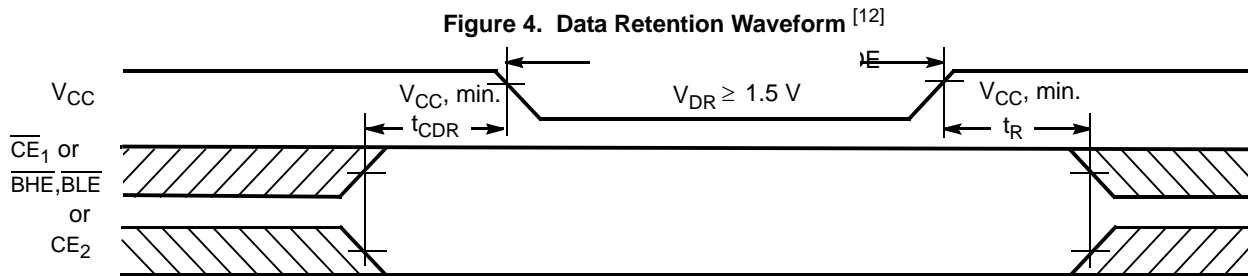
| Parameters      | 2.5 V | 3.0 V | Unit |
|-----------------|-------|-------|------|
| R1              | 16667 | 1103  | Ω    |
| R2              | 15385 | 1554  | Ω    |
| R <sub>TH</sub> | 8000  | 645   | Ω    |
| V <sub>TH</sub> | 1.20  | 1.75  | V    |

## Data Retention Characteristics

Over the Operating Range

| Parameter        | Description                          | Conditions   | Min | Typ <sup>[9]</sup> | Max | Unit          |
|------------------|--------------------------------------|--|-----|--------------------|-----|---------------|
| $V_{DR}$         | $V_{CC}$ for data retention          |  | 1.5 | –                  | –   | V             |
| $I_{CCDR}$       | Data retention current               | $V_{CC} = 1.5\text{ V}$ ,<br>$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | –   | –                  | 10  | $\mu\text{A}$ |
| $t_{CDR}^{[10]}$ | Chip deselect to data retention time |  | 0   | –                  | –   | ns            |
| $t_R^{[11]}$     | Operation recovery time              | CY62167DV30LL-55   | 55  | –                  | –   | ns            |
|                  |                                      | CY62167DV30LL-70   | 70  | –                  | –   |               |

## Data Retention Waveform



### Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .

10. Tested initially and after any design or process changes that may affect these parameters.

11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min.})} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(\text{min.})} \geq 100\text{ }\mu\text{s}$ .

12.  $\overline{BHE}, \overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip can be deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

| Parameter <sup>[13]</sup>          | Description  | 55 ns |     | 70 ns |     | Unit |
|------------------------------------|--|-------|-----|-------|-----|------|
|                                    |  | Min   | Max | Min   | Max |      |
| <b>Read Cycle</b>                  |  |       |     |       |     |      |
| t <sub>RC</sub>                    | Read cycle time  | 55    | –   | 70    | –   | ns   |
| t <sub>AA</sub>                    | Address to data valid  | –     | 55  | –     | 70  | ns   |
| t <sub>OHA</sub>                   | Data hold from address change  | 10    | –   | 10    | –   | ns   |
| t <sub>ACE</sub>                   | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid                 | –     | 55  | –     | 70  | ns   |
| t <sub>DOE</sub>                   | $\overline{OE}$ LOW to data valid  | –     | 25  | –     | 35  | ns   |
| t <sub>LZOE</sub>                  | $\overline{OE}$ LOW to low Z <sup>[14]</sup>                                 | 5     | –   | 5     | –   | ns   |
| t <sub>HZOE</sub>                  | $\overline{OE}$ HIGH to high Z <sup>[14, 15]</sup>                           | –     | 20  | –     | 25  | ns   |
| t <sub>LZCE</sub>                  | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to low Z <sup>[14]</sup>      | 10    | –   | 10    | –   | ns   |
| t <sub>HZCE</sub>                  | $\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to high Z <sup>[14, 15]</sup> | –     | 20  | –     | 25  | ns   |
| t <sub>PU</sub>                    | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power-up                   | 0     | –   | 0     | –   | ns   |
| t <sub>PD</sub>                    | $\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power-down                 | –     | 55  | –     | 70  | ns   |
| t <sub>DBE</sub>                   | $\overline{BLE}/\overline{BHE}$ LOW to data valid                            | –     | 55  | –     | 70  | ns   |
| t <sub>LZBE</sub>                  | $\overline{BLE}/\overline{BHE}$ LOW to low Z <sup>[14]</sup>                 | 10    | –   | 10    | –   | ns   |
| t <sub>HZBE</sub>                  | $\overline{BLE}/\overline{BHE}$ HIGH to high Z <sup>[14, 15]</sup>           | –     | 20  | –     | 25  | ns   |
| <b>Write Cycle <sup>[16]</sup></b> |  |       |     |       |     |      |
| t <sub>WC</sub>                    | Write cycle time   | 55    | –   | 70    | –   | ns   |
| t <sub>SCE</sub>                   | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end                  | 40    | –   | 60    | –   | ns   |
| t <sub>AW</sub>                    | Address setup to write end   | 40    | –   | 60    | –   | ns   |
| t <sub>HA</sub>                    | Address hold from write end  | 0     | –   | 0     | –   | ns   |
| t <sub>SA</sub>                    | Address setup to write start   | 0     | –   | 0     | –   | ns   |
| t <sub>PWE</sub>                   | $\overline{WE}$ pulse width  | 40    | –   | 45    | –   | ns   |
| t <sub>BW</sub>                    | $\overline{BLE}/\overline{BHE}$ LOW to write end                             | 40    | –   | 60    | –   | ns   |
| t <sub>SD</sub>                    | Data setup to write end  | 25    | –   | 30    | –   | ns   |
| t <sub>HD</sub>                    | Data hold from write end   | 0     | –   | 0     | –   | ns   |
| t <sub>HZWE</sub>                  | $\overline{WE}$ LOW to high-Z <sup>[14, 15]</sup>                            | –     | 20  | –     | 25  | ns   |
| t <sub>LZWE</sub>                  | $\overline{WE}$ HIGH to low-Z <sup>[14]</sup>                                | 10    | –   | 10    | –   | ns   |

### Notes

13. Test conditions for all parameters other than Tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.

14. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.

15. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.

16. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.

### Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) [17, 18]

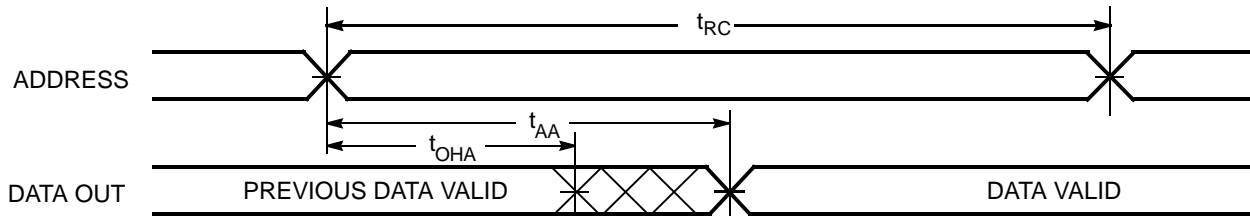
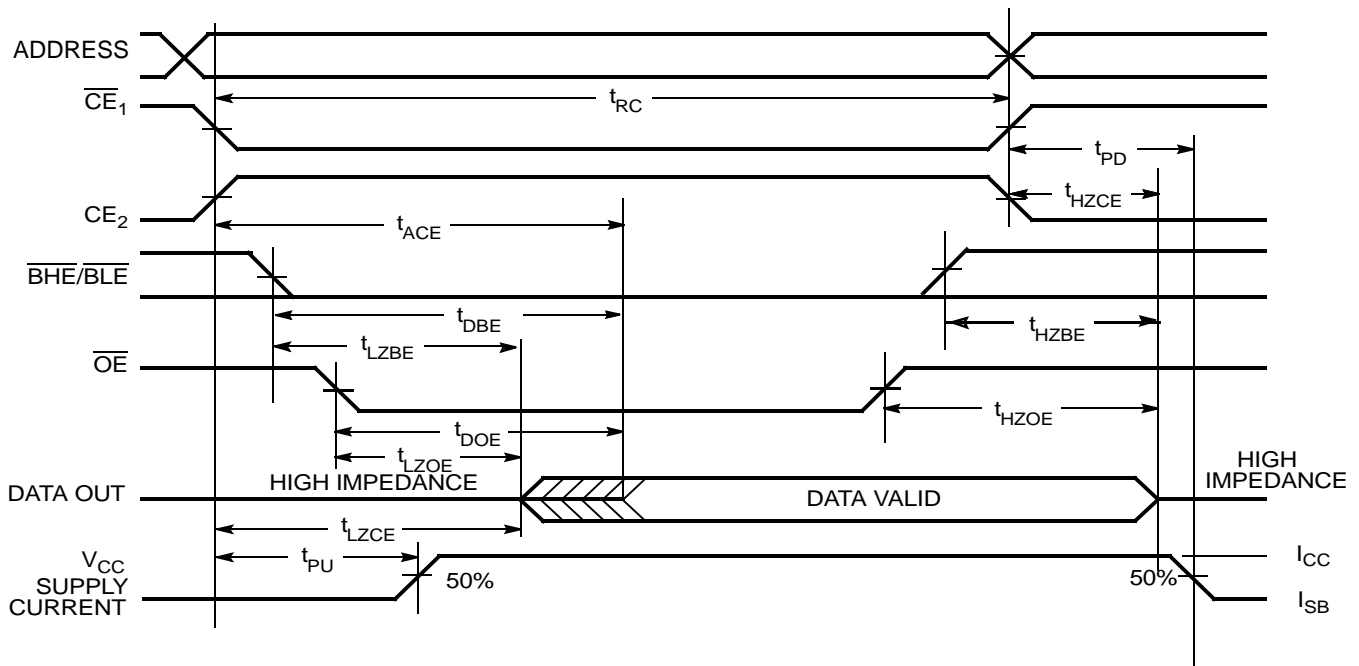


Figure 6. Read Cycle 2 ( $\overline{OE}$  Controlled) [18, 19]



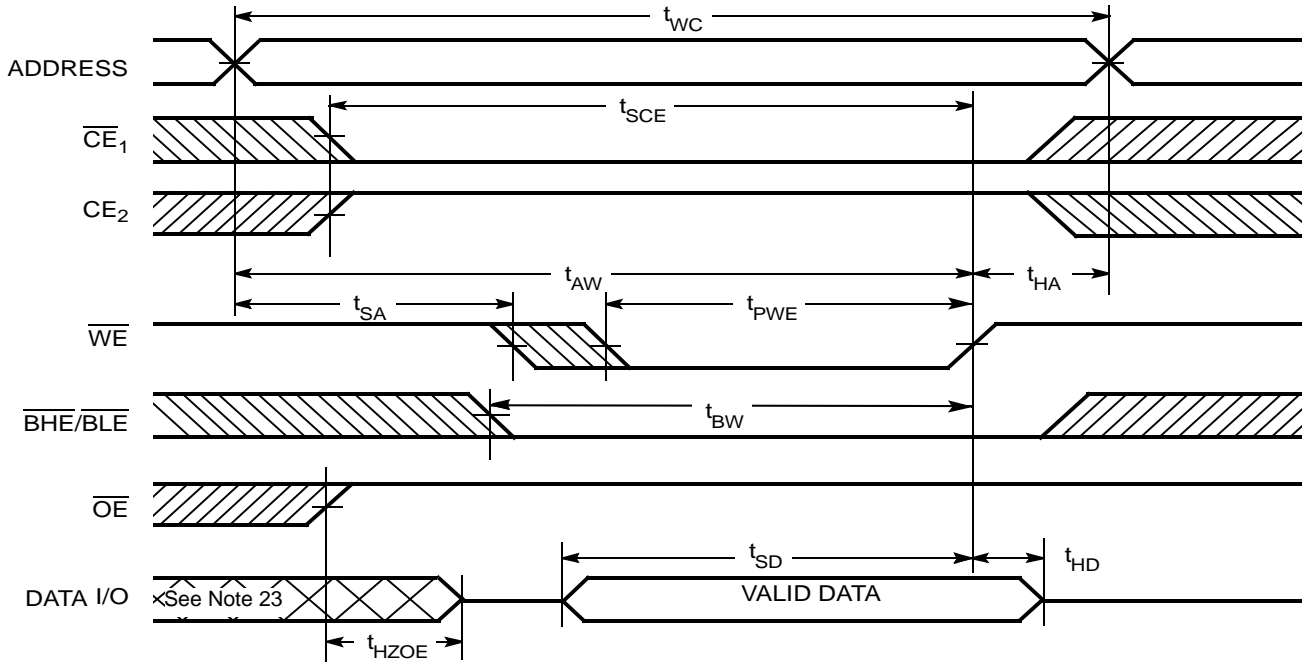
**Notes**

- 17. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1$  =  $V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ , and  $CE_2$  =  $V_{IH}$ .
- 18.  $\overline{WE}$  is HIGH for read cycle.
- 19. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.



Switching Waveforms (continued)

Figure 7. Write Cycle 1 ( $\overline{WE}$  Controlled) [20, 21, 22]



Notes

20. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.

21. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .

22. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.

23. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [24, 25, 26]

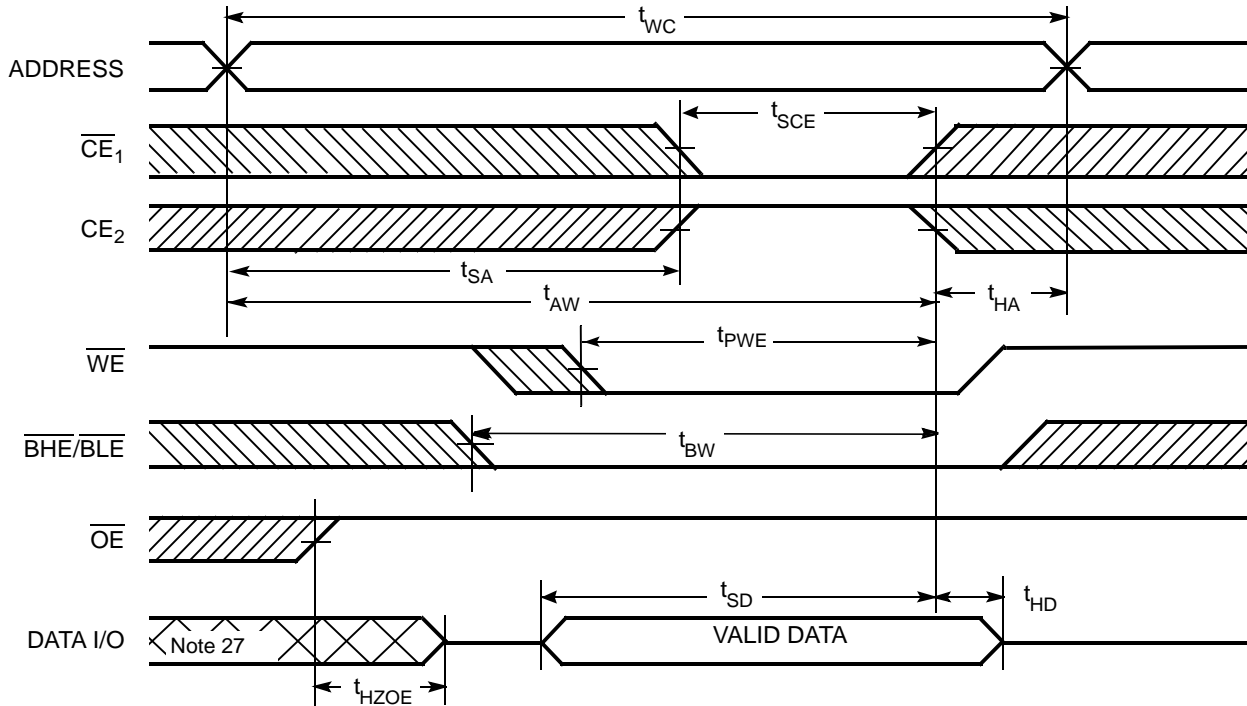
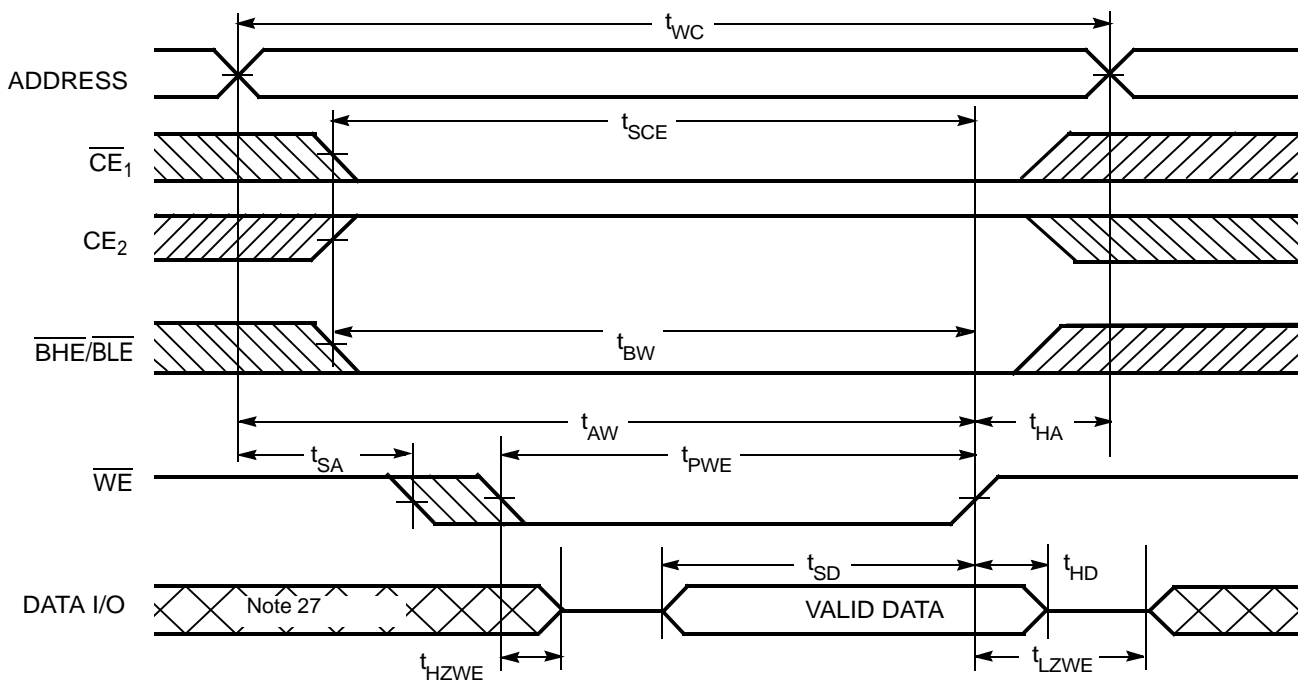


Figure 9. Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [26]



Notes

24. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the Write.

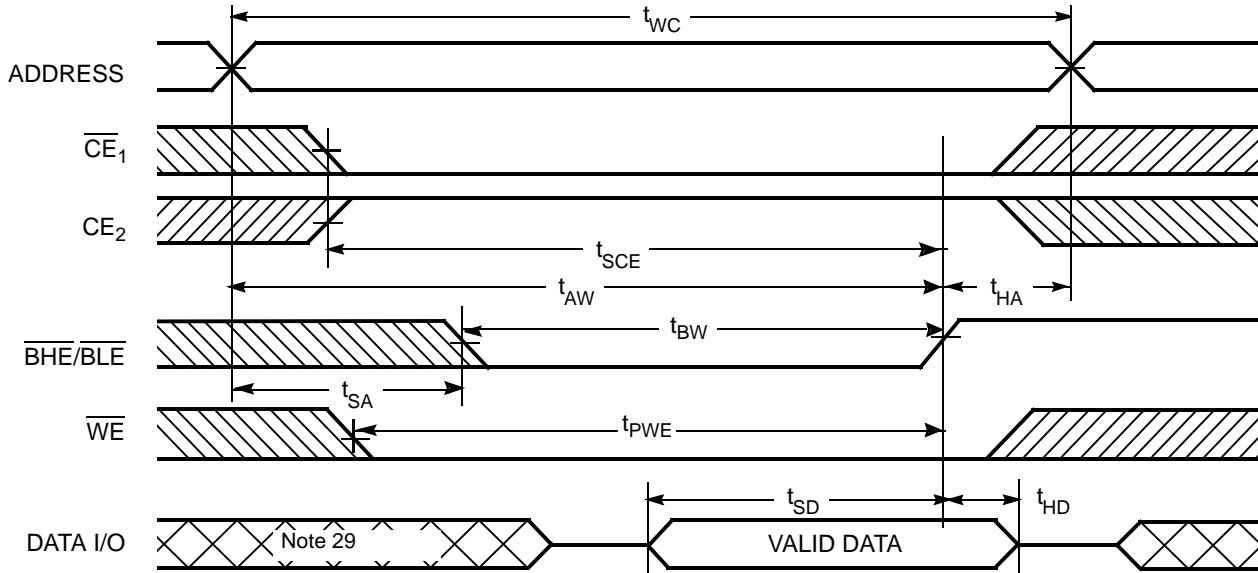
25. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .

26. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.

27. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 10. Write Cycle 4 ( $\overline{\text{BHE/BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [28]



Notes

- 28. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = V_{IH}$ , the output remains in a high-impedance state.
- 29. During this period, the I/Os are in output state and input signals should not be applied.

**Truth Table**

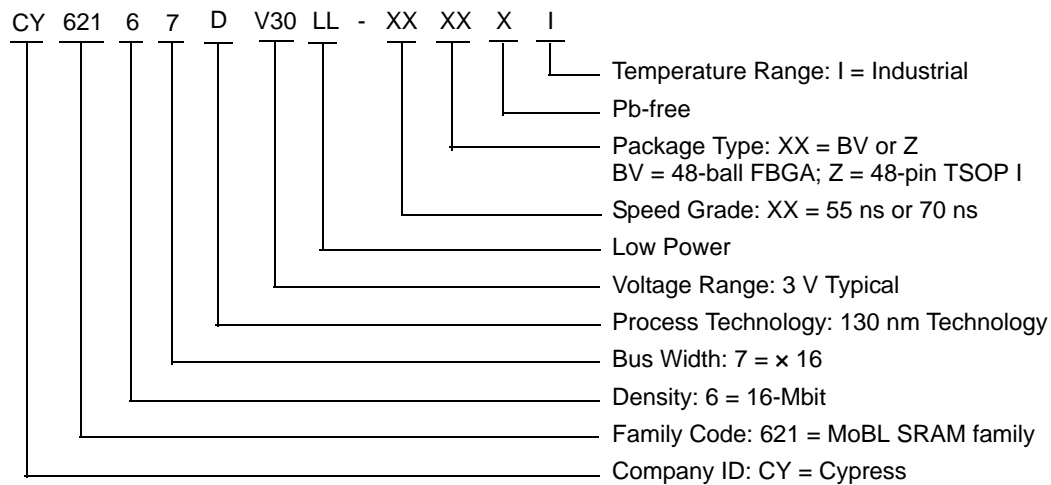
| $\overline{CE}_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs   | Mode                | Power                |
|-------------------|--------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H                 | X      | X               | X               | X                | X                | High Z   | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| X                 | L      | X               | X               | X                | X                | High Z   | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| X                 | X      | X               | X               | H                | H                | High Z   | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| L                 | H      | H               | L               | L                | L                | Data out ( $I/O_0$ – $I/O_{15}$ )                                  | Read                | Active ( $I_{CC}$ )  |
| L                 | H      | H               | L               | H                | L                | High Z ( $I/O_8$ – $I/O_{15}$ );<br>Data out ( $I/O_0$ – $I/O_7$ ) | Read                | Active ( $I_{CC}$ )  |
| L                 | H      | H               | L               | L                | H                | Data out ( $I/O_8$ – $I/O_{15}$ );<br>High Z ( $I/O_0$ – $I/O_7$ ) | Read                | Active ( $I_{CC}$ )  |
| L                 | H      | L               | X               | L                | L                | Data in ( $I/O_0$ – $I/O_{15}$ )                                   | Write               | Active ( $I_{CC}$ )  |
| L                 | H      | L               | X               | H                | L                | High Z ( $I/O_8$ – $I/O_{15}$ );<br>Data in ( $I/O_0$ – $I/O_7$ )  | Write               | Active ( $I_{CC}$ )  |
| L                 | H      | L               | X               | L                | H                | Data in ( $I/O_8$ – $I/O_{15}$ );<br>High Z ( $I/O_0$ – $I/O_7$ )  | Write               | Active ( $I_{CC}$ )  |
| L                 | H      | H               | H               | L                | H                | High Z   | Output disabled     | Active ( $I_{CC}$ )  |
| L                 | H      | H               | H               | H                | L                | High Z   | Output disabled     | Active ( $I_{CC}$ )  |
| L                 | H      | H               | H               | L                | L                | High Z   | Output disabled     | Active ( $I_{CC}$ )  |

## Ordering Information

| Speed (ns) | Ordering Code        | Package Diagram | Package Type                             | Operating Range |
|------------|----------------------|-----------------|--|-----------------|
| 55         | CY62167DV30LL-55BVI  | 51-85178        | 48-ball FBGA (8 × 9.5 × 1 mm)            | Industrial      |
|            | CY62167DV30LL-55BVXI |                 | 48-ball FBGA (8 × 9.5 × 1 mm) Pb-free    |                 |
|            | CY62167DV30LL-55ZXI  | 51-85183        | 48-pin TSOP I (12 × 18.4 × 1 mm) Pb-free |                 |
| 70         | CY62167DV30LL-70BVI  | 51-85178        | 48-ball FBGA (8 × 9.5 × 1 mm)            |                 |

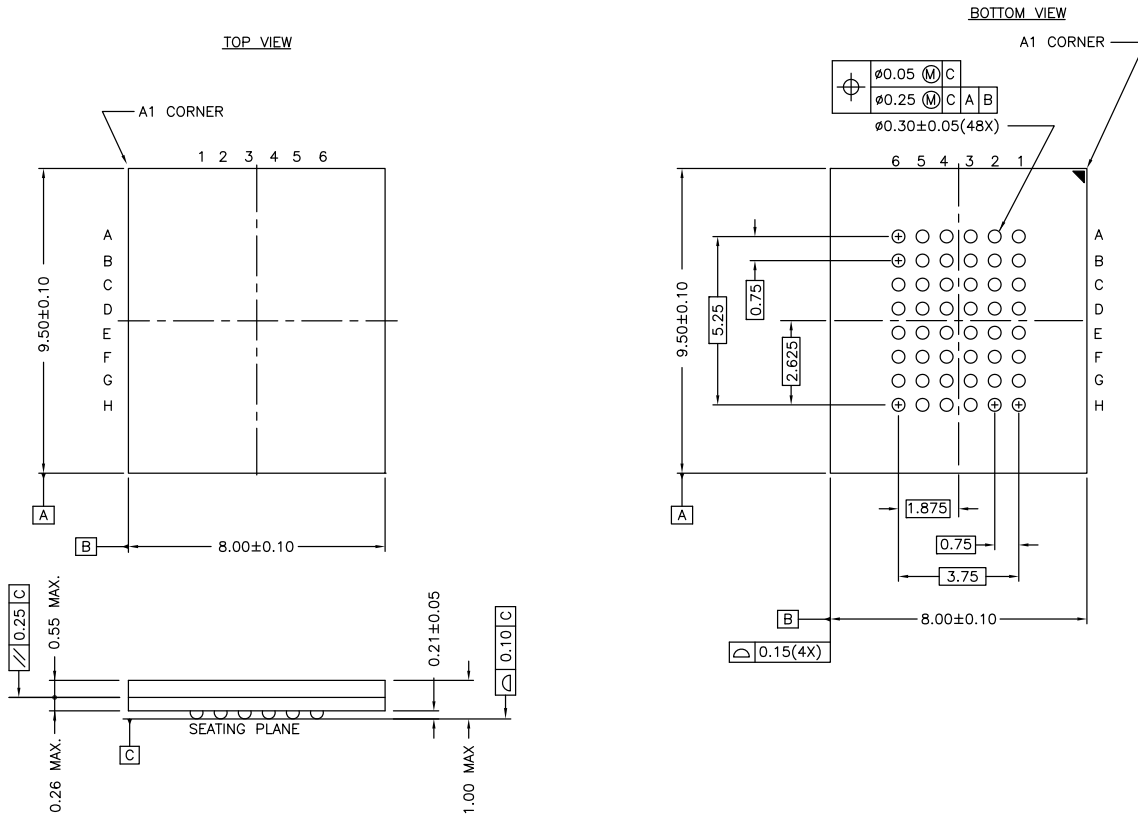
Please contact your local Cypress sales representative for availability of these parts

## Ordering Code Definitions



### Package Diagrams

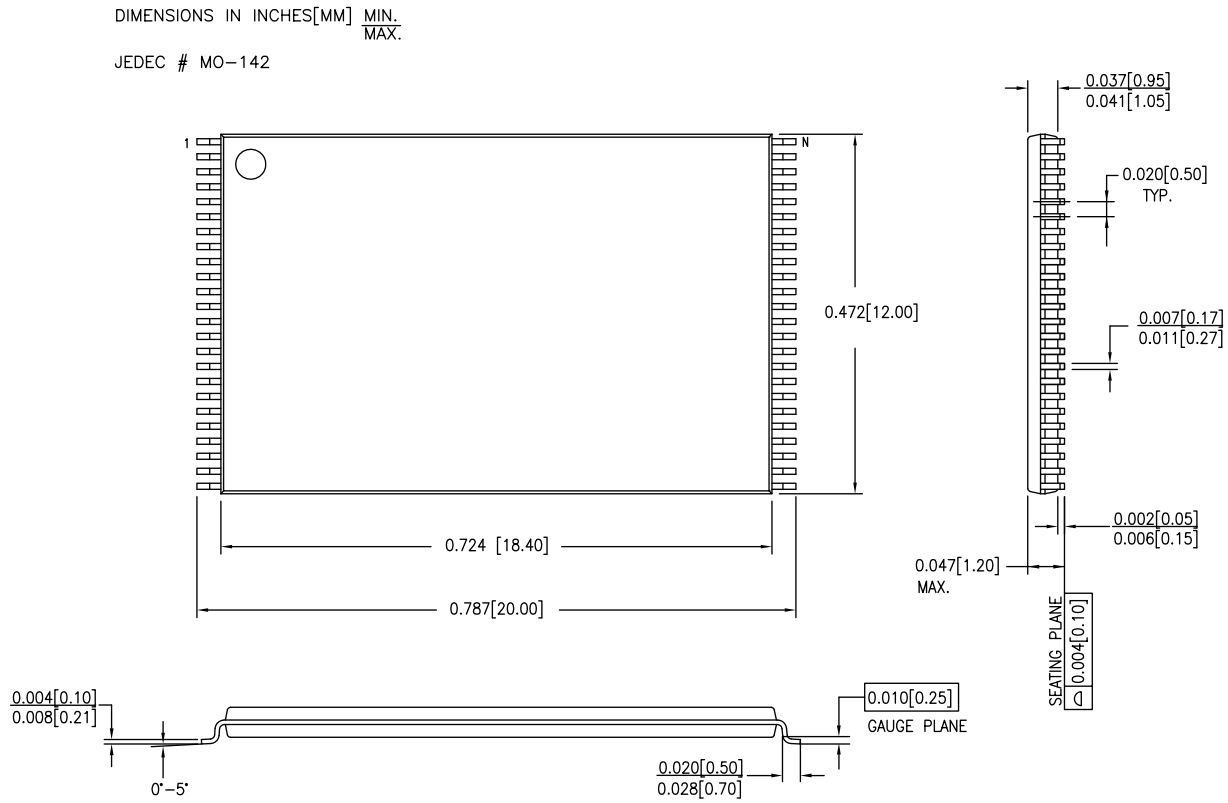
Figure 11. 48-ball VFBGA (8 × 9.5 × 1 mm) BV48B Package Outline, 51-85178



51-85178 \*C

Package Diagrams (continued)

Figure 12. 48-pin TSOP I (12 x 18.4 x 1 mm) Z48A Package Outline, 51-85183



51-85183 \*C

## Acronyms

| Acronym | Description                             |
|---------|---|
| CMOS    | Complementary Metal Oxide Semiconductor |
| I/O     | Input/Output                            |
| SRAM    | Static Random Access Memory             |
| TSOP    | Thin Small Outline Package              |
| VFBGA   | Very Fine-Pitch Ball Grid Array         |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degrees Celsius |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| ns     | nanosecond      |
| Ω      | ohm             |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |



Document History Page

| Document Title: CY62167DV30 MoBL®, 16-Mbit (1 M x 16) Static RAM<br>Document Number: 38-05328 |         |                 |                 |  |
|---|---------|-----------------|-----------------|--|
| Revision  | ECN     | Orig. of Change | Submission Date | Description of Change  |
| **  | 118408  | GUG             | 09/30/02        | New data sheet.  |
| *A  | 123692  | DPM             | 02/11/03        | Changed status from Advanced to Preliminary.<br>Added package diagram  |
| *B  | 126555  | DPM             | 04/25/03        | Minor change: Changed Sunset Owner from DPM to HRT   |
| *C  | 127841  | XRJ             | 09/10/03        | Added 48 TSOP I package  |
| *D  | 205701  | AJU             | See ECN         | Changed BYTE pin usage description for 48 TSOP I package   |
| *E  | 238050  | KKV/AJU         | See ECN         | Replaced 48-ball VFBGA package diagram; Modified Package Name in Ordering Information table from BV48A to BV48B  |
| *F  | 304054  | PCI             | See ECN         | Added 45-ns Speed Bin in AC, DC and Ordering Information tables<br>Added Footnote #12 on page #4<br>Added Pb-free packages on page # 10  |
| *G  | 492895  | VKN             | See ECN         | Modified datasheet to explain x8 configurability.<br>Removed L power bin from the product offering<br>Updated Ordering Information Table   |
| *H  | 2896036 | AJU             | 03/19/10        | Removed 45-ns. Removed inactive parts from Ordering Information.<br>Updated Packaging Information<br>Updated links in Sales, Solutions, and Legal Information.   |
| *I  | 3067267 | RAME            | 11/08/10        | Updated datasheet as per new template<br>Added <a href="#">Ordering Code Definitions</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Updated all table notes to footnote.<br>Package diagram updated 51-85178 from ** to *A  |
| *J  | 3329789 | RAME            | 07/27/11        | Removed references to AN1064 SRAM system guidelines.<br>Updated template according to current CY standards.  |
| *K  | 4108382 | AJU             | 08/29/2013      | Updated <a href="#">Pin Configurations</a> :<br>Removed the note "Ball H6 for the FBGA package can be used to upgrade to a 32M density" and its reference in <a href="#">Figure 1</a> .<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85178 – Changed revision from *A to *C.<br>Updated in new template. |
| *L  | 4192919 | VINI            | 11/15/2013      | No technical updates.<br>Completing Sunset Review.   |
| *M  | 4574377 | VINI            | 11/19/2014      | Added related documentation hyperlink in page 1.   |

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