*Click **here** for production status of specific part numbers.*

MAX9296A

Dual GMSL2/GMSL1 to CSI-2 Deserializer

General Description

The MAX9296A deserializer converts single or dual serial inputs to MIPI CSI-2 outputs. The device operates in either GMSL1 or GMSL2 mode. The MAX9296A also sends and receives side-channel data, enabling full-duplex transmission of forward path video and bidirectional control data over low-cost 50Ω coax or 100Ω STP cables to meet the GMSL2 or GMSL1 channel specification.

The GMSL2 links operate at a fixed rate of 3Gbps or 6Gbps in the forward direction and 187.5Mbps in the reverse direction. In GMSL1 mode, each serial link can be paired with 3.12Gbps or 1.5Gbps GMSL1 serializers or operate up to 4.5Gbps with GMSL2 serializers. The MAX9296A supports mixed GMSL2 and GMSL1 links. The serial inputs operate independently, allowing videos with different timings and resolutions to be received on each input.

Video data from both inputs can be aggregated for output on a single CSI-2 port or replicated on a second port for redundant processing.

Each four-lane CSI-2 port can be programmed to operate with any number of active data lanes. Each CSI-2 port supports 16 virtual channels and allows virtual channel and data type reassignment.

In GMSL1 and GMSL2 modes, the side-channel operates at 9.6kbps to 1Mbps in UART-to-UART mode, and 9.6kbps to 1Mbps in I^2C-to-I^2C mode with clock stretching. Using the side-channel, a µC residing on either end of the link can program serializer, deserializer, and peripheral device registers independent of video timing. In GMSL2 mode, two additional pass-through I^2C or UART channels and a pass-through 50MHz SPI channel provides peripheral control.

The MAX9296A operates over the automotive temperature range of -40°C to +105°C and is AEC-Q100 qualified.

Applications

- High-Definition (2MP+/4MP 60fps) Advanced Driver Assistance Systems (ADAS)
  - Surround View Systems (SVS)
  - Rear View Cameras (RVC)
  - Camera Monitoring Systems (CMS)
  - Driver Monitoring Systems (DMS)
- 8MP 40fps Forward Vision Cameras (FVC)
- Satellite Lidar and Radar Sensors
- Gesture Cameras
- ECU-to-ECU Links

Ordering Information appears at end of data sheet.

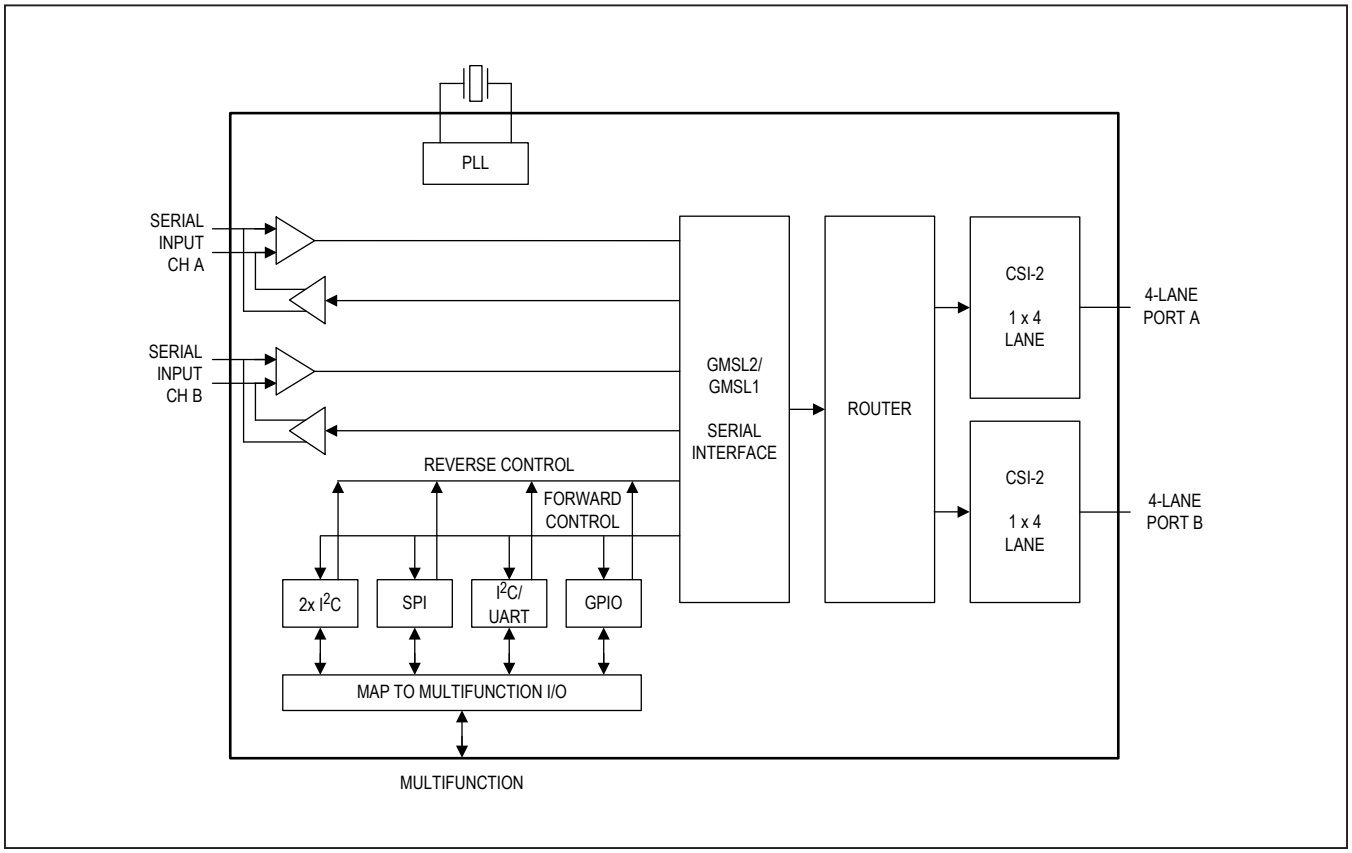
Benefits and Features

- Dual Four-Lane MIPI CSI-2 v1.3 Output Ports
  - Aggregation and Replication Functions
  - 16-Channel Virtual Channel Support
  - Supports RAW8/10/12/14/16/20, RGB565/666/888, YUV422 8-/10-bit, User-Defined, and Generic Long Packet Data Types
- Advanced MIPI D-PHY v1.2 Transmitters
  - 80Mbps to 2.0Gbps per Lane
  - Polarity Flip and Data-Lane Reassignment
- Flexible Input Configuration
  - Independent Serial Inputs Accept Video with Different Timing and Resolution
  - Support for Mixed GMSL2 and GMSL1 Inputs
- Multiple GMSL2 Data Rates for System and Power Flexibility
  - 3Gbps or 6Gbps Forward Link Rates
  - 187.5Mbps Reverse Link Rate
- Backward-Compatible GMSL1 Mode
- Full-Duplex Capability Over a Single Wire
- Ideal for High-Definition Camera Applications
  - Supports 2MP+/4MP at 60fps and 8MP at 40fps
- ASIL-Relevant Functional Safety Features (GMSL2)
  - ASIL-B Compliant in GMSL2 Mode
  - 16-Bit CRC Protection of Side-Channel Data (I^2C, UART, SPI, GPIO) with Retransmission Upon Error Detection
  - Optional 32-Bit Video-Line CRC
  - Video Watermark Insertion and Detection
- Forward and Reverse Channel PRBS for BER Testing of Serial Link
- Line Fault Monitoring
- Continuous Link Margin Monitoring and Optimization
  - Adaptive Equalization Allows 15m Coax Cable with Multiple In-Line Connectors
  - Eye-Opening Monitor for Continuous Link Margin Diagnosis
- Concurrent Side-Channel for Device Configuration and Communicating with Remote Peripherals
  - GMSL2: I^2C/UART, Pass-Through I^2C/UART, SPI, GPIO and Register-Programmable GPIO
  - GMSL1: I^2C/UART, GPI-GPO Link and Register-Programmable GPIO
  - Four Hardware-Programmable Device Addresses
- Compact 7mm x 7mm TQFN Package with Exposed Pad

19-100424; Rev 0; 11/18

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

(All voltages with respect to ground.)

V_{DDIO} .....-0.3V to +3.9V
V_{DD18} .....-0.3V to +2.0V
V_{DD}.....-0.3V to +2.0V
V_{TERM} .....-0.3V to +1.32V
CAP_VDD.....-0.3V to +1.1V
SIO_ (Active State) (Note A) .....(V_{DD18} - 1.1V) to V_{DD18}
SIO_ (Inactive state) (Note A) .....-0.3V to +1.1V
XRES, X2 .....-0.3V to (V_{DD18} + 0.3V)
All Other Pins (Note B).....-0.3V to (V_{DDIO} + 0.3V)
DA/B_P/N, CKA/BP/N (Note C) .....-0.3V to (V_{TERM} + 0.1V)
Continuous Power Dissipation (T_A = +70°C)
TQFN, TQFN-SW (Multilayer, derate 40mW/°C above +70°C).....2200mW
TQFN, TQFN-SW (Single-layer, derate 27.8mW/°C above +70°C).....1527mW
Storage Temperature Range..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C

Note A: Active state means the device is powered up and not in sleep or power-down modes. Inactive means the device is not powered up or powered up in sleep or power-down mode.
Note B: Specified maximum voltage or 3.9V, whichever is lower.
Note C: Specified maximum voltage or 1.36V, whichever is lower.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

48-Pin TQFN

Package Code	T4877+11
Outline Number	**21-0144**
Land Pattern Number	**90-0130**
THERMAL RESISTANCE, SINGLE-LAYER BOARD:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	1°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

48-Pin TQFN-SW (Side-Wettable)

Package Code	T4877Y+11
Outline Number	**21-100045**
Land Pattern Number	**90-100016**
THERMAL RESISTANCE, SINGLE-LAYER BOARD:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	1°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GMSL2 REVERSE CHANNEL SERIAL OUTPUTS (See Figure 1)							
Output Voltage Swing (Single Ended)	V_O	R_L = 100Ω ±1%		190	250	310	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1%, peak-to-peak differential voltage		380	500	620	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)}-V_{OD(L)}\rvert$				25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state		V_{DD18} - 0.45	V_{DD18} - 0.3	V_{DD18} - 0.15	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1%, $\lvert V_{OS(H)} - V_{OS(L)}\rvert$				25	mV
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}		50	55	60	Ω
GMSL1 REVERSE CHANNEL SERIAL OUTPUTS							
Differential High Output Peak Voltage $V_{(SIO\_P)}$ - $V_{(SIO\_N)}$	V_{RODH}	Forward channel disabled (Figure 2)	HIM disabled	30		70	mV
			HIM enabled	50		110	
Differential Low Output Peak Voltage $V_{(SIO\_P)}$ - $V_{(SIO\_N)}$	V_{RODL}	Forward channel disabled (Figure 2)	HIM disabled	-70		-30	mV
			HIM enabled	-110		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled	HIM disabled	30		70	mV
			HIM enabled	50		110	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled	HIM disabled	-70		-30	mV
			HIM enabled	-110		-50	
Differential Output Offset Voltage $(V_{(SIO\_P)} + V_{(SIO\_N)})/2$	V_{DOS}			V_{DD18} - 0.3		V_{DD18}	V
Termination Resistance (Internal)	R_T	Any pin to V_{DD18}		50	55	60	Ω
D-PHY LP TRANSMITTER							
Thevenin High-Level Output Voltage	V_{OH}			0.95	1.2	1.3	V
Thevenin Low-Level Output Voltage	V_{OL}			-50		50	mV
Output Impedance	Z_{OLP}			110			Ω

DC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D-PHY HS TRANSMITTER						
HS Transmit Static Common-Mode Voltage	V_{CMTX}	See Figure 3	150	200	250	mV
V_{CMTX} Mismatch When Output Is Differential-1 Or Differential-0	$\lvert\Delta V_{CMTX(1,0)}\rvert$	$\Delta V_{CMTX(1,0)} = (V_{CMTX(1)} - V_{CMTX(0)})/2$, (Figure 4)			5	mV
HS Transmit Differential Voltage	$\lvert V_{OD}\rvert$	See Figure 3	140	200	270	mV
V_{OD} Mismatch When Output Is Differential-1 Or Differential-0	$\lvert\Delta V_{OD}\rvert$	See Figure 4			14	mV
HS Output High Voltage	V_{OHHS}				360	mV
Single-Ended Output Impedance	Z_{OS}		40	50	62.5	Ω
Single-Ended Output Impedance Mismatch	ΔZ_{OS}				10	%
I/O PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup/ Pulldown Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V

DC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	I_{IN}	All pullup/pulldown devices disabled, V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pull-up Resistor	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Internal Pulldown Resistance	R_{PD}			1		MΩ
Input Capacitance	C_{IN}			3		pF
PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
LINE FAULT DETECTION INPUT (See Figure 25, Figure 26)						
Open Pin Voltage	V_{O0}	LMN0 or LMN2		1.25		V
	V_{O1}	LMN1 or LMN3		0.75		
REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2)						
X1 Input Capacitance	C_{IN_X1}			3		pF
X2 Input Capacitance	C_{IN_X2}			1		pF
Internal X2 Limit Resistor	R_{LIM}			1.2		kΩ
Internal Feedback Resistor	R_{FB}			10		kΩ
Transconductance	g_M			28		mA/V
REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1, X2 UNCONNECTED)						
High-Level Input Voltage	V_{IH}		0.9			V
Low-Level Input Voltage	V_{IL}				0.4	V
Input Impedance	R_{IN}			10		kΩ
X1 Input Capacitance	C_{IN_X1}			3		pF

DC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GMSL2 POWER SUPPLY CURRENT							
Supply Current (Note 4)	I_{DD}	Single 6Gbps link, 5.2Gbps video payload input, RGB888, output on port A, replicated on port B, each port four data lanes, 1.3Gbps per lane	V_{TERM} = 1.26V		31	50	mA
			V_{DD18} = 1.9V		92	120	
			V_{DD} = 1.05V		150	400	
			V_{DD} = 1.26V		150	400	
		Two 6Gbps links, 5.2Gbps video payload input per link, RGB888, link A output on port A, link B output on port B, each port four data lanes, 1.3Gbps per lane	V_{TERM} = 1.26V		33	50	
			V_{DD18} = 1.9V		150	190	
			V_{DD} = 1.05V		240	550	
			V_{DD} = 1.26V		240	550	
Maximum V_{DDIO} Supply Current	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} at 1.9V		44		µA/MHz
			V_{DDIO} at 3.6V		81		
GMSL1 POWER SUPPLY CURRENT							
Supply Current (Note 4)	I_{DD}	Two 4.5Gbps links, 3.6Gbps video payload input per link, HBM, RGB888, link A output on port A, link B output on port B, each port four data lanes, 900Mbps per lane, 60Hz GPI	V_{TERM} = 1.26V		33	50	mA
			V_{DD18} = 1.9V		86	100	
			V_{DD} = 1.05V		115	350	
			V_{DD} = 1.26V		115	350	
			V_{DDIO} = 3.6V		0	1	
MAXIMUM POWER-DOWN AND SLEEP CURRENT							
Maximum Power-Down Current	I_{DD}	V_{DDIO} at 3.6V	T_A = +25°C		6		µA
			T_A = +105°C		6		
		V_{TERM} at 1.26V	T_A = +25°C		1		
			T_A = +105°C		1		
		V_{DD18} at 1.9V	T_A = +25°C		1		
			T_A = +105°C		5		
		V_{DD} at 1.26V	T_A = +25°C		1		
			T_A = +105°C		1		

AC Electrical Characteristics

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Sleep Current	I_{DD}	V_{DDIO} at 3.6V	T_A = +25°C		6		µA
			T_A = +105°C		6		
		V_{TERM} at 1.26V	T_A = +25°C		1		
			T_A = +105°C		1		
		V_{DD18} at 1.9V	T_A = +25°C		20		
			T_A = +105°C		25		
		V_{DD} at 1.26V	T_A = +25°C		1		
			T_A = +105°C		1		
GMSL2 FORWARD CHANNEL SWITCHING CHARACTERISTICS							
Lock Time	t_{LOCK}	From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK (Figure 6)			20		ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packets at SIO_ to valid packets at the CSI-2 output (assumes link locked and registers configured)			0.1ms + (6600 x t_{PCLK})		ms
Maximum Video Latency	t_{VL}	Time from the first pixel in a GMSL2 packet at SIO_ to the first pixel in the CSI-2 output packet (Figure 7)			1 video line + (128 x t_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip			1		µs
GMSL2 REVERSE CHANNEL SERIAL OUTPUTS (SIO_P, SIO_N)							
GMSL Reverse Channel Transmitter Rise/Fall Time	t_R, t_F	20% to 80%, V_O = 250mV, R_L = 100Ω			2300		ps
Total Serial Output p-p Jitter	t_{TSOJ}	PRBS7, single-ended or differential output			0.15		UI
Deterministic Serial Output p-p Jitter	t_{DSOJ}	PRBS7, single-ended or differential output			0.1		UI
GMSL1 SWITCHING CHARACTERISTICS							
Maximum Lock Time	t_{LOCK}	See Figure 8			4		ms
Maximum Power-Up Delay	t_{PU}	See Figure 9			8.5		ms
Maximum Video Latency	t_{VL}	Time from the first pixel in a video line at SIO_ to the first pixel in the CSI-2 output packet (Figure 10)			1 video line + (128 x t_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the chip			1		µs

AC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission, see Figure 2 (Note 2)	100		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission see Figure 2 (Note 2)	100		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included), see Figure 11 (Note 2)			350	µs
D-PHY HS TRANSMITTER						
Common-Level Variations, HF	$\Delta V_{CMTX(HF)}$	> 450MHz (Figure 4) (Note 2)			15	mV_{RMS}
Common-Level Variations, LF	$\Delta V_{CMTX(LF)}$	50MHz–450MHz (Figure 4) (Note 2)			25	mV_{PEAK}
20% to 80% Rise Time and Fall Time	t_R and t_F	(Note 2)			0.4	UI
		(Note 2)	50			ps
Tx Differential Return Loss	Sdd_{TX}	fh_{MAX} = 1.0GHz		-10		dB
		f_{MAX} = 1.5GHz		-8		
Tx Common Mode Return Loss	Scc_{TX}	f_{MAX} = 1.5GHz		-7		dB
Data Lane Bit Rate	DL_{BR}		80		2000	Mbps
Clock Lane Frequency	CL_{FREQ}		40		1000	MHz
CSI-2 Output Inter-packet Spacing	t_{SPACE}			300ns + 370UI		ns
D-PHY LP TRANSMITTER (NOTE 2)						
15% to 85% Rise Time and Fall Time	t_{RLP}/t_{FLP}	(Note 3)			25	ns
30% to 85% Rise Time and Fall Time	t_{REOT}	(Figure 12, Figure 14) (Note 5)			35	ns
Load Capacitance	C_{LOAD}	(Note 3)	0		70	pF
D-PHY DATA-CLOCK TIMING (NOTE 2)						
UI Instantaneous	UI_{INST}		0.5		12.5	ns
UI Variation	ΔUI	UI ≥ 1ns within a single burst	-10%		+10%	UI
		0.667ns ≤ UI ≤ 1ns within a single burst	-5%		+5%	
Data to Clock Skew	T_{SKEW}	0.08 to 1.0Gbps (Figure 15)	-0.15		+0.15	UI_{INST}
		> 1.0 to 1.5Gbps (Figure 15)	-0.2		+0.2	
Static Data to Clock Skew (Tx)	T_{SKEW} Static	> 1.5Gbps (Figure 15)	-0.2		+0.2	UI_{INST}
Dynamic Data to Clock Skew (Tx)	T_{SKEW} Dynamic	> 1.5Gbps (Figure 15)	-0.15		+0.15	UI_{INST}

AC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D-PHY GLOBAL OPERATION TIMING (Note 2)						
Time that the HS Clock Drives by the Transmitter Prior to Any Associated Data Lane Beginning the Transition from LP to HS Mode	$T_{CLK-PRE}$	See Figure 13	8			UI
Time that the Transmitter Drives the Clock Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$T_{CLK\_PREPARE}$	See Figure 13	38		95	ns
TCLK-PREPARE + Time that the Transmitter Drives the HS-0 State Prior to Starting the Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	See Figure 13	300			ns
Transmitted Time Interval from the Start of THS-TRAIL to the Start of the LP-11 State Following an HS Burst	T_{EOT}	See Figure 12, Figure 13, Figure 14			105 + 12 x UI	ns
Time that the Transmitter Drives LP-11 Following an HS Burst	$T_{HS-EXIT}$	See Figure 12, Figure 13, Figure 14	100			ns
Time that the Transmitter Drives the Data Lane LP-00 Line State Immediately Before the HS-0 Line State Starting the HS Transmission	$T_{HS-PREPARE}$	See Figure 12, Figure 13, Figure 14	40 + 4 x UI		85 + 6 x UI	ns
THS-PREPARE + Time that the Transmitter Drives the HS-0 State Prior to Transmitting the Sync Sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	See Figure 12, Figure 14	145 + 10 x UI			ns

AC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time that the Transmitter Drives the Flipped Differential State After Last Payload Data Bit of an HS Transmission Burst	$T_{HS-TRAIL}$	See Figure 12, Figure 14	60 + 4 x UI			ns
Initialization Time	T_{INIT}		100			µs
Transmitted Length of Any Low-Power State Period	T_{LPX}	See Figure 12, Figure 13, Figure 14	50			ns
Time that the Transmitter Drives the Skew-Calibration Sync Pattern, 0xFFFF	$T_{SKEWCAL\_SYNC}$	See Figure 14		16		UI
Time that the Transmitter Drives the Skew-Calibration Pattern in the Initial Skew-Calibration Mode	$T_{SKEWCAL}$	See Figure 14			100	µs
		See Figure 14	2^{15}			UI
Time that the Transmitter Drives the Skew-Calibration Pattern in the Periodic Skew-Calibration Mode	$T_{SKEWCAL}$	See Figure 14			10	µs
		See Figure 14	2^{10}			UI
I²C/UART PORT TIMING						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO}	20 x V_{DDIO}/ 5.5V		150	ns
I²C/UART Wake Time	t_{WAKEUP}	From power-up, or rising edge of PWDNB to local register access; for remote register access, I²C/UART wake time is the same as lock time (t_{LOCK})		2.25		ms
I²C TIMING (SEE FIGURE 16)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range	9.6		100	kHz
		Mid f_{SCL} range	100		400	
		High f_{SCL} range	400		1000	

AC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B	(Note 2)			100	pF

AC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GMSL2 SPI MASTER (See Figure 17) (Note 6)						
Operating Frequency	f_{MCK}	(Note 2)	0.588		50	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}	(Note 2)	$t_{MCK}/2 - 3$	$t_{MCK}/2$		ns
MOSI Output Valid Time	t_{MOV}	After SCLK falling edge (Note 2)	2.3		$t_{MCK} - 2.3$	ns
MISO Input Setup Time	t_{MIS}	Before programmed sampling edge	13.5			ns
MISO Input Hold Time	t_{MIH}	After programmed sampling edge	-2			ns
GMSL2 SPI SLAVE (See Figure 18) (Note 6)						
Operating Frequency	f_{SCK}	(Note 2)			50	MHz
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns
MISO Output Valid Time	t_{SOV}	After SCLK falling edge (Note 2)	11.3		$t_{SCK} - 1.5$	ns
MOSI Input Setup Time	t_{SIS}	Before SCLK rising edge	5			ns
MOSI Input Hold Time	t_{SIH}	After SCLK rising edge	3			ns
REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1, X2) (Note 2)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
REFERENCE CLOCK REQUIREMENTS (EXTERNAL CLOCK INPUT ON X1, X2 FLOATING) (Note 2)						
Frequency	f_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
Input Jitter		6Gbps/187.5Mbps, sinusoidal jitter < 1MHz (falling edge), upstream serializer using crystal reference			600	ps p-p
Input Duty Cycle	T_{DUTY}		40		60	%
Input Fall Time	t_F	80% to 20%			4	ns

AC Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = 25°C, unless otherwise noted.) (Note 1)

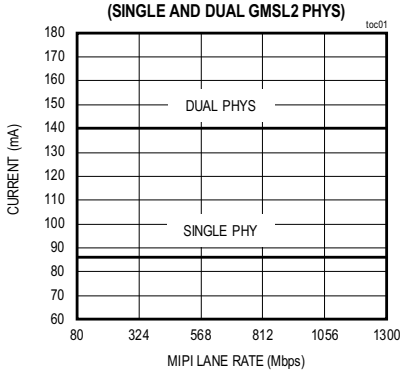
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
SIO__	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, Coax Configuration		±6		
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, STP Configuration		±4		
		ISO10605, R_D = 330Ω, C_S = 150pF, Air Discharge		±6		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Note 1: Limits are 100% tested at T_A = +105°C unless otherwise noted. Limits within the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 2: Not production tested. Guaranteed by design and characterization.
Note 3: C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of Tx and Rx are assumed to always be < 10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
Note 4: Color bar pattern. Maximum supply currents are measured at indicated supply voltages. Typical supply currents are measured at typical supply voltages.
Note 5: Additional 60pF at Rx termination center tap.
Note 6: Measured at 50MHz. See Table 5 for pin-programming recommendations.

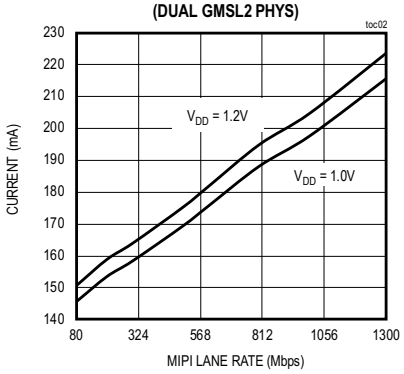
Typical Operating Characteristics

(V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. 6Gbps forward rate, 187.5Mbps reverse rate, PRBS24 data, single GMSL2 PHY configuration: SIOA or SIOB GMSL2 input enabled, data output on 4-lane Port A and replicated on 4-lane Port B, dual GMSL2 PHY configuration: SIOA and SIOB GMSL2 inputs enabled, SIOA data output on 4-lane Port A, SIOB data output on 4-lane Port B.)

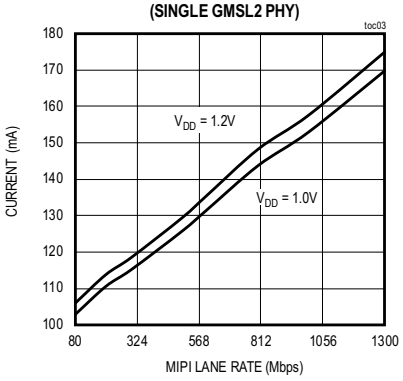
V_{DD18} CURRENT vs. MIPI DATA (SINGLE AND DUAL GMSL2 PHYS)



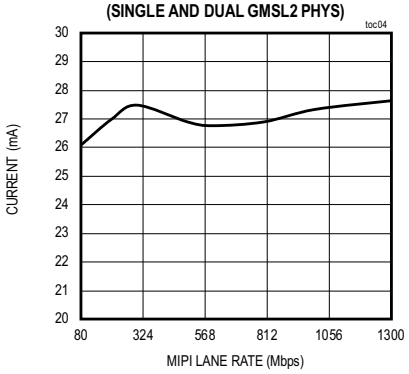
V_{DD} CURRENT vs. MIPI DATA (DUAL GMSL2 PHYS)



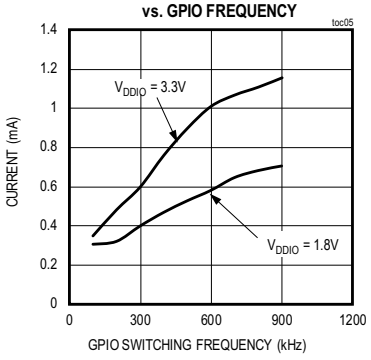
V_{DD} CURRENT vs. MIPI DATA (SINGLE GMSL2 PHY)



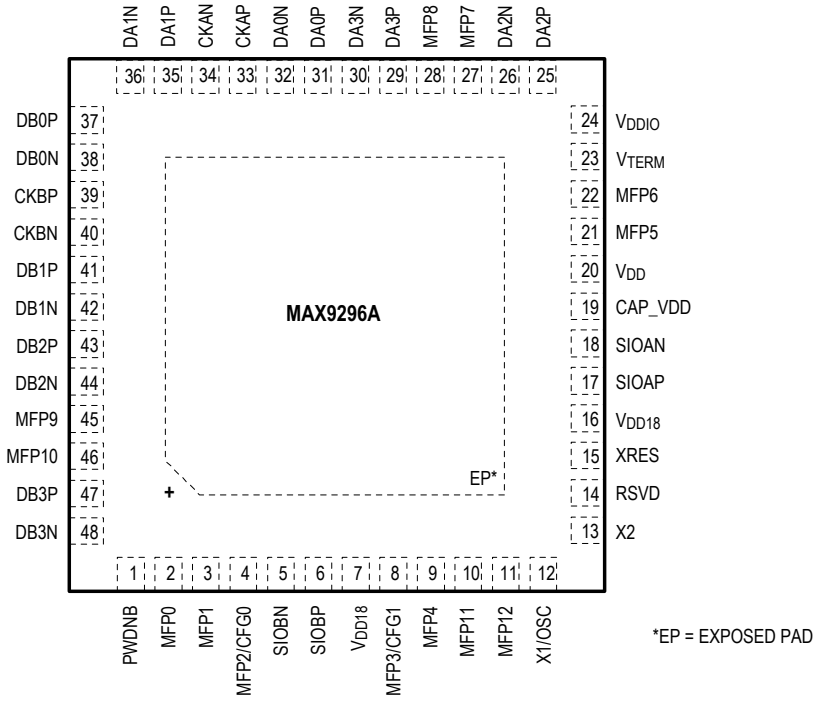
V_{TERM} CURRENT vs. MIPI DATA (SINGLE AND DUAL GMSL2 PHYS)



V_{DDIO} CURRENT vs. GPIO FREQUENCY



Pin Configuration



Pin Description

PIN NUMBER	PIN NAME	FUNCTION MODES		DESCRIPTION
		GMSL2	GMSL1	
SERIAL I/O				
5	SIOBN	SIOBN	SIOBN	Inverted Twisted-Pair Serial-Data Input/Output B
6	SIOBP	SIOBP	SIOBP	Noninverted Coax/Twisted-Pair Serial-Data Input/Output B
17	SIOAP	SIOAP	SIOAP	Noninverted Coax/Twisted-Pair Serial-Data Input/Output A
18	SIOAN	SIOAN	SIOAN	Inverted Twisted-Pair Serial-Data Input/Output A
CSI-2 PORTS				
25	DA2P	DA2P	DA2P	CSI-2 Port A Data Lane 2 Noninverted Output
26	DA2N	DA2N	DA2N	CSI-2 Port A Data Lane 2 Inverted Output
29	DA3P	DA3P	DA3P	CSI-2 Port A Data Lane 3 NonInverted Output
30	DA3N	DA3N	DA3N	CSI-2 Port A Data Lane 3 Inverted Output
31	DA0P	DA0P	DA0P	CSI-2 Port A Data Lane 0 Noninverted Output
32	DA0N	DA0N	DA0N	CSI-2 Port A Data Lane 0 Inverted Data Output
33	CKAP	CKAP	CKAP	CSI-2 Port A Clock Lane Noninverted Output
34	CKAN	CKAN	CKAN	CSI-2 Port A Clock Lane Inverted Output
35	DA1P	DA1P	DA1P	CSI-2 Port A Data Lane 1 Noninverted Output

Pin Description (continued)

PIN NUMBER	PIN NAME	FUNCTION MODES		DESCRIPTION
		GMSL2	GMSL1	
36	DA1N	DA1N	DA1N	CSI-2 Port A Data Lane 1 Inverted Output
37	DB0P	DB0P	DB0P	CSI-2 Port B Data Lane 0 Noninverted Output
38	DB0N	DB0N	DB0N	CSI-2 Port B Data Lane 0 Inverted Output
39	CKBP	CKBP	CKBP	CSI-2 Port B Clock Lane Noninverted Output
40	CKBN	CKBN	CKBN	CSI-2 Port B Clock Lane Inverted Output
41	DB1P	DB1P	DB1P	CSI-2 Port B Data Lane 1 Noninverted Output
42	DB1N	DB1N	DB1N	CSI-2 Port B Data Lane 1 Inverted Output
43	DB2P	DB2P	DB2P	CSI-2 Port B Data Lane 2 Noninverted Output
44	DB2N	DB2N	DB2N	CSI-2 Port B Data Lane 2 Inverted Output
47	DB3P	DB3P	DB3P	CSI-2 Port B Data Lane 3 Noninverted Output
48	DB3N	DB3N	DB3N	CSI-2 Port B Data Lane 3 Inverted Output
MULTIFUNCTION PINS (*DEFAULT STATE AFTER POWER-UP) (INPUT READ OR OUTPUT WRITE BY REGISTER PROGRAMMING ONLY)**				
2	MFP0	SDA1 RX1 SDA2 RX2 FRSYNC_OUT VS2 DE2/DV2 SCLK MS GPIO0*	FRSYNC_OUT CNTL1 MS GPIO0*(**)	SDA1: Pass-Through I^2C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. RX1: Pass-Through UART Input with an Internal 40kΩ Pullup to V_{DDIO}. SDA2: Pass-Through I^2C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. RX2: Pass-Through UART Input with an Internal 40kΩ Pullup to V_{DDIO}. FRSYNC_OUT: Frame Sync Push-Pull Output. VS2: Video Stream Vertical Sync Monitor Push-Pull Output. DE2/DV2: Video Stream Data Enable or Data Valid Monitor Push-Pull Output. SCLK: SPI Clock. When configured as master, push-pull clock output. When configured as a slave, clock input with internal 1MΩ pulldown to ground. MS: UART Mode Select with Internal 1MΩ Pulldown to Ground. Set MS low to select base mode. Set MS high to select bypass mode. MS state can also be temporarily overwritten by a register write. GPIO0: Configurable General-Purpose Input or Output. Power-up default is GPI0 general-purpose inputwith a 1MΩ pulldown to ground. CNTL1: Control 1 Push-Pull Output.

Pin Description (continued)

PIN NUMBER	PIN NAME	FUNCTION MODES		DESCRIPTION
		GMSL2	GMSL1	
3	MFP1	SCL1 TX1 SCL2 TX2 LOCK* GPIO1	FRSYNC_IN LOCK* GPIO1**	SCL1: Pass-Through I²C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. TX1: Pass-Through UART Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. SCL2: Pass-Through I²C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. TX2: Pass-Through UART Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. LOCK: Open-Drain Lock Indication Output with an Internal 40kΩ Pullup to V_{DDIO}. GPIO1: Configurable General-Purpose Input or Output. FRSYNC_IN: Frame Sync Input with an Internal 1MΩ Pulldown to Ground.
4	MFP2/ CFG0	CFG0 BNE SS1 GPO2*	CFG0 CNTL0 GPO2*(**)	CFG0: Configuration Pin. Voltage at Pin Sets Device Mode, Which is Latched at Power-Up. Connect to a resistor-divider between V_{DDIO} and ground. See Table 10. BNE: When Configured as Slave, SPI Buffer Not Empty Push-Pull Output. When BNE is high, SPI data is available. SS1: SPI Slave Select. When configured as the master, Slave 1 Select Push-Pull Output. GPO2: General-Purpose Push-Pull Output. Power-up default is high impedance. CNTL0: Control 0 Push-Pull Output.
8	MFP3/ CFG1	CFG1 VS1 DE1/DV1 SS2 GPO3*	CFG1 CNTL3 GPO3*(**)	CFG1: Configuration Pin. Voltage at the pin sets device mode, which is latched at power-up. Connect to a resistor-divider between V_{DDIO} and ground. See Table 11. VS1: Video Stream Vertical Sync Monitor Push-Pull Output. DE1/DV1: Video Stream Data Enable or Data Valid Monitor Push-Pull Output. SS2: SPI Slave Select. When configured as the master, Slave 2 Select push-pull output. GPO3: General-Purpose Push-Pull Output. Power-up default is high impedance. CNTL3: Control 3 Push-Pull Output.
9	MFP4	RO(Alt) ERRB* GPIO4	ERRB* GPIO4**	RO(Alt): When Configured as a Slave, SPI Mode-Select Input with an Internal 1MΩ Pulldown to Ground. When RO is high, enables a master read from MISO. When RO is low, enables a master write to MOSI. ERRB: Open-Drain Error Indication Output with an Internal 40kΩ Pullup to V_{DDIO}. When ERRB is low, a data error, line fault or interrupt is detected. ERRB is high when PWDNB is low. GPIO4: Configurable General-Purpose Input or Output.

Pin Description (continued)

PIN NUMBER	PIN NAME	FUNCTION MODES		DESCRIPTION
		GMSL2	GMSL1	
21	MFP5	SDA2 RX2 SDA1 RX1* MOSI GPIO5	CNTL2 GPI_1 GPIO5*(**)	SDA2: Pass-Through I²C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. RX2: Pass-Through UART Input with an Internal 40kΩ Pullup to V_{DDIO}. SDA1: Pass-Through I²C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. RX1: Pass-Through UART Input with an Internal 40kΩ Pullup to V_{DDIO} (Default 1Mbps Rate). MOSI: SPI Master Out Slave In. When configured as the master, the push-pull output drives data to the external slave. When configured as a slave, input with an internal 1MΩ pulldown to ground that receives data from external master. GPIO5: Configurable General-Purpose Input or Output. Power-up default with a receiver enabled and open-drain driver high with an internal 40kΩ pullup to V_{DDIO}. CNTL2: Control 2 Push-Pull Output. GPI_1: General-Purpose Input with an Internal 40kΩ Pullup to V_{DDIO}.
22	MFP6	SCL2 TX2 SCL1 TX1* MISO GPIO6	FRSYNC_IN CNTL4 GPI_0 GPIO6*(**)	SCL2: Pass-Through I²C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. TX2: Pass-Through UART Output with an Internal 40kΩ Pullup to V_{DDIO}. SCL1: Pass-Through I²C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}. TX1: Pass-Through UART Output with an Internal 40kΩ Pullup to V_{DDIO} (Default 1Mbps Rate). MISO: SPI Master In Slave Out. When configured as a master, input with an internal 1MΩ pulldown to ground that receives data from the external slave. When configured as a slave, push-pull output that drives data to an external master. GPIO6: Configurable General-Purpose Input or Output. Power-up default with the receiver enabled and open-drain driver high with internal 40kΩ pullup to V_{DDIO}. FRSYNC_IN: Frame Sync Input with an Internal 1MΩ Pulldown to Ground. CNTL4: Control 4 Push-Pull Output. GPI_0: General-Purpose Input with an Internal 40kΩ Pullup to V_{DDIO}.
27	MFP7	RO LMN0 GPI7*	LMN0 GPI7*(**)	RO: When Configured as Slave, SPI Mode-Select Input with an Internal 1MΩ Pulldown to Ground. When RO is high, enables a master read from MISO. When RO is low, enables a master write to MOSI. LMN0: Line Fault Monitor Input. GPI7: General-Purpose Input with a 1MΩ Pulldown to Ground.
28	MFP8	LMN1 GPI8*	LMN1 GPI8*(**)	LMN1: Line Fault Monitor Input. GPI8: General-Purpose Input with a 1MΩ Pulldown to Ground.
45	MFP9	LMN2 GPI9*	LMN2 GPI9*(**)	LMN2: Line Fault Monitor Input. GPI9: General-Purpose Input with 1MΩ Pulldown to Ground.

Pin Description (continued)

PIN NUMBER	PIN NAME	FUNCTION MODES		DESCRIPTION
		GMSL2	GMSL1	
46	MFP10	LMN3 GPI10*	LMN3 GPI10*(**)	LMN3: Line Fault Monitor Input. GPI10: General-Purpose Input with a 1MΩ Pulldown to Ground.
10	MFP11	SDA Rx GPI11_ODO11	SDA RX GPI11_ ODO11**	SDA: I²C Data Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO} (SDA or RX Selected by CFG0 at Power-Up). Rx: UART Input with Internal 40kΩ Pullup to V_{DDIO} (SDA or Rx Selected by CFG0 at Power-Up). GPI11_ODO11: General-Purpose Input and/or Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO}.
11	MFP12	SCL Tx GPI12_ODO12	SCL TX GPI12_ ODO12**	SCL: I²C Clock Input/Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO} (SCL or Tx Selected by CFG0 at Power-Up). Tx: UART Open-Drain Output with an Internal 40kΩ Pullup to V_{DDIO} (SCL or Tx Selected by CFG0 at Power-Up). GPI12_ODO12: General-Purpose Input and/or Open-Drain Output with Internal 40kΩ Pullup to V_{DDIO}.
MISCELLANEOUS - REFER TO EXTERNAL COMPONENTS REQUIREMENTS TABLE				
1	PWDNB	PWDNB	PWDNB	Active-Low, Power-Down Input with an Internal 1MΩ Pulldown to Ground. Set PWDNB Low to Enter Power-Down Mode.
12	X1/OSC	X1/OSC	X1/OSC	Crystal/Oscillator Input. Connect to either a 25MHz Crystal or 25MHz External Clock Source. Required in both GMSL2 and GMSL1 Modes.
13	X2	X2	X2	Crystal Input. Connect to One Terminal of a 25MHz Crystal and Connect a Load Capacitor from X1/OSC to Ground (Load Capacitor Value Depends on Crystal Used). Applies in both GMSL2 and GMSL1 Modes.
14	RSVD	RSVD	RSVD	Reserved. Make no electrical connection to this pin.
15	XRES	XRES	XRES	Used to Calibrate SIO Output Driver Swings. Connect an external 402Ω resistor between XRES and ground.
19	CAP_ VDD	CAP_VDD	CAP_VDD	Decoupling Capacitor for 1V Core Supply.
POWER SUPPLIES - REFER TO EXTERNAL COMPONENT REQUIREMENTS TABLE				
7	VDD18	VDD18	VDD18	1.8V Analog Supply.
16	VDD18	VDD18	VDD18	1.8V Analog Supply.
20	VDD	VDD	VDD	1.0V Core Supply. Connect a 0.95V to 1.05V supply, or connect a 1.14V to 1.26V supply to use the internal 1.0V regulator. In order to use the internal 1.0V regulator, first write REG_ENABLE = 1, then write REG_MNL = 1.
23	VTERM	VTERM	VTERM	1.2V D-PHY Termination Supply.
24	VDDIO	VDDIO	VDDIO	1.8V to 3.3V I/O Supply.
EP	EP	EP	EP	Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Block Diagram

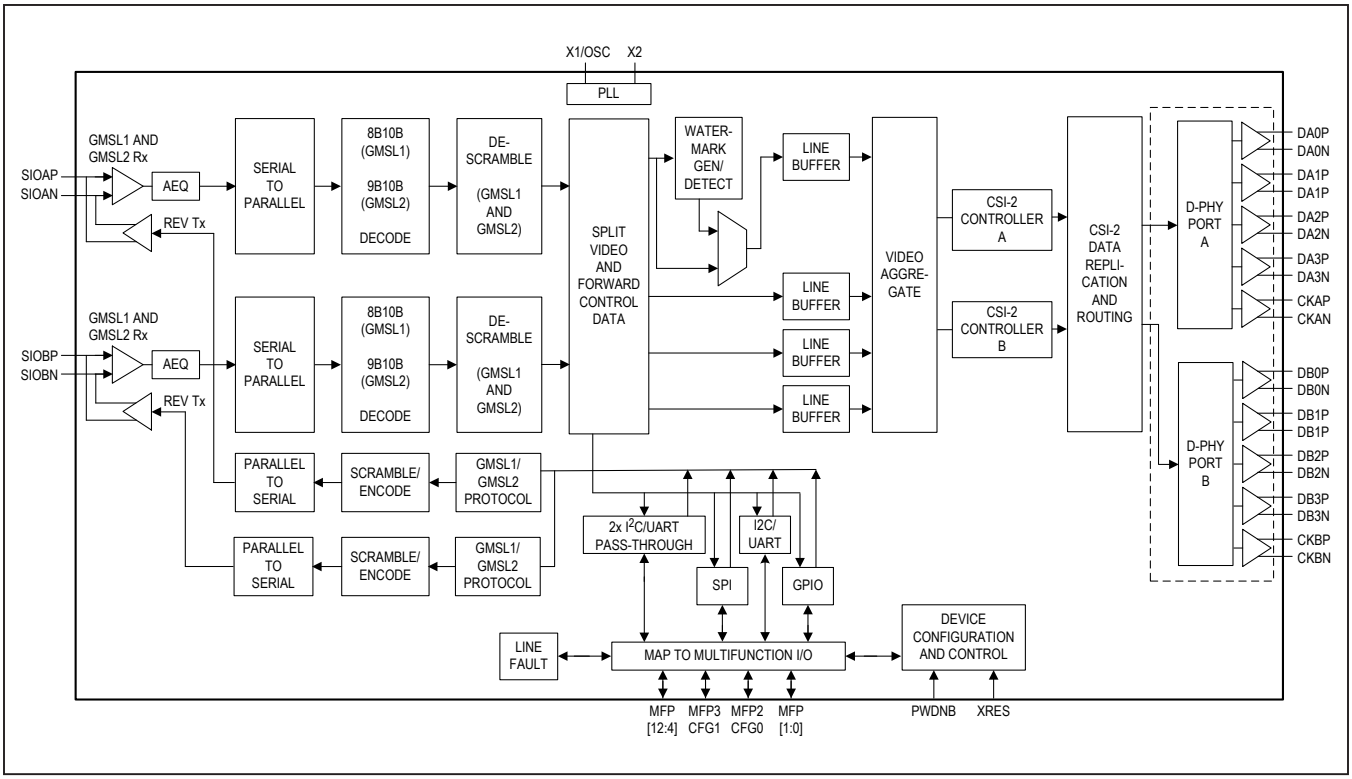


Table 1. Recommended Operating Conditions

PARAMETER	PIN NAME	NOMINAL VOLTAGE (V)	MIN	TYP	MAX	UNIT
Supply Range	V_{TERM}	—	1.14	1.2	1.26	V
	V_{DD18}	—	1.7	1.8	1.9	
	V_{DD}	1.0	0.95	1.0	1.05	
		1.2	1.14	1.2	1.26	
	V_{DDIO}	1.8	1.7	1.8	1.9	
		3.3	3.0	3.3	3.6	
Maximum Supply Noise*	V_{TERM}	—		50		mV_{P-P}
	V_{DD18}	—		25		
	V_{DD}	1.0		50		
		1.2		50		
	V_{DDIO}	1.8		50		
		3.3		100		
Operating Junction Temperature, T_J			-40		+125	°C

**Supply noise < 1MHz*

Table 2. External Component Requirements (Figure 25 and Figure 26)

COMPONENT	SYMBOL	CONDITION		VALUE	UNIT
XRES	R_{XRES}			402 ±1%, use a single resistor	Ω
Line Fault Pulldown Resistor	R_{PD}			49.9 ±1%	kΩ
Line Fault Series Resistor	R_{EXT}			48.7 ±1%	kΩ
Link Isolation Capacitors	C_{LINK}	Place close to the SIO_ pins (5, 6, 17, 18) used in the application.	GMSL2 Mode	0.1	µF
			GMSL1 Mode, HIM disabled	0.22	µF
			GMSL1 Mode, HIM enabled	0.047 to 0.22	µF
Crystal		Place as close as possible to pins 12 and 13.		25MHz ±200ppm	
Crystal Load Capacitors		Use crystal loading capacitor guidance from the crystal manufacturer. Select values that compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins 12 (X1/OSC) and pin 13 (X2).			
V_{DDIO} Decoupling Capacitor		Place a 0.01µF capacitor as close as possible to pin 24. Include a minimum of 10µF bulk decoupling on the PCB.			
V_{DD18} Decoupling Capacitors		Place a 0.01µF capacitors as close as possible to pins 7 and 16. Include a minimum of 10µF bulk decoupling on the PCB.			
V_{TERM} Decoupling Capacitor		Place a 0.01µF capacitor as close as possible to pin 23. Include a minimum of 10µF bulk decoupling on the PCB.			
V_{DD} Decoupling Capacitor		Place a 0.1µF capacitor as close as possible to pin 20. Include a minimum of 10µF bulk decoupling on the PCB.			
CAP_VDD Decoupling Capacitor		Place a 0.1µF capacitor as close as possible to pin 19. Include a minimum of 10µF bulk decoupling near the pin.			
Open-Drain Pullup Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations.			
Resistors for Configuration Pin Resistor Divider	R1, R2	Place resistor divider close to pin 4 (MFP2/CFG0).		Use ±1% tolerance resistors. See Table 10.	Ω
	R1, R2	Place resistor divider close to pin 8 (MFP3/CFG1).		Use ±1% tolerance resistors. See Table 11.	Ω

Functional Diagrams

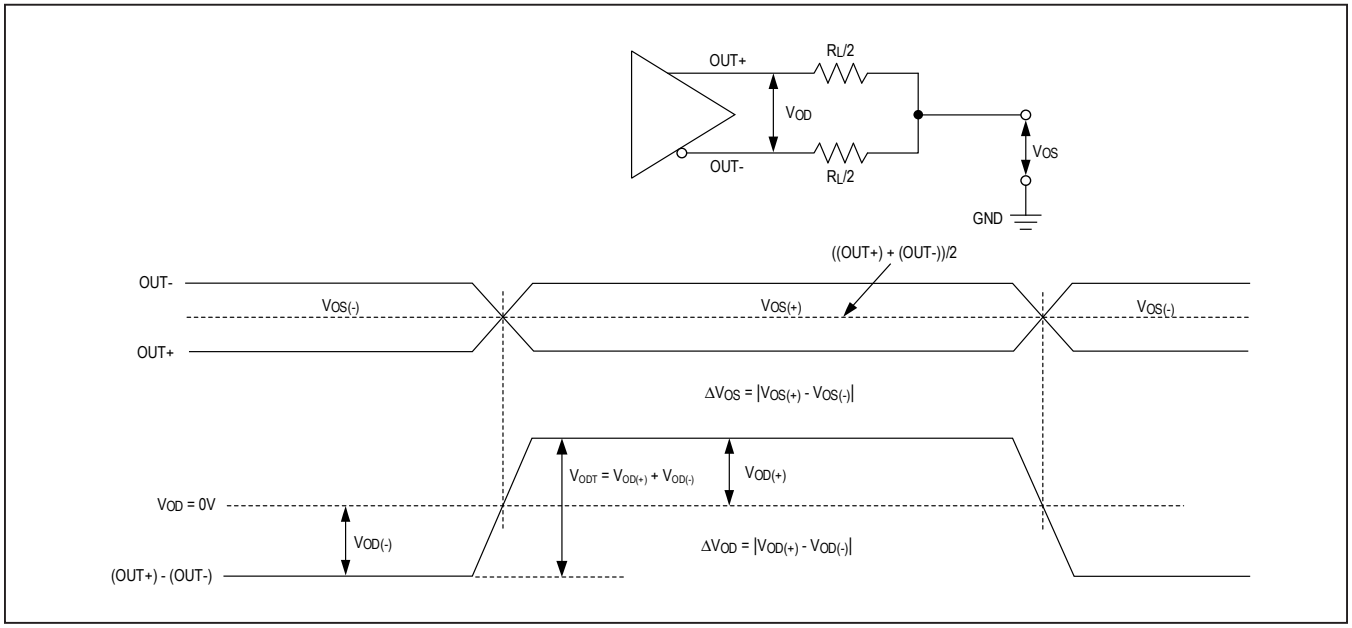


Figure 1. GMSL2 Reverse Channel Serial Outputs

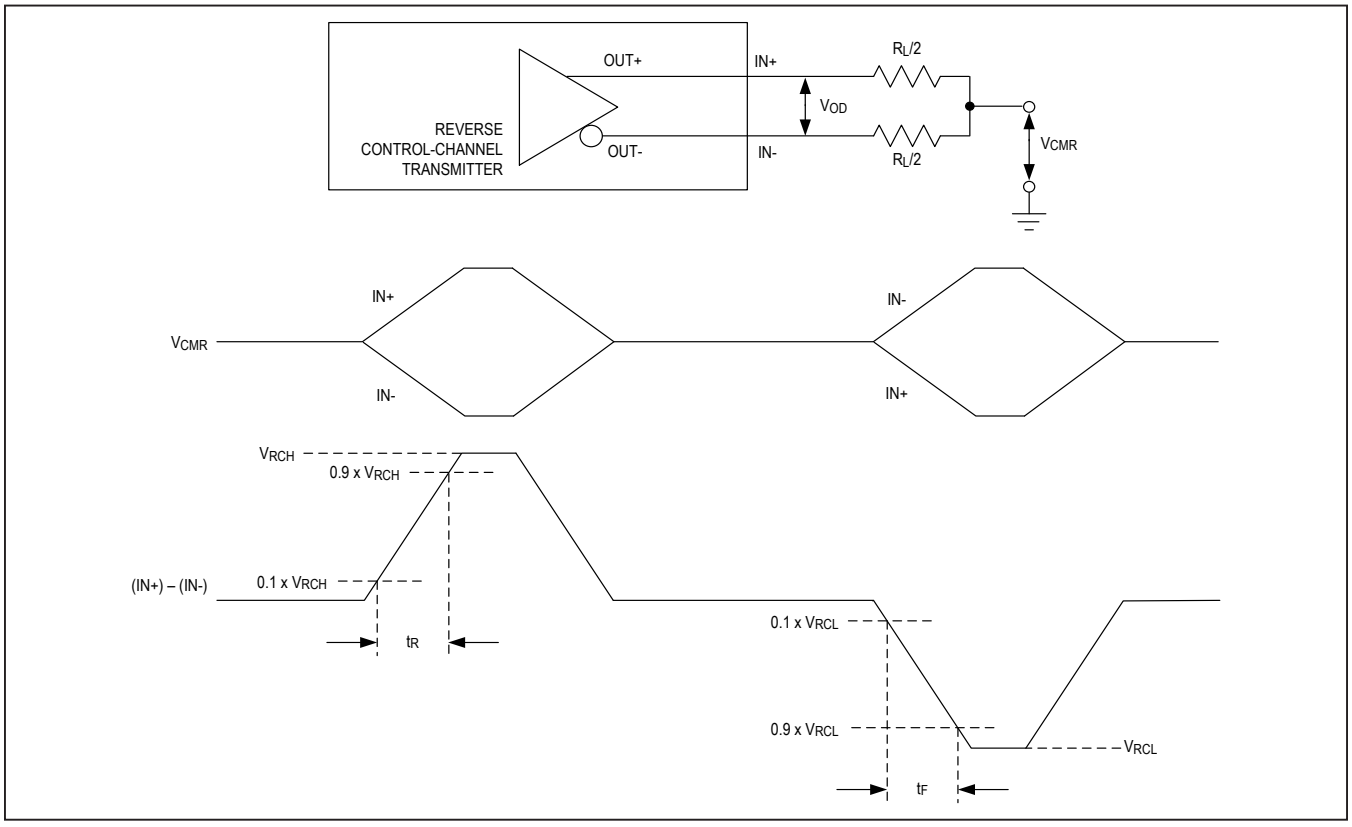


Figure 2. GMSL1 Reverse Channel Serial Outputs

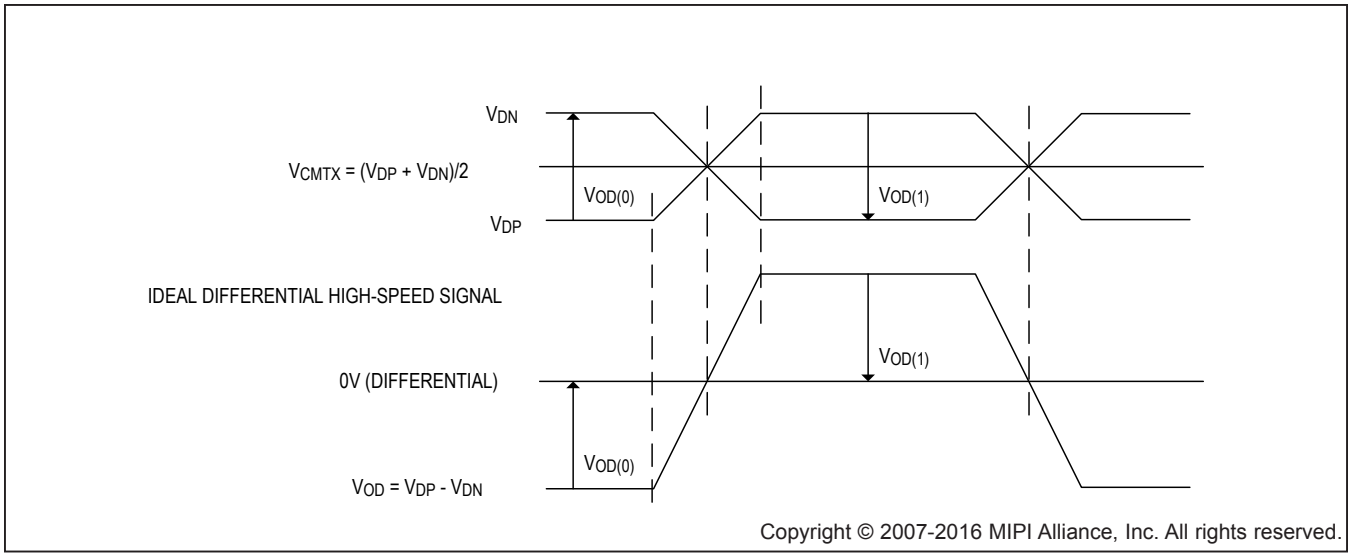


Figure 3. Ideal Single-ended and Resulting Differential HS Signals

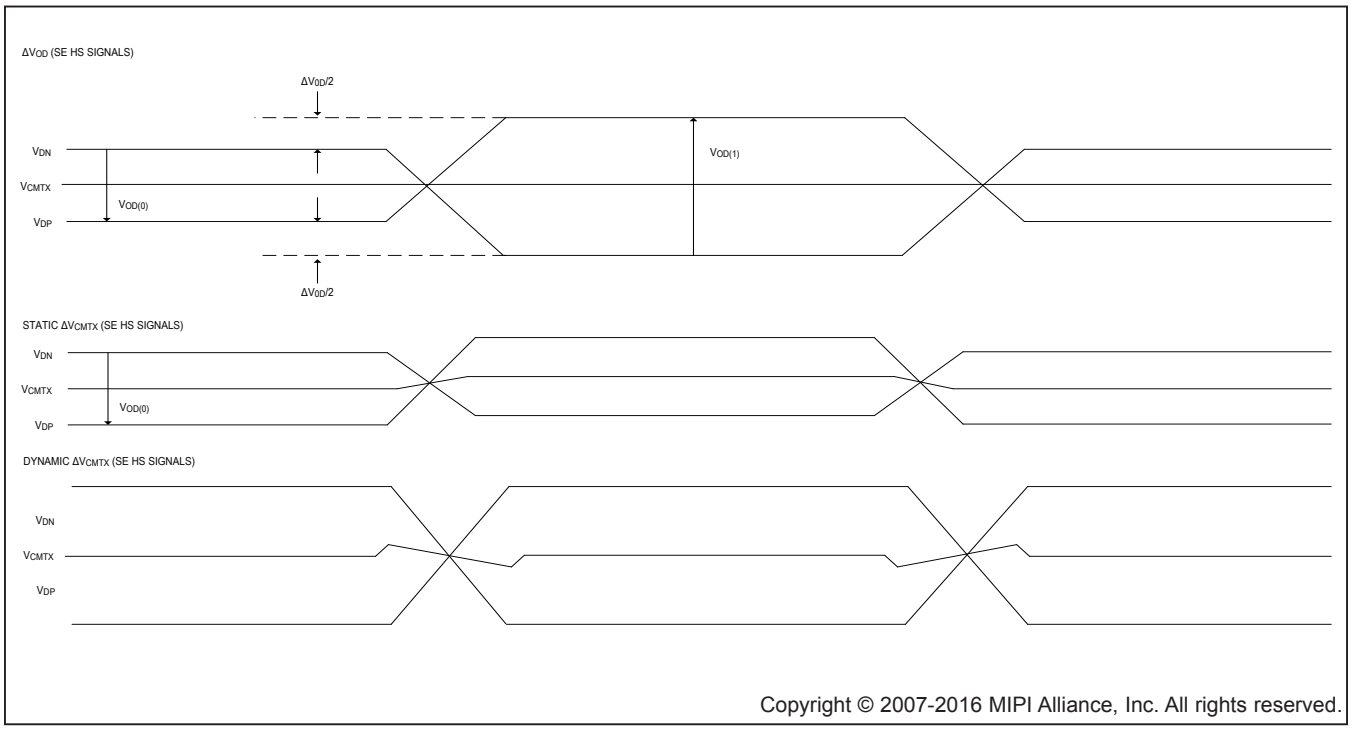


Figure 4. Possible Delta V_{CMTX} and Delta V_{OD} Distortions of Single-Ended HS Signals

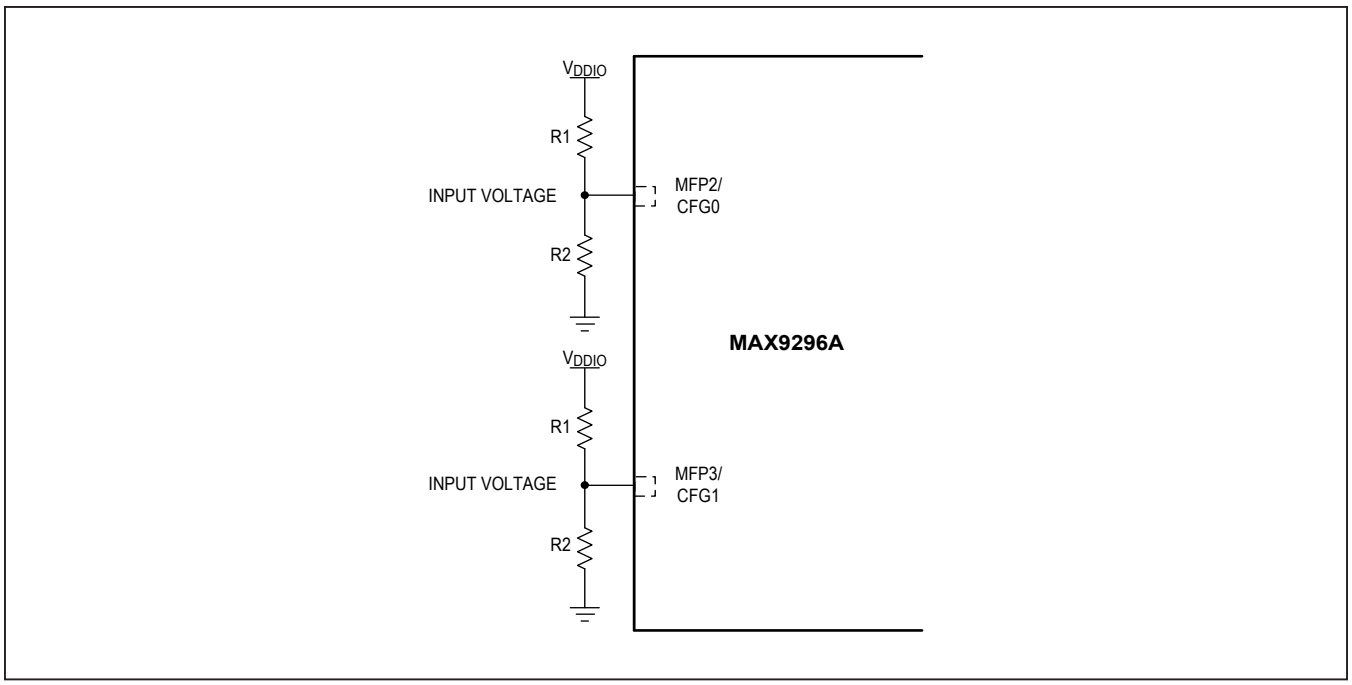


Figure 5. Configuration Pin Connection

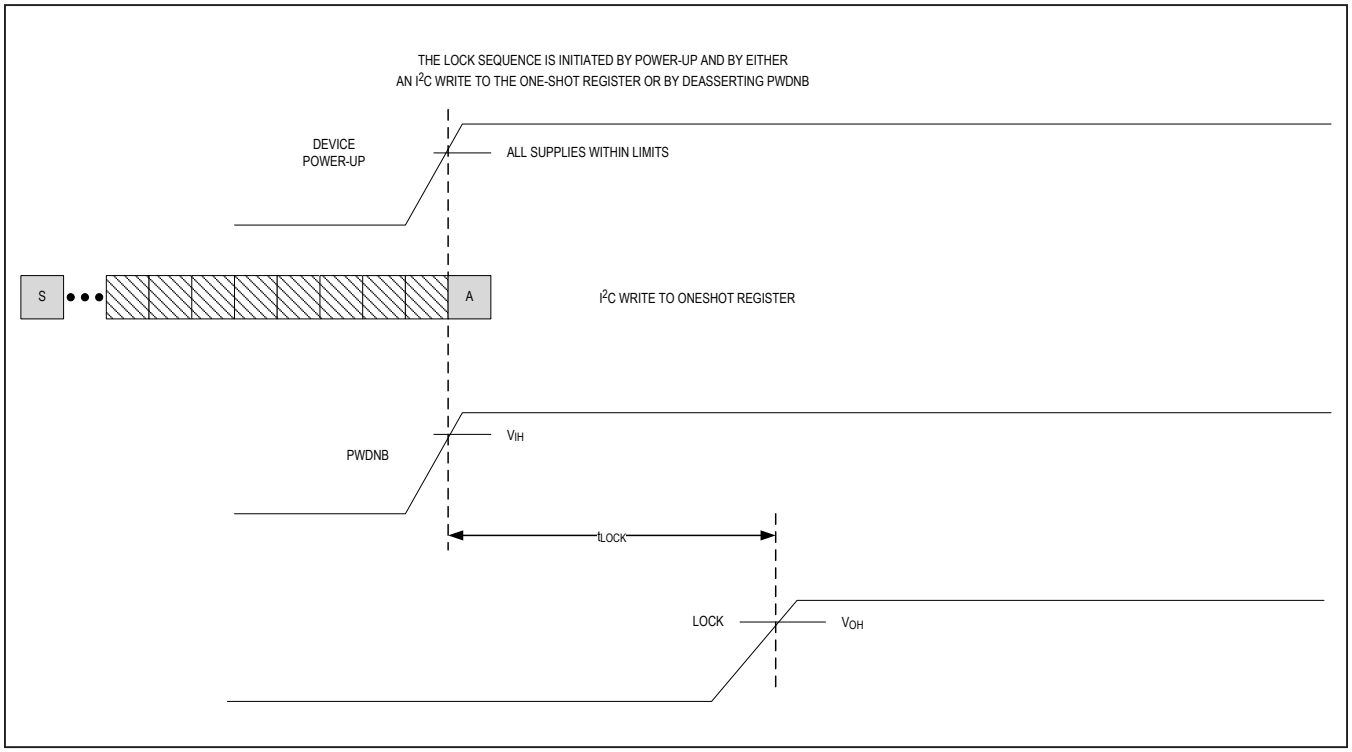


Figure 6. GMSL2 Lock Time

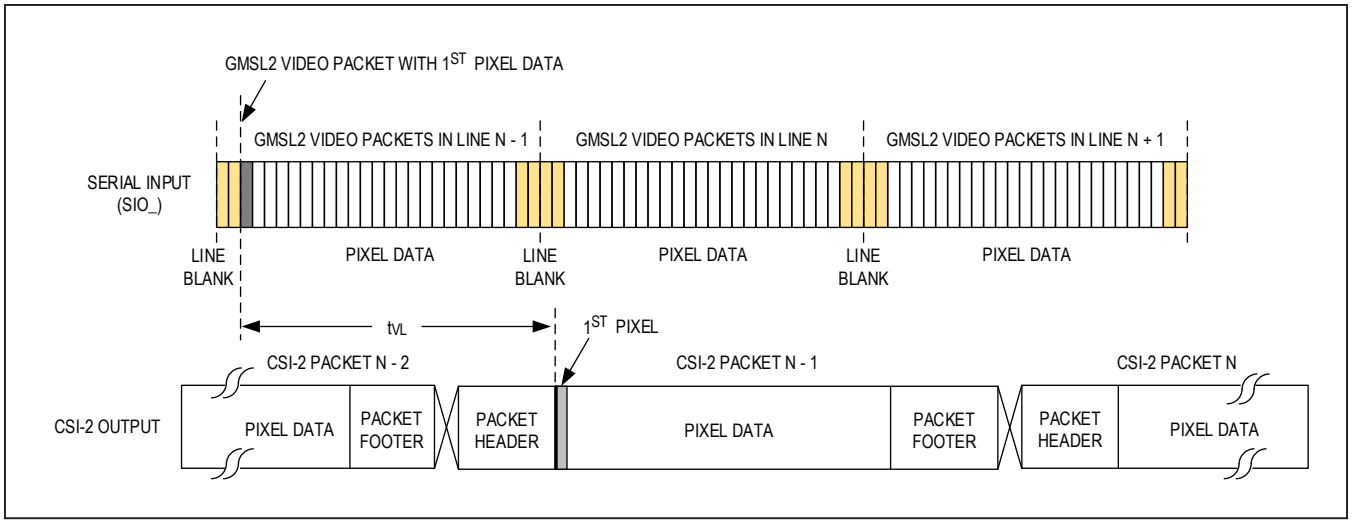


Figure 7. GMSL2 Video Latency

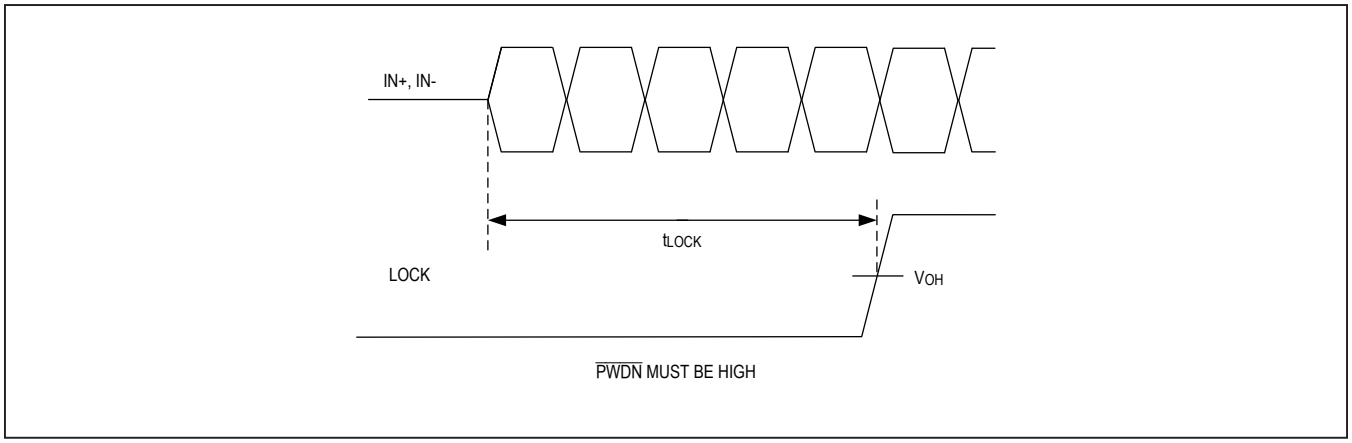


Figure 8. GMSL1 Lock Time

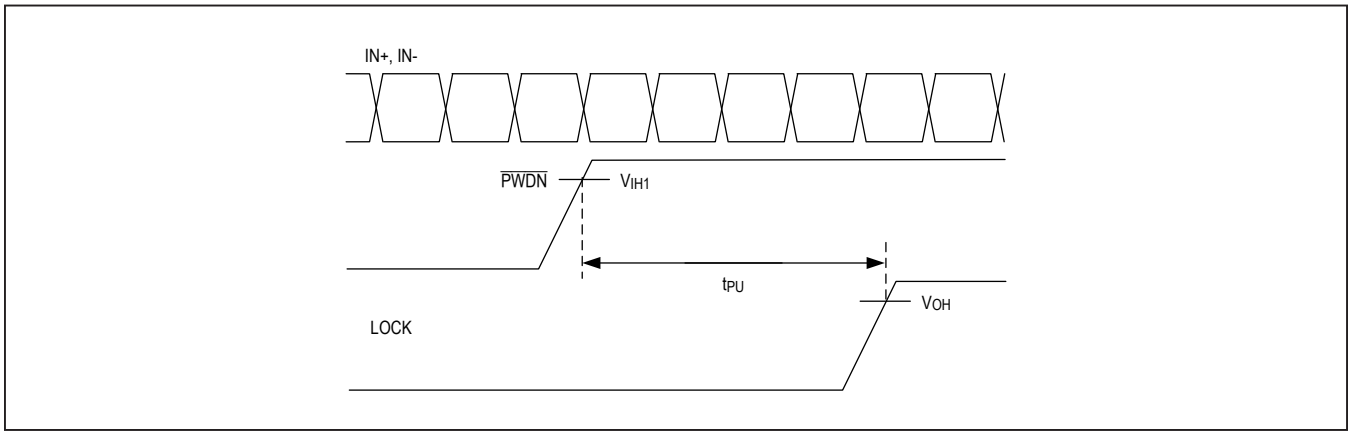


Figure 9. GMSL1 Power-Up Delay

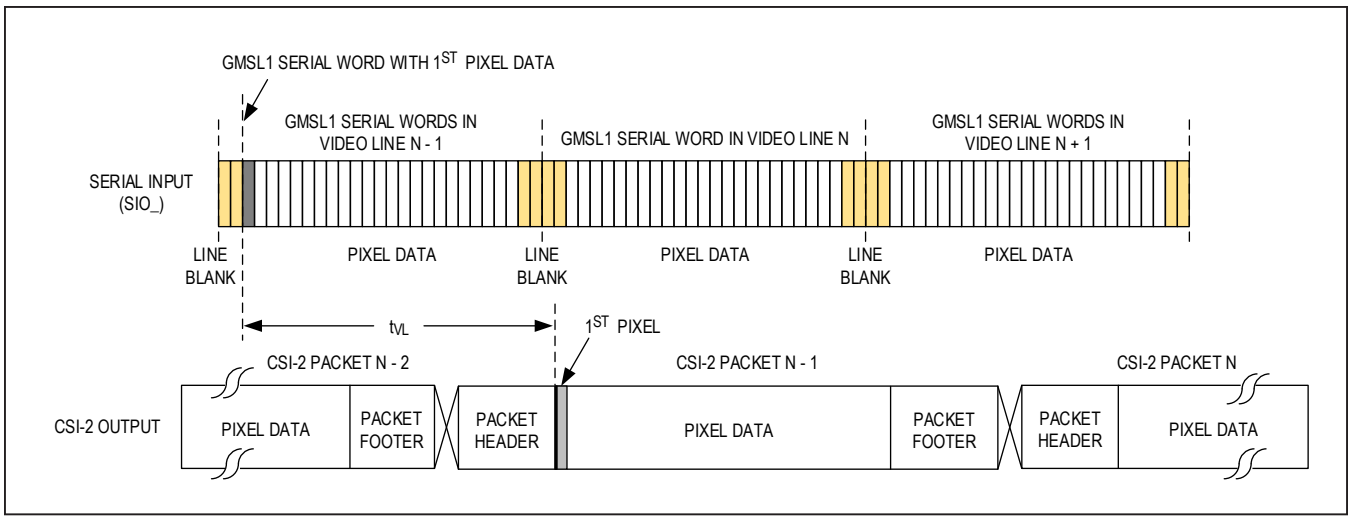


Figure 10. GMSL1 Video Latency

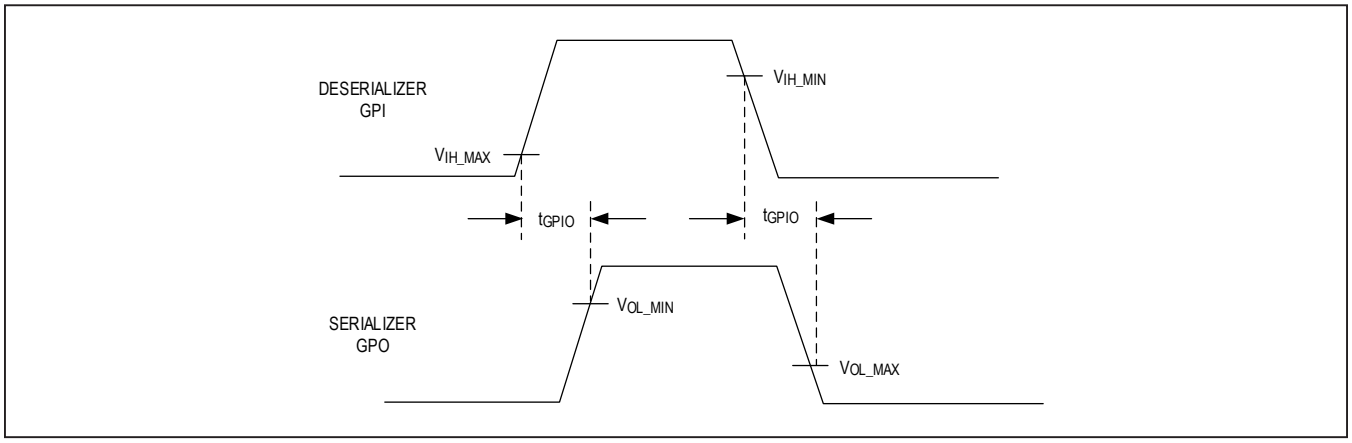


Figure 11. GSML1 GPI-to-GPO Delay

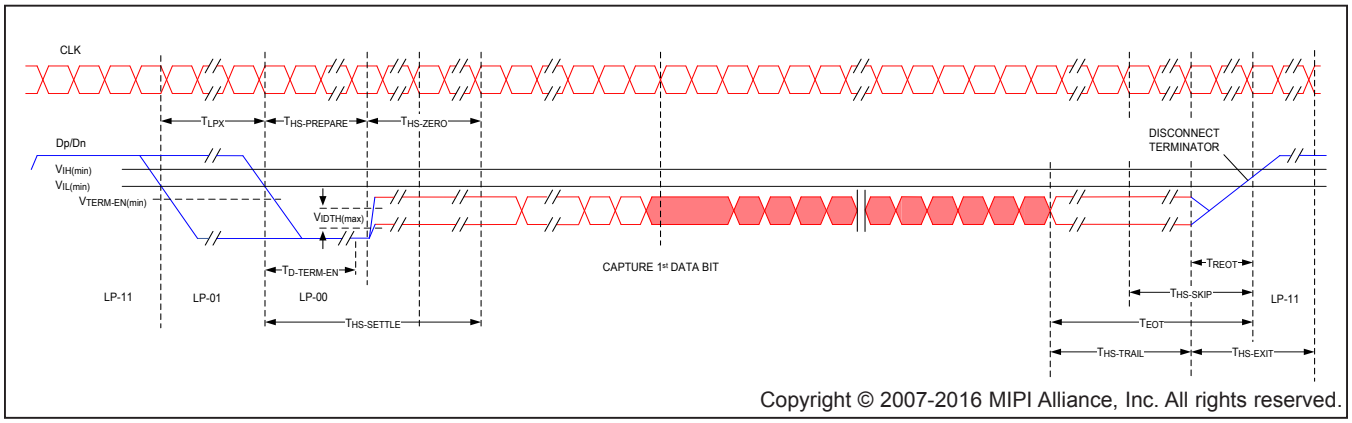


Figure 12. D-PHY Global Operation Timing (a)

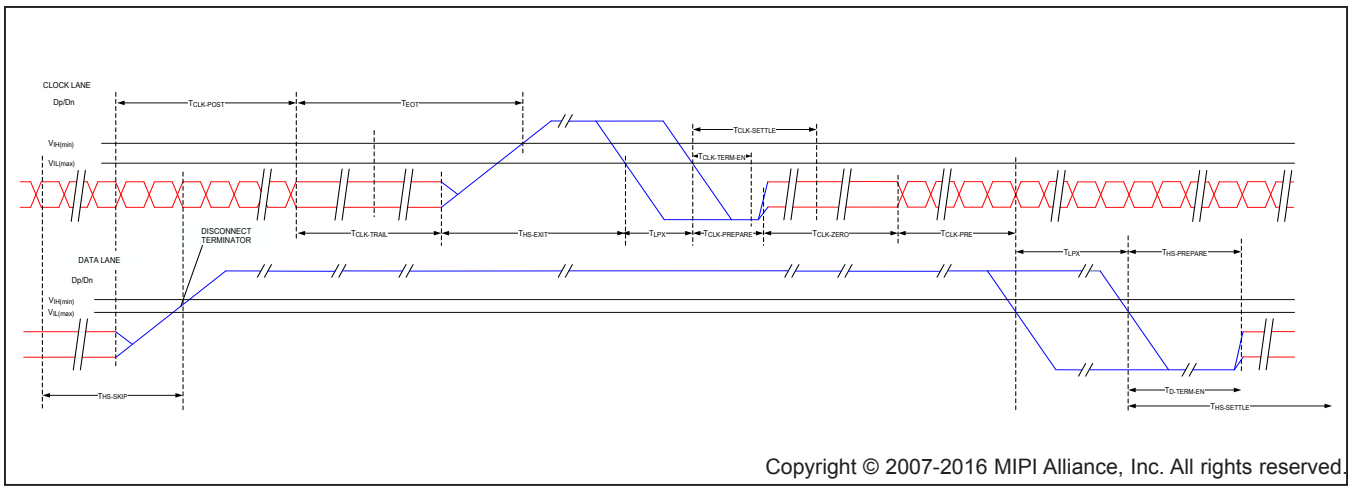


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Figure 13. D-PHY Global Operation Timing (b)

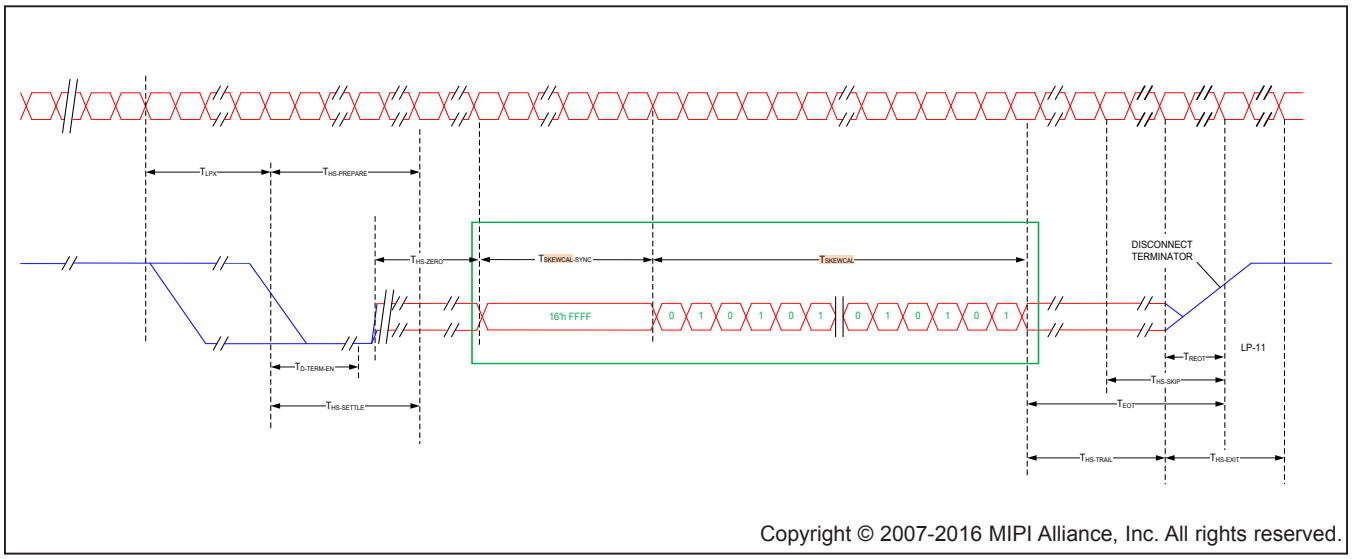

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Figure 14. D-PHY High-Speed Skew Calibration

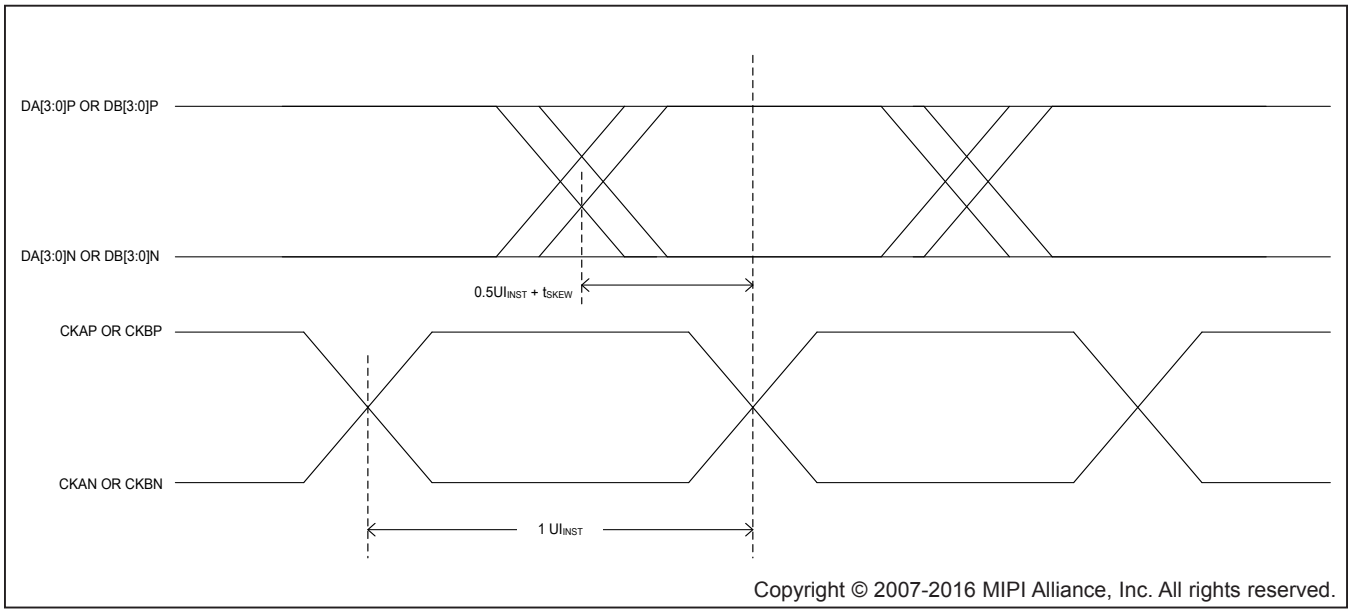

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Figure 15. D-PHY Data Clock Timing

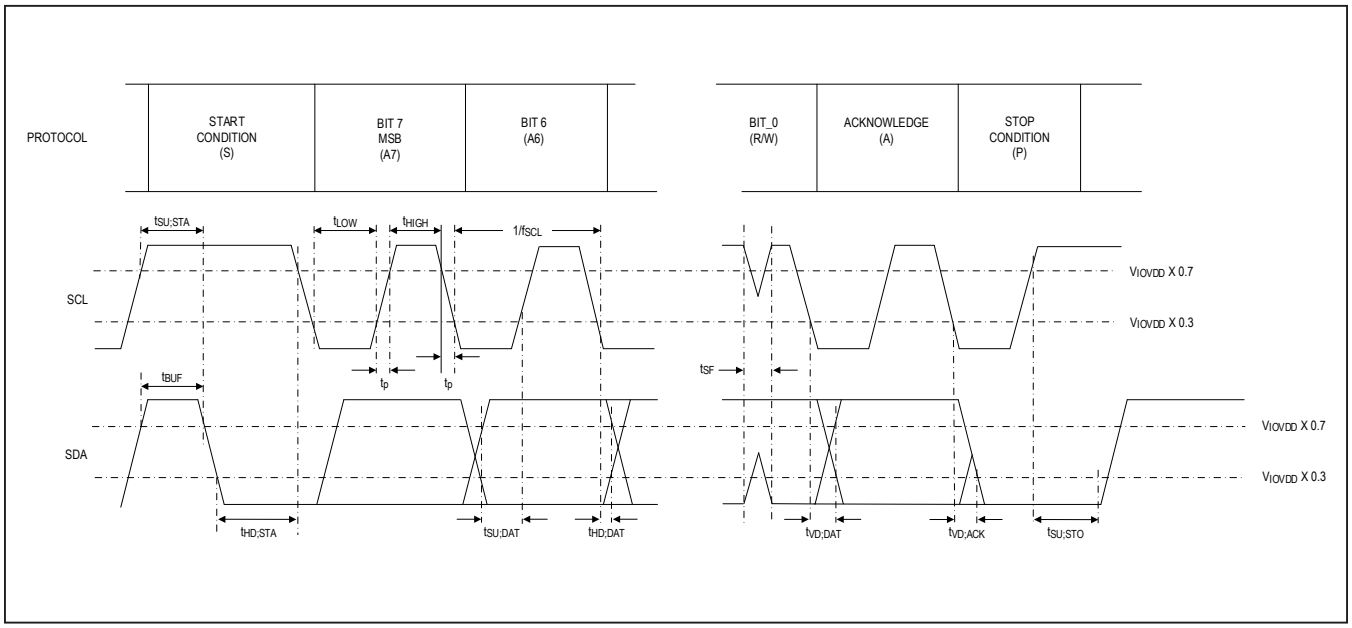

Figure 16. I²C Timing Parameters

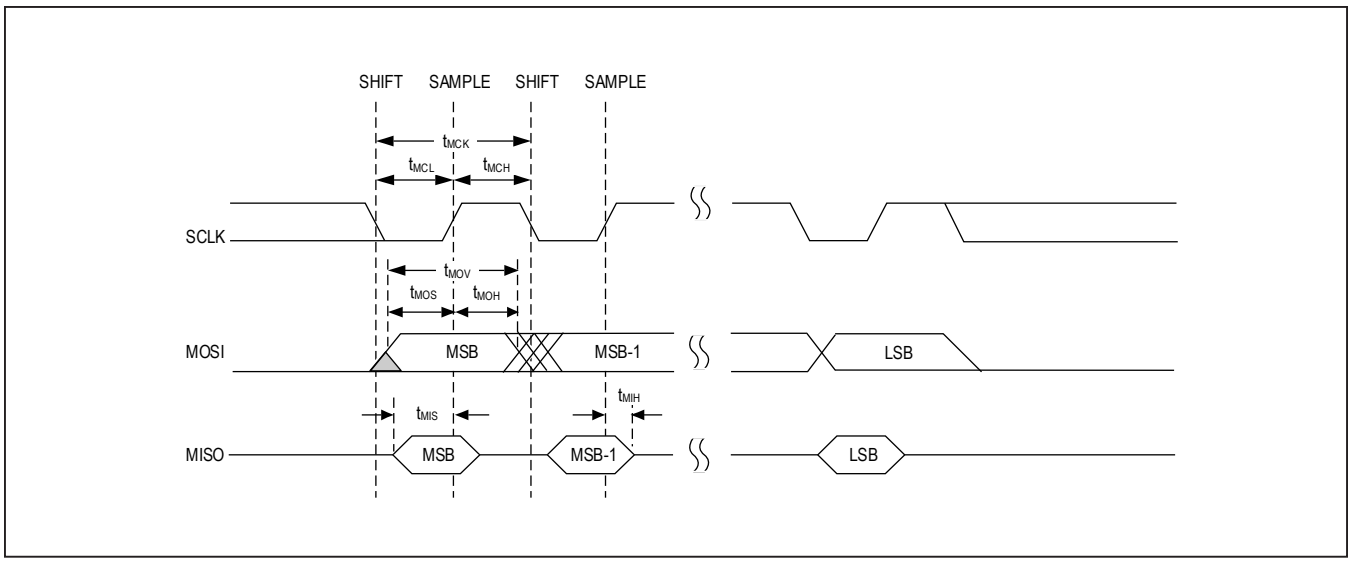

Figure 17. SPI Master-Mode Timing Parameters

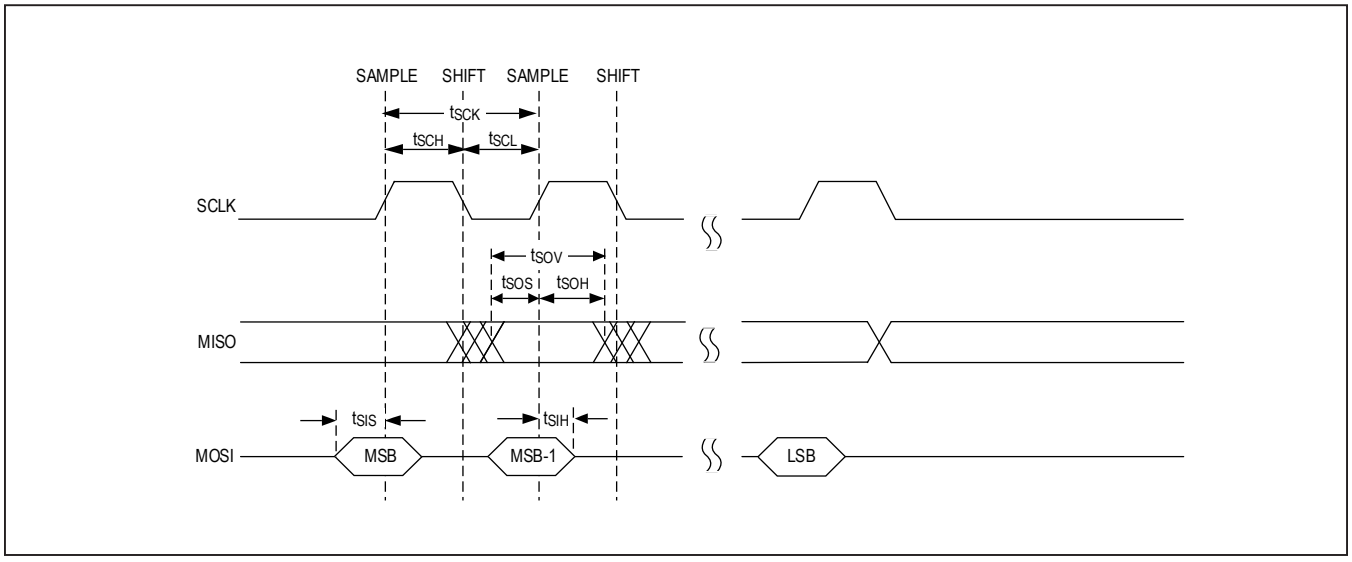

Figure 18. SPI Slave-Mode Timing Parameters

Detailed Description

Introduction

Maxim's GMSL2 serializers and deserializers provide sophisticated link management for high-speed, low bit-error-rate, serial data transport. They support a comprehensive suite of display, camera, and communication interfaces over a single wire.

GMSL2 devices for display applications provide up to 6Gbps forward and 1.5Gbps reverse packetized data transmission over each fixed-speed link. GMSL2 devices for camera, radar, and lidar applications provide a reverse channel rate of 187.5Mbps. Most devices with two GMSL2 links provide a total capacity of 12Gbps and 3Gbps reverse in specific configurations.

The following sections provide a brief overview of the device functions and features. Contact factory for additional information and details on the configuration of each function and feature.

Product Overview

The MAX9296A converts data on single or dual GMSL2/GMSL1 serial inputs to CSI-2 packets on one or two CSI-2 output ports.

Data from the serial inputs can be aggregated and output on a single CSI-2 port, replicated on a second port, or output on either port.

The dual-link mode functions logically as a single link, but doubles the forward channel bandwidth by using two serial links.

The MAX9296A pairs with any GMSL2 or GMSL1 serializer.

Figure 19 shows a single serial link transporting video data for capture by an SoC. The forward channel operates at a fixed 3Gbps or 6Gbps rate. The reverse channel operates at a fixed 187.5Mbps rate. Idle packets are substituted to fill any unused link bandwidth in both forward and reverse channels.

Forward- and reverse-channel bandwidth can be allocated in any proportion to video or control data. For this link, and the following examples, the maximum payload data rate in the forward direction for a single link is approximately 5.2Gbps for a 6Gbps GMSL2 link and 2.6Gbps for a 3Gbps GMSL2 link. The maximum payload data rate in the reverse direction is approximately 162Mbps for a 6Gbps or 3Gbps GMSL2 link.

The number of D-PHY v1.2 data lanes in a CSI-2 port is programmable as one, two, three, or four lanes. The maximum bit rate per lane is 2.0Gbps.

Figure 20 shows two video sources operating independently. The sources can have different video timing, resolutions, frame rates, and data types. Both serial links must be set to the same forward rate (both 3Gbps or both 6Gbps).

Data from link A and link B are output on separate dedicated CSI-2 ports for capture by the SoC. Dedicated ports allow an SoC with slower D-PHY lanes to capture data from two high-bandwidth sources.

Figure 21 shows two video sources operating independently. The sources can have different video timing, resolutions, frame rates, and data types. Both serial links must be set to the same forward rate (both 3Gbps or both 6Gbps).

In this example, data from link A and link B are aggregated before being output for capture by the SoC. Aggregating reduces the number of CSI-2 ports required on the SoC.

The SoC identifies the video source by reading the packet's virtual channel or data type. If both sources use the same virtual channel or data type, the MAX9296A can be programmed to assign a different virtual channel and/or data type (16 of each are available).

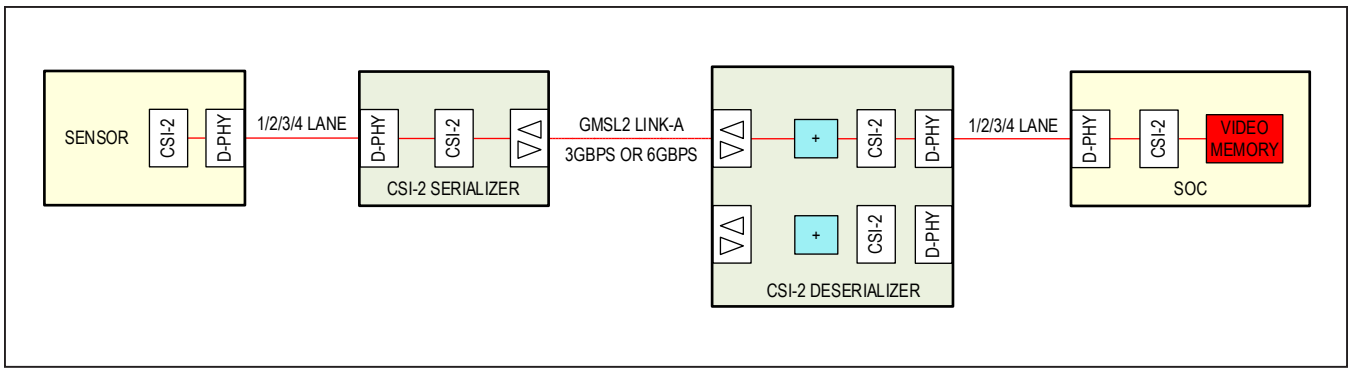

Figure 19. Single GMSL2 Link

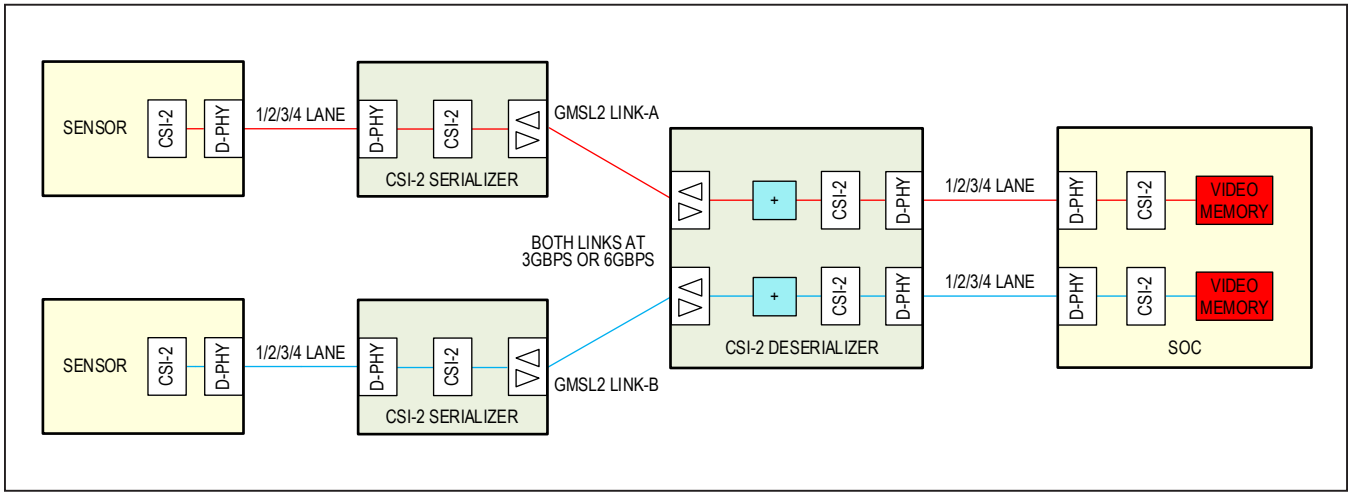

Figure 20. Independent GMSL2 Links with Dedicated Outputs

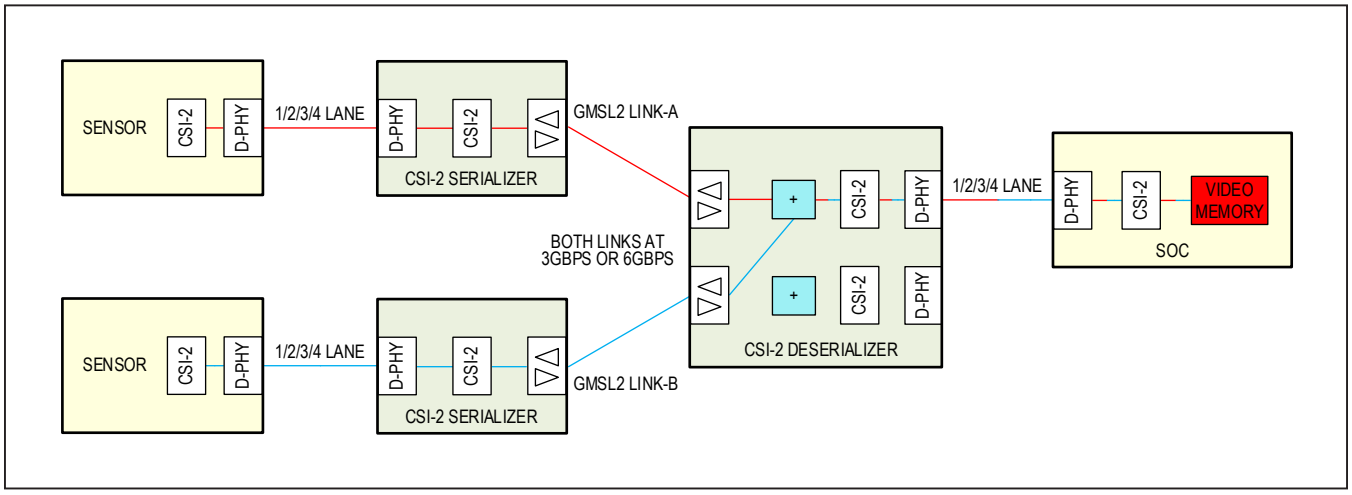

Figure 21. Independent GMSL2 Links with Aggregated Output

Figure 22 shows two video sources operating independently. The sources can have different video timing, resolutions, frame rates, and data types. Both serial links must be set to the same forward rate (both 3Gbps or both 6Gbps).

In this example, data from link A and link B are aggregated and output on one CSI-2 port and replicated on the other CSI-2 port. Data on the replicated output is captured by a second SoC for dual processing.

Figure 23 shows two video sources operating independently over GMSL1 and GMSL2 links. The sources can have different video timing, resolutions, frame rates, and data types. Typically, video on the GMSL1 link is a single data type. Unlike a CSI-2 interface, the parallel interface of the source on the GMSL1 link does not provide a virtual channel or data type to forward to the MAX9296A. Instead, the virtual channel and data type for the GMSL1 link can be assigned by programming MAX9296A registers.

The GMSL1 link maximum payload data rate is 3.6Gbps when paired with a GMSL2 serializer operating in GMSL1 compatible mode at 4.5Gbps. When paired with legacy GMSL1 serializers, the forward channel rate is limited to the serializer's highest data rate. The maximum control-channel bit rate for all GMSL1 devices is 1Mbps.

In this example, data from GMSL2 link A and GMSL1 link B are aggregated before being output for capture by the SoC. Aggregating reduces the number of CSI-2 ports required on the SoC.

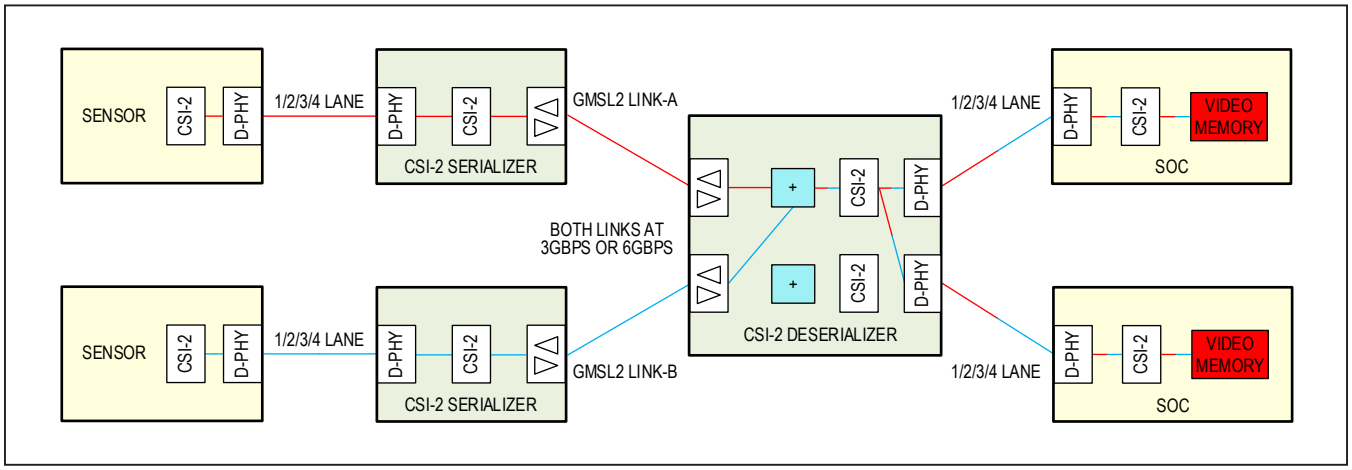

Figure 22. Independent GMSL2 Links with Aggregated and Replicated Output

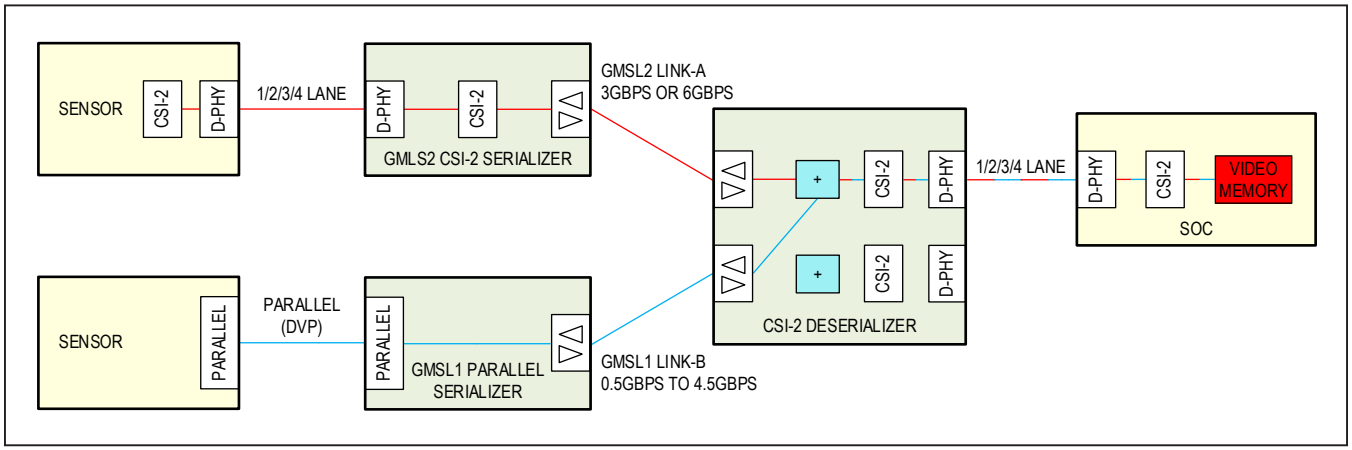

Figure 23. Independent GMSL1 and GMSL2 Links with Aggregated Output

Figure 24 shows a dual link transporting video for capture by an SoC. The logical function of dual link is the same as the single link in Figure 19, but bandwidth is shared equally on two links instead of one, doubling the data rate compared to the single link. In dual link mode, circuitry in the MAX9296A compensates for typical mismatches in serial link interconnect delay. The maximum payload data rate in the forward direction is approximately 10.4Gbps for a 2x 6Gbps dual link and 5.2Gbps for a 2x 3Gbps Dual Link. The data rate in the reverse direction is approximately 364Mbps (2x 162Mbps) for both forward rates.

Other Functions

GMSL2 serializers and deserializers have a main I²C/UART control-channel interface that an ECU uses to access serializer and deserializer registers and peripheral devices from either end of the link. Each device also has two pass-through I²C/UART channels available for local or remote peripheral control. The pass-through I²C/UART channels do not have access to serializer and deserializer registers.

For peripheral control, the MAX9296A includes an SPI master/slave interface with two slave select pins. The SPI interface enables a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. The host can be located at either end of the link, or can swap ends by reprogramming the GMSL2 devices. A GMSL2 device can be configured as an SPI master or slave.

The multifunction pins (MFPs) on the MAX9296A can be configured to provide a variety of general-purpose input, output, and input/output functions (GPIOs). GPIOs are typically used to pass low speed (< 100Kbps) signals over the GMSL2 link, although rates in excess of 1MHz are also supported. A pass-through GPIO can be set up in the forward or reverse direction.

The MAX9296A includes a video crossbar and watermark generation or detection. The crossbar can be used to reorder the color and sync signals. Watermark generation and detection is used to verify that the video image is not frozen.

GMSL2 devices incorporate numerous link-margin optimization and monitoring functions to aid in maximizing link-margin. Continuous (1Hz) adaptive equalization optimizes link-margin to adapt to environmental changes and cable aging. An eye-opening monitor with various threshold alarm levels provides continuous link-margin diagnosis. The monitor issues a runtime alert whenever link degradation is detected. PRBS checking verifies correct link and video-channel operation.

GMSL2 Protocol

GMSL2 is a fixed-rate transmission medium designed to carry multiple types of communication channels concurrently. The link bit rate is based on either a constant-frequency link clock generated from the 25MHz crystal oscillator or on an external reference frequency. The link clock is completely independent of the video pixel clock.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels. Bandwidth allocation is dynamic. An inactive channel consumes no link bandwidth to allow other active channels to share the full link bandwidth. Maximum packet size is limited, preventing a single channel from consuming link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill the unused link bandwidth.

The same data protocol is used on forward and reverse channels and for both video and control-channel data.

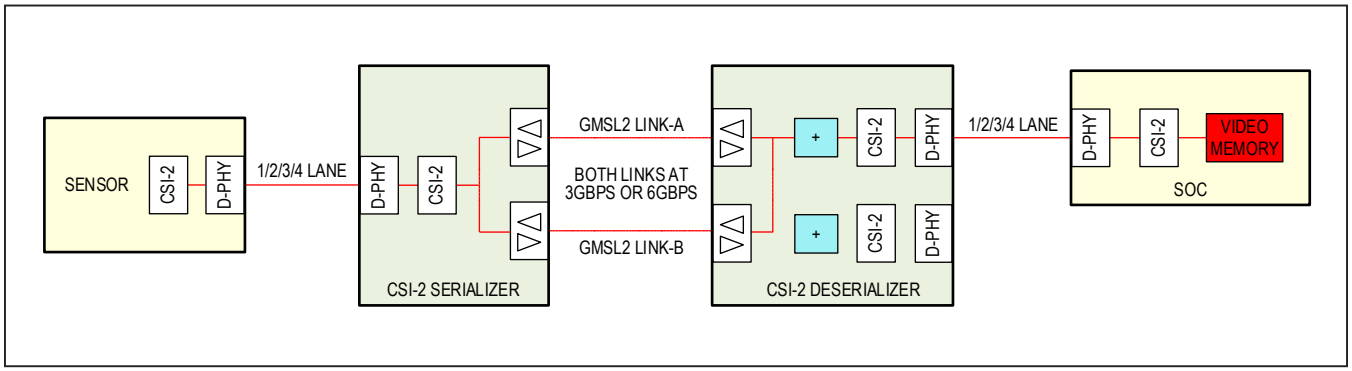

Figure 24. Dual Link GMSL2

GMSL2 Physical Layer

Maxim's GMSL2 serial links family has transmitter and receiver capabilities enabled simultaneously, allowing full-duplex operation on a single wire. A single cable between the serializer and deserializer delivers data transmitted from each end of the link. Forward transmission refers to data sent from the serializer to the deserializer. Reverse transmission refers to data sent from the deserializer to the serializer.

Fixed forward rate options of 3Gbps or 6Gbps are available for both coax and STP. The defaults are 6Gbps in coax mode and 3Gbps in STP mode. The reverse rate is fixed at 187.5Mbps for devices intended for camera, radar, and lidar applications. Both forward and reverse rates are doubled in dual link configurations, in which a serializer and paired deserializer are connected using two links. Dual link mode is not available in all GMSL2 device configurations.

Cabling Options

GMSL2 accommodates either 50Ω coaxial or 100Ω shielded-twisted pair (STP) cabling. Applications using two links can also use shielded-twisted quad (STQ) cabling.

Cables must have sufficient return and insertion loss characteristics for best full-duplex link performance. The available link rates and GMSL2 dynamic link optimization enable support of a wide range of cabling options. Contact the factory for insertion and return loss guidelines.

CFGI's level at at power-up determines which cabling option—coax or STP—applies. See Table 11.

In coax mode, use only the noninverted SIO pin. In STP configurations, both the noninverted and inverted SIO pins are enabled by default. Any unused SIO pins must be AC-terminated with 50Ω to ground.

The GMSL2 design guideline allows cable lengths of up to 15m for coax or up to 7.5m for STP commonly used in the automotive industry. The guideline assumes two in-line connectors (in addition to the endpoint connectors) and 25mm of PCB trace at each end.

A 100nF AC-coupling capacitor is normally used for GMSL2 links.

Line Fault

GMSL2 deserializers include a novel line-fault detection circuit that detects and reports open-circuit, short to battery, short to ground, and line-to-line short. The line-fault monitor requires external resistors R_{EXT} and R_{PD} connected to the LMN_ pins as shown in Figure 25 and Figure 26.

Line-fault detection configuration options and status are available through registers. If unmasked, a line-fault condition asserts ERRB. **Line-fault detection cannot be used when power is supplied over the link (i.e., power over coax, or POC).**

The line-fault monitor pins offer flexible connection and programming. When the MAX9296A is used with twisted-pair cables, either monitor pair (LMN0/LMN1 or LMN2/LMN3) can connect to either serial I/O pair (SIOAP/SIOAN or SIOBP/SIOBN). The polarity of a monitor pair's connection to the twisted-pair cable is arbitrary.

When the link is single-ended (coax), any of the line-monitor pins can be used.

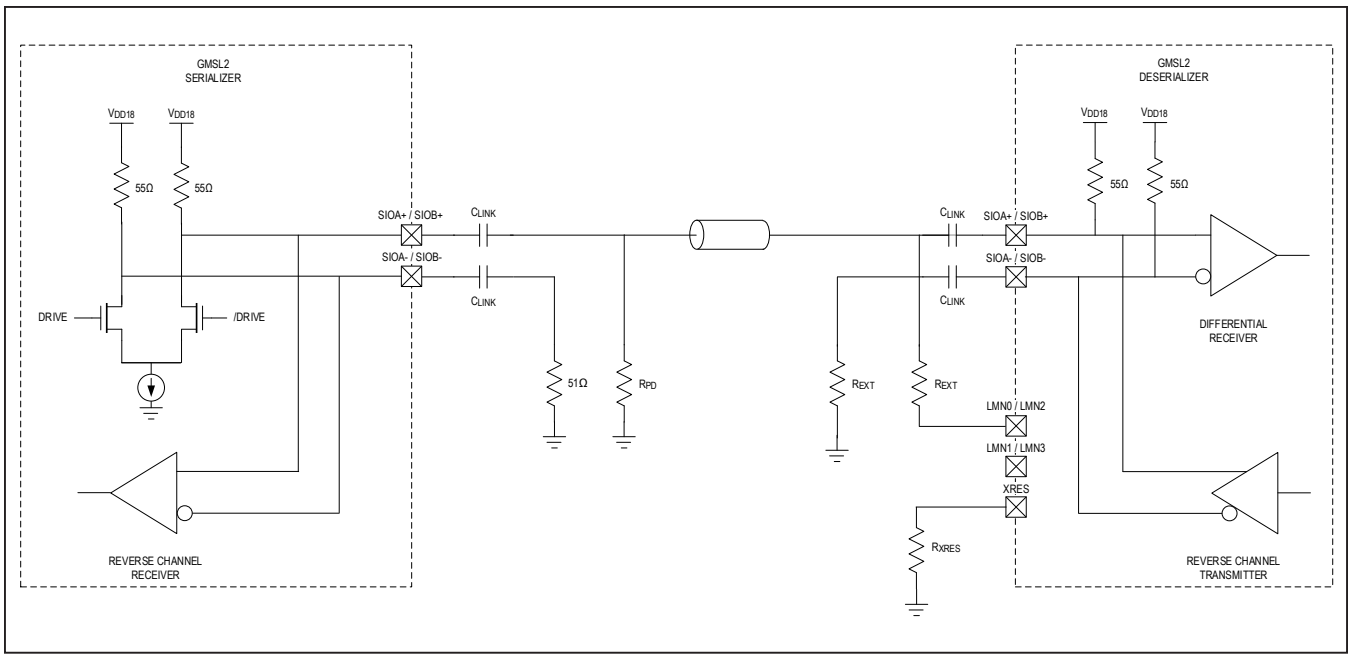

Figure 25. Line Fault Detection Connection for Coax Cable

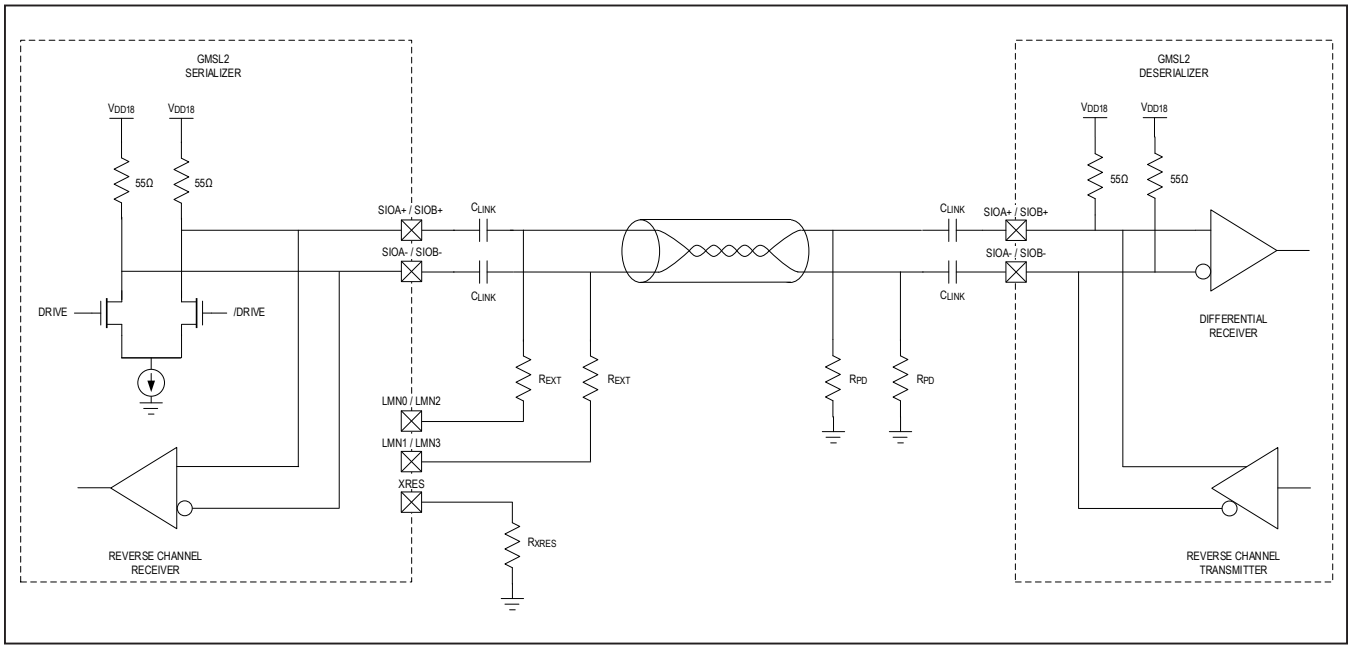

Figure 26. Line Fault Detection Connection for STP Cable

GMSL2 Bandwidth Sharing

The GMSL forward bandwidth is shared among video, the I²C/UART control channel, pass-through I²C/UARTs, SPI, and GPIOs, as well as various protocol-specific data exchanges (i.e., info frames, sync, and acknowledgements). The reverse-channel bandwidth is similarly shared, with the exception of video packets.

The total link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth.

A packet-based transmission format and dynamic bandwidth allocation allow link bandwidth to be shared flexibly among the various communication channels that request the link for packet transmissions. With dynamic bandwidth allocation, an inactive channel consumes no link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol limits maximum packet size to prevent a single channel from monopolizing the link bandwidth at the expense of other channels.

The video and control-channel packets can be assigned a priority level of low, normal, high, or urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with maximum latency requirements can be assigned an increased priority.

GMSL2 Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps or 6Gbps. The reverse link rate is also fixed at 187.5Mbps for devices intended for camera, radar, and lidar applications. The GMSL2 protocol overhead is approximately 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction.

Worst-case applications must not exceed the available throughput of the forward and reverse links. Maxim's evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that estimates initial bandwidth requirements. Maxim also offers other tools useful for calculating link bandwidth utilization. Consult the factory for high-bandwidth use cases to ensure error-free performance.

Table 3 provides rough estimates of the bandwidth utilization for each of the communication channels.

Table 3. Forward and Reverse Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION MAX9296A
Forward Video	H x V x fps x bpp x (1+% blanking) x 1.14
I²C	18 to 60 x I²C clock rate, depending on available link bandwidth
UART	6 x UART bit rate, 5.5 x when parity bit enabled
SPI	2.5 x SPI rate
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Definitions:

H = horizontal resolution

V = vertical resolution

fps = frames per second

bpp = bits per pixel

blanking = total horizontal and vertical blanking

GMSL1 Backwards Compatibility

The MAX9296A is designed to pair with any GMSL1 serializer. However, some GMSL1 serializer features are not supported. GMSL1 backwards compatibility is only supported with forward link rates from 500Mbps to 4.5Gbps and a reverse link rate of 1Mbps. The full 4.5Gbps GMSL1 forward link bandwidth is available only when the MAX9296A is paired with GMSL2 serializers that include GMSL1 support. In this case, both devices must be configured to use GMSL1 compatibility mode. When the MAX9296A is paired with a legacy GMSL1 only serializer, the MAX9296A must be configured for GMSL1 compatibility mode, and the available forward link rate is reduced to comply with the limitations of the specified GMSL1 serializer.

Table 4 specifies the availability of common GMSL2 features in GMSL2 devices that are operated in GMSL1 mode. The MAX9296A might not support all GMSL1 features in Table 4. Some GMSL2 features, such as SPI, are only available in GMSL2 mode, and as a result, they are never available in GMSL1 mode regardless of the devices used. Features not supported by both devices in a link must be disabled. All utilized features must be enabled and configured consistently, with settings appropriate to both ends of the link.

Most features specified in Table 4 can be enabled/disabled by appropriate register configuration and/or configuration input pin power-up state. Serializer and deserializer subsystems are responsible for implementing the configuration pin connections needed to achieve the desired settings. Interfacing coax interconnects to non-coax capable GMSL1 devices requires special hardware considerations to ensure reliable functionality. Contact the factory for additional information regarding general GMSL1 operation or GMSL1/GMSL2 device interoperability.

GMSL1 mode designs can increase activity detector noise tolerance by writing to the activity detector threshold register LOSVTH<6:0> = 0x08 (0x143C<6:0> and 0x153C<6:0> for SIOA_ input and SIOB_ input, respectively).

Table 4. Feature Availability in GMSL1 Mode

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
Coax	Yes	Yes
Bus Width Select (BWS)	Yes	Yes
High-Bandwidth Mode (HIBW)	Yes	Yes
Data Rate Select (DRS) (Low speed mode)	Yes	Yes
DBL (Double Mode)	Yes	Yes
HSYNC/VSYNC Encoding	Yes	Yes
Pixel CRC (6 bits per pixel)	Yes	Yes
Video Line CRC (32 bits per line)	Yes	Yes
Hamming Error Correction	No	No
I^2C to I^2C	Yes	Yes
UART to UART	Yes	Yes
UART to I^2C	No	No
Pass-Through I^2C Channels	No	No
I^2C Address Translation	Yes	Yes
SPI Control Channel	No	No
High-Immunity Mode	Yes	Yes
REV_FAST with HIBW Mode	Yes	Yes
Packet Control Channel with CRC	Yes	Yes
Packet CC Retransmission	Yes	Yes
Configuration Link	Yes	Yes

Table 4. Feature Availability in GMSL1 Mode (continued)

FEATURE NAME	GMSL2 SERIALIZER IN GMSL1 MODE	GMSL2 DESERIALIZER IN GMSL1 MODE
I²S on Forward Link	Yes	No
I²S on Reverse Link	No	No
7.1 TDM	Yes	No
GPI to GPO on Reverse Channel	Yes	Yes
Frame Sync	Yes	Yes
Delay Compensated GPI/GPO	No	No
Line Fault	Yes	Yes
UART Base Mode	Yes	Yes
UART Bypass Mode	Yes	Yes
Spread Spectrum	Yes	Yes
Pre/Deemphasis	No	N/A
Legacy Programmable Equalization	N/A	No
Adaptive Equalization	N/A	Yes
Twisted Pair Splitter Mode	No	N/A
Auto HDCP	No	No
Watermark	Yes	No
Video Timing Generator	Yes	No
Video Crossbar	Yes	Yes
PRBS	Yes	Yes
CNTL0, 1, 2, 3 on Forward Channel	Yes	Yes
A/V Status Register Interrupt	No	No
Serializer Audio Output from HDMI Source	Yes	N/A
HS/VS/DE Inversion	Yes	Yes
WS/SCK Inversion	Yes	N/A
Jitter-Filtering PLL	No	No
Sleep Mode	Yes	Yes

Power Supplies

The MAX9296A offers an array of power supply configuration options.

The 1V core supply can be provided directly or by an internal regulator. For optimum power efficiency, connect 1.0V ±5% to V_{DD}. If using the internal regulator, connect 1.2V ±5% to V_{DD}, and first write REG_ENABLE = 1, then write REG_MNL = 1.

The V_{DDIO} supply for the GPIO pins can be 1.8V to 3.3V for flexibility in accommodating devices interfacing to the part. The allowable supply voltage range is 1.7V (1.8V -5%) to 3.6V (3.3V +9%).

V_{DD18} is the primary analog supply. It requires a 1.8V ±5% connection.

V_{TERM} is the D-PHY termination supply. It requires a 1.2V ±5% connection.

See Table 1 for power supply tolerances and noise requirements. Properly bypassing all power supplies is essential to ensuring high frequency circuit stability See Table 2. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

Thermal Management

Power consumption of GMSL2 devices varies depending on how the device is used. Care must be taken to provide sufficient heat dissipation with proper board and cooling design techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below +125°C to meet electrical specifications and avoid impacting device reliability.

Refer to Application Note 4083: *Thermal Characterization of IC Packages* for guidance.

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. All GMSL2 devices support the following interfaces:

- Main I²C/UART (internal access)
- Pass-through I²C/UART
- SPI
- GPIO

Some GMSL2 devices also support the following interfaces:

- I²S/TDM audio
- RGMII/RMII

All of the above interfaces can pass data through the GMSL2 link, but the GMSL2 device registers can be accessed and configured only through the main I²C/UART interface.

The side channel, with its various interfaces, is accessed using multifunction pins. Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit in the number of pins available on a given device, not all interfaces can be simultaneously supported. See Table 7 and Table 8 and the *Pin Description* section for default and alternate multifunction pin functions, as well as available combinations of interfaces.

Main I²C/UART

The main I²C/UART is located on the SDA_RX and SCL_TX pins of each GMSL2 device. The I²C (SDA, SCL) or UART (Tx, Rx) interface is selected by the CFG0 pin voltage at power-up (see Table 10). The selected interface provides master access to both GMSL2 registers and device registers from either end of the link.

The master µC can reside on either end of the link (usually the serializer side for display applications and the deserializer side for camera applications). The MAX9296A supports dual master microcontrollers provided that software arbitration (such as token passing) is used to prevent packet collisions. The control channel allows only one master µC to communicate at a time.

To configure peripheral devices over the link, the GMSL2 serializer and deserializer must use the same control-channel interface (both I²C or both UART). Unlike GMSL1 devices, there is no I²C-to-UART conversion capability. I²C/UART outputs are open-drain and require appropriately sized external pullup resistors for proper operation.

Pass-Through I²C/UART

GMSL2 devices have two pass-through I²C/UART channels. These channels do not have access to registers in either the GMSL2 serializer or the deserializer; they simply tunnel the I²C or UART signal across the GMSL2 link. This allows I²C channels to be separated so that no multimaster conflicts occur. I²C/UART outputs are open drain and require appropriately sized external pullup resistors for proper operation.

SPI

GMSL2 enables a host SPI master on one side of the GMSL2 link to control a peripheral SPI slave on the opposite side. Communication can be in either direction across the GMSL2 link.

The SPI clock range is 600kHz to 50MHz. Care must be taken to meet setup and hold time requirements when using at speeds higher than 20MHz.

General-Purpose Inputs and Outputs (GPIO)

GPIOs are typically used to pass low-speed (< 100Kbps) signals over the GMSL2 link. A pass-through GPIO can be set up in the forward (serializer to deserializer) or reverse (deserializer to serializer) direction. GPIO transmissions are transition-based; a GPIO packet is created and transmitted on the GMSL2 link when a rising- or falling-edge transition is detected at a GPI pin. The transition is regenerated at a GPO on the other end of the link.

The multifunction pin GPIO can be programmed as GPI (input), GPO (push-pull output or open-drain output), or GPIO (bidirectional input/output). Each GPIO can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). Although an internal pullup is provided, high-speed open-drain outputs require an appropriate value external pullup resistor to V_{DDIO}. Inputs cannot be left floating. Always ensure that every pin configured as an input has a pullup or pulldown programmed or is driven by another IC.

A GPI on one side of the serial link can be mapped to a single GPO or multiple GPOs on the other side of the link. Each GPI is assigned a pin ID, with the destination GPO(s) on the other side of the link set to the same pin ID. By default, the ID mapping is GPIO0-GPIO0, GPIO1-GPIO1, GPIO2-GPIO2, etc. However, the GPIO mapping can be arbitrarily changed through register settings.

GPI transitions can be transmitted in two modes: delay-compensated and non-delay-compensated. When delay compensation is enabled, the GPI-to-GPO delay across the link is a precise, fixed value. Latency increases, but jitter and skew decrease.

The state of each GPIO can be read or written by register either locally or remotely over the GMSL2 link by a µC using the control-channel I^2C/UART interface.

In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible based on priority and available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-delay-compensated mode should be used with signals tolerant to delay variation (i.e., µC interrupts).

The MAX9296A register settings allow priorities to be assigned to GPI pins. If no priorities are set, GPI transitions are transmitted in the order they occur. However, when priorities are set, transitions on GPIs with higher priority are transmitted earlier.

Typical GMSL2-only device delays for 6Gbps forward and 187.5Mbps reverse-link rates are shown in Table 6.

Table 5. SPI Latching Edge and Speed

FREQUENCY (MHz)	V_{DDIO} (V)	LATCHING EDGE	SPI_SPEED[1:0]
< 12.5	1.7–2.24	Opposite from shift	01
	2.25–3.6		10
12.5–25	1.7–2.24	Opposite from shift	00
	2.25–3.6		01
25–50	1.7–2.24	Same as shift	00
	2.25–3.6		01

Table 6. Typical GPIO Delays for Forward and Reverse Link Transmission

	DELAY COMPENSATION	DELAY
GPIO forwarding from serializer to deserializer (6Gbps forward channel)	0	720ns
	1	3.5µs
GPIO forwarding from deserializer to serializer (187.5Mbps reverse channel)	0	6µs
	1	15µs

MFP Function Map and Speed Groups

Side-channel functions, such as pass-through I²C/UART and SPI, are enabled by programming Multi-Function Pins (MFPs). Each MFP has several possible functions, but only one can be used at a time.

Some functions require only a single MFP, but most are implemented across a group of MFPs. For example, LOCK is a single MFP, but SPI takes several MFPs. A user selects MFP functions to suit their use-case by programming the appropriate registers.

Each MFP is placed in one of four speed groups (A-C and NA) with each speed group having a default output transition time. Register programming allows the transition time of most speed groups to be changed from their default values. However, for the SDA_, SCL_, TX_, LOCK, ERRB and ODO_ functions, the open-drain driver's fall time is not adjustable and the rise time is determined by the value of the pull-up resistor. When a speed group's transition time is changed, the transition time of all applicable functions in an MFP's speed group are changed.

Transition times depend on the transition time setting and V_{DDIO} supply voltage. Refer to Table 9 for typical transition times.

Table 7. GMSL2 Pin Function Map

PIN	LATCH ON POWER-UP	I²C/UART	SPI	OTHER FUNCTIONS	GPIO	POWER-UP DEFAULT	SPEED GROUP	TRANSITION TIME DEFAULT
MFP0		Pass-through I²C/ UART#1 SDA1/RX1 or pass-through I²C/ UART#2 SDA2/RX2	SCLK	FRSYNC_OUT VS2 DE1/DV1 MS	GPIO0	GPI0	A	"10"
MFP1		Pass-through I²C/ UART#1 SCL1/TX1 or pass-through I²C/ UART#2 SCL2/TX2		LOCK	GPIO1	LOCK	C	"11"
MFP2	CFG0		BNE/SS1		GPO2	GPO2	B	"11"
MFP3	CFG1		SS2	VS1 DE1/DV1	GPO3	GPO3	B	"11"
MFP4			RO(Alt)	ERRB	GPIO4	ERRB	C	"11"
MFP5		Pass-through I²C/ UART#2 SDA2/RX2 or pass-through I²C/ UART#1 SDA1/RX1	MOSI		GPIO5	RX1	A	"10"
MFP6		Pass-through I²C/ UART#2 SCL2/TX2 or pass-through I²C/ UART#1 SCL1/TX1	MISO		GPIO6	TX1	A	"10"
MFP7			RO	LMN0	GPI7	GPI7	NA	NA
MFP8				LMN1	GPI8	GPI8	NA	NA
MFP9				LMN2	GPI9	GPI9	NA	NA
MFP10				LMN3	GPI10	GPI10	NA	NA
MFP11		Main-channel SDA/Rx			GPI11/ ODO11	SDA or Rx	NA	NA
MFP12		Main-channel SCL/Tx			GPI12/ ODO12	SCL or Tx	NA	NA

NA = Not applicable

Table 8. GMSL1 Pin Function Map

PIN	LATCH ON POWER-UP	I²C/UART	OTHER FUNCTIONS	GPIO	POWER-UP DEFAULT	SPEED GROUP	TRANSITION TIME DEFAULT
MFP0			FRSYNC_OUT MS CNTL1	GPIO0	GPI0	A	"10"
MFP1			FRSYNC_IN LOCK	GPIO1	LOCK	C	"11"
MFP2	CFG0		CNTL0	GPO2	GPO2	B	"11"
MFP3	CFG1		CNTL3	GPO3	GPO3	B	"11"
MFP4			ERRB	GPIO4	ERRB	C	"11"
MFP5			CNTL2 GPI_1	GPIO5	GPIO5	A	"10"
MFP6			FRSYNC_IN CNTL4 GPI_0	GPIO6	GPIO6	A	"10"
MFP7			LMN0	GPI7	GPI7	NA	NA
MFP8			LMN1	GPI8	GPI8	NA	NA
MFP9			LMN2	GPI9	GPI9	NA	NA
MFP10			LMN3	GPI10	GPI10	NA	NA
MFP11		Main Channel SDA/RX		GPI11/ODO11	SDA or RX	NA	NA
MFP12		Main Channel SCL/TX		GPI12/ODO12	SCL or TX	NA	NA

NA = Not applicable

Table 9. Control- and Side-Channel Typical Rise and Fall Times

PIN OR SPEED GROUP TRANSITION TIMES	RISE TIME*		FALL TIME**	
	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V	V_{DDIO} = 1.8V	V_{DDIO} = 3.3V
LOCK, ERRB	2.1ns	1.1ns	2.0ns	1.1ns
"00"	1.0ns	0.7ns	1.0ns	0.7ns
"01"	3.0ns	1.0ns	3.0ns	1.0ns
"10"	5.0ns	3.0ns	5.0ns	3.0ns
"11"	10.0ns	5.0ns	10.0ns	5.0ns
SDA_, SCL_, TX_, ODO_	***	***	40.0ns	30.0ns

**20% to 80%, 10pF load.*

***80% to 20%, 10pF load.*

****Rise time for open-drain outputs depends on external pullup resistor value.*

CFG Latch at Power-Up Pins

Voltage levels at the CFG0 and CFG1 pins are latched at power-up, or upon a low-to-high transition of PWDNB. These levels set initial register values and functional modes that may not be easily programmed through I²C or UART after the IC powers up. The CFG pins select device address, I²C or UART main control channel, GMSL2 serial rate, and coax or STP cable. See Table 10 and Table 11).

The voltage level for each pin is set by an external precision resistor divider connected between VDDIO and ground (Figure 5), or for some configurations, by a single resistor connected to V_{DDIO} or ground. Table 10 and Table 11 show the recommended resistor values to select each configuration. The voltage level at the CFG pins is typically latched 1ms after all MAX9296A supplies reach minimum levels required by the power-on-reset (POR) circuit. CFG pins must not be loaded with more than 10pF at power-up to ensure the proper voltage level.

If the requirements described in the Table 10 and Table 11 notes are met, the CFG pin's secondary functions can be used after the CFG pin voltage levels are latched at power-up. See the *Pin Description* section and Table 7 and Table 8 for secondary functions). CFG pins cannot be used as general-purpose inputs.

Table 10. CFG0 Input Map

CFG0 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (Notes a, b)			SUGGESTED RESISTOR VALUES (±1% TOLERANCE) (Note c)		MAPPED CONFIGURATION (Note d)	
MIN (%)	TYP (%)	MAX (%)	R1 (Ω)	R2 (Ω)	I²SCEL	DEVICE ADDRESS
0.0	0.0	11.7	OPEN	10000	I²C	0x90
16.9	20.2	23.6	80600	20500		0x94
28.8	32.1	35.5	68100	32400		0xD0
40.7	44.0	47.4	56200	44200		0xD8
52.6	56.0	59.3	44200	56200	UART	0xD8
64.5	67.9	71.2	32400	68100		0xD0
76.4	79.8	83.1	20500	80600		0x94
88.3	100	100	10000	OPEN		0x90

Table 11. CFG1 Input Map

CFG1 INPUT VOLTAGE (PERCENTAGE OF V_{DDIO}) (Notes a, b)			SUGGESTED RESISTOR VALUES (±1% TOLERANCE) (Note c)		MAPPED CONFIGURATION (Notes e, f, g)		
MIN (%)	TYP (%)	MAX (%)	R1 (Ω)	R2 (Ω)	CXTP	GMSL1/ GMSL2	HIM/ GMSL2 RATE
0.0	0.0	11.7	OPEN	10000	COAX	GMSL2	6Gbps
16.9	20.2	23.6	80600	20500		GMSL1	HIM Enabled
28.8	32.1	35.5	68100	32400			HIM Disabled
40.7	44.0	47.4	56200	44200	STP	GMSL2	6Gbps
52.6	56.0	59.3	44200	56200			3Gbps
64.5	67.9	71.2	32400	68100		GMSL1	HIM Enabled
76.4	79.8	83.1	20500	80600			HIM Disabled
88.3	100	100	10000	OPEN	COAX	GMSL2	3Gbps

Notes:

a) Voltage divider resistor tolerance, V_{DDIO} supply ripple, and external loading must not cause the CFG0 or CFG1 input voltage to exceed the maximum or minimum limits.

b) Until the input voltage is latched, any load on CFG0 or CFG1 (other than R1 and R2) must be ≥ 25 x (R1 + R2). Load capacitance (including R1 and R2) must be lumped-load ≤ 10pF.

c) Each resistor in the voltage divider must be ≤100kΩ.

d) I^2CSEL: I^2C or UART interface for SDA_RX and SCL_TX
DEVICE ADDRESS: device address

e) CXTP: Shielded twisted-pair (SIO_P, SIO_N) or coax (SIO_P) serial link.
GMSL1/GMSL2: GMSL1 or GMSL2 operating mode.
HIM applies when GMSL1 operating mode is selected. High Immunity Mode for reverse control channel.
GMSL2 RATE applies when GMSL2 operating mode is selected. 3Gbps or 6Gbps GMSL2 serial link bit rate.

f) Serial links SIOA_ and SIOB_ are set to the same forward rate.

g) GMSL1 default BWS = 0 (24 bit).

Clocking

GMSL Reference Clock

The GMSL2 devices require a reference clock source to generate the 6GHz line rate clock and associated internal clocks. Both the serializer and deserializer can be clocked with an external 25MHz crystal or an external clock source with a frequency accuracy of ±200ppm.

Spread-Spectrum Clocking

Maxim's GMSL2 links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to mitigate electromagnetic interference emitted from devices and interconnections and to provide additional margin.

SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to ±2500ppm from the center frequency.

Power-Up and Link Startup

GMSL2 ICs are in power-down mode when PWDNB pin is low or when any of the power supplies are down. Register and configurations are set to default reset conditions.

The serializer and deserializer can power up in any order. After PWDNB is released and all power supplies are up, each device starts its power-up sequence and performs the following actions in sequence:

1) Latch at power-up pins register set. Set internal registers according to the selected configuration (selected by CFG0, CFG1).
2) Control channel (I^2C or UART) is functional on local side. Device registers are writable and readable.
3) Link is established based on the following settings:
   a) Single-link automatic selection mode (AUTO_LINK = 1 and LINK_CFG = 1 or 2): Automatically select which PHY to use to establish GMSL2 link by periodically attempting to handshake using PHY A and PHY B.
   b) Single-link manual selection mode (AUTO_LINK = 0 and LINK_CFG = 1 or 2): If LINK_CFG = 1, establish link using PHY A. If LINK_CFG = 2, establish link using PHY B.
   c) Dual-link mode (LINK_CFG = 0): Establish link using both PHYs.
   d) Splitter (serializer)/aggregator (deserializer) mode (LINK_CFG = 3): Establish link using both PHYs (for specific applications only).
4) Each enabled PHY performs link calibration, equalizer adaptation, and data-channel locking. Both chips set their LOCK pin high.
5) Control channel is available from the remote side.

This entire link-up process, from the time that the last part's PWDNB input is brought high, takes approximately 20ms nominally and 100ms maximum for any channels that meet the GMSL2 channel specification.

After the devices are linked, they can be configured. This can be done locally or over the control channel, by a microcontroller on either the serializer side or the deserializer side.

Device Reset

There are three general-reset options available through register writes:

1) RESET_ALL resets all blocks, including all registers, digital blocks, and analog blocks. This process is similar to driving the PWDNB pin low and then high.
2) Setting RESET_LINK resets all GMSL PHY-related digital logic and all data pipelines. After this bit is set, all control registers are still accessible through the local control channel. The link remains in RESET until RESET_LINK is cleared.
3) RESET_ONESHOT resets all GMSL PHY-related digital logic and all data pipelines, and then automatically clears itself. This is similar to setting and clearing RESET_LINK.

Program the registers that affect GMSL-2 link operation (i.e., TX_RATE, RX_RATE, CXTP_A/B, AUTO_LINK, LINK_CFG, GMSL2) first, followed by RESET_LINK or RESET_ONESHOT.

Link and Video Lock

Link Lock

Link lock happens automatically on power-up, and is an indication that the cable is plugged in and the system is running. Lock is obtained with no interaction or commands from the microcontroller to the GMSL2 parts.

Link lock indicates that the PLLs for the GMSL2 link are locked to each other and the data receive paths are locked (forward channel in serializer, reverse channel in deserializer). Video and control-channel functions (I^2C/UART, SPI, GPIO) can be used immediately after link lock is asserted.

In dual link, only one link locks automatically. The user must then program the serializer to the desired operating mode.

The GMSL2 link uses the crystal or external reference input as the reference clock for the GMSL2 link, so a valid video input (pixel clock) is not needed for the GMSL2 link to lock.

Video Lock

The video-lock bit indicates that the deserializer is receiving valid video data. After the GMSL2 link has locked, the deserializer video output PLL begins its locking sequence. The deserializer normally begins outputting video data several milliseconds after it asserts line lock, provided that it is receiving video packets from the serializer. The video lock status is typically read from a register. However, the deserializer LOCK pin behavior can be changed by a register setting so that the LOCK pin is asserted only when the deserializer is outputting video.

Power Standby and Sleep Mode

A power-manager block is present in all GSML2 products. Its primary function is to monitor supply voltages and control power-down (standby) and sleep modes.

There are two ways to enter low-power mode while all power supplies are active: asserting the PWDNB pin or invoking the sleep state. Both states offer very low power supply currents.

Asserting the PWDNB pin (active-low) places the device in standby power mode and resets the digital registers and configurations to their default power-up condition. Any supply that drops below its internal threshold settings also places the device in power-down mode.

The sleep state offers the preservation of all critical register settings and configurations. The device can be put into the sleep state through an I^2C/UART command. The resume state restores the device to the pre-sleep condition, without the need for additional register writes. Resume is invoked by an I^2C command or a low-frequency clock beacon transmitted from the master device over the GMSL2 link.

Error and Fault-Condition Monitoring

Both the serializer and deserializer have an open-drain, multipurpose error reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a subblock of registers, so the reason for assertion of ERRB can be determined by reading the register status.

AEQ (Adaptive Equalization)

GMSL2 devices automatically adapt receiver characteristics to compensate for the insertion and return loss characteristics of the channel, which consist of the cables, connectors and PCBs. This optimizes performance on any channel that meets the GMSL2 channel spec.

The equalizer architecture makes GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and is then invoked at a rate of approximately 1Hz to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to maximize the eye opening using the built-in eye-opening monitor.

Video Pipes, Aggregation and Replication

See Figure 27, and Figure 28.

In GMSL2 pixel mode, the transportation of video data is based on the concept of video pipes. Carrying data in pipes allows GMSL2 to bridge different digital video interfaces (i.e., HDMI source to CSI-2 sink) and perform watermark generation and detection.

A pipe carries a video stream (or streams) and associated video synchronization data.

A pipe operates in one of three modes. In all modes, a pipe can carry multiple concurrent video streams, with each stream having different virtual channels and data types, as follows:

Mode 1: Streams with constant bpp of up to 24bpp. The bpp of the streams must be the same.

Mode 2: Streams with 16, 14, 12, 10, or 8bpp. Streams less than 16bpp are padded with zeros.

Mode 3: Streams with two different bpp values. The bpp of one stream must be twice the bpp of the other stream. The higher bpp stream maximum is 24bpp.

Modes 1 and 3 carry data at full bandwidth but put more restrictions on bpp than Mode 2. Mode 2 allows streams with different bpp, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL2 link (because of zero-padding). Mode 1 or Mode 3 are sufficient for most applications. Mode 2 requires less programming and is more convenient if the application does not require maximum link bandwidth.

The MAX9296A has four video pipes. If a rear-view camera with YUV422 output is connected (for example), one pipe is sufficient to carry the YUV422 video stream. High bandwidth, high dynamic range (HDR) cameras that output multiple-exposure data usually require more than one pipe. In an HDR camera application with multiexposure data of RAW16 and RAW12 per pixel along and two lines of embedded data per frame would, in Mode 3, use one pipe for RAW16 and embedded 8-bit data and, in Mode 1, another pipe for RAW12 data. The total number of pipes used by all serializers connected to the MAX9296A can not exceed four pipes.

Each of the four pipes in the MAX9296A has a dedicated video-line buffer. Each 32k byte (256kb) video-line buffer has capacity for a line length of up to 8191 24-bit pixels (8191 pixels includes line-blanking pixels).

Before data enters a line buffer, it goes through a cross-point switch and a data type (DT) and virtual channel (VC) reassignment stage. If the video source has a CSI-2 output, packet DT and VC can be left as-is or reassigned through register programming. Up to 16 DT/VC incoming pairs can be mapped to 16 DT/VC outgoing pairs.

If the video source does not have a CSI-2 output, a DT and VC can be programmed in the MAX9296A for insertion into the CSI-2 output packet. The cross-point switch can change the order of the bits in the incoming video pixel data to any order, if desired.

A line buffer stores a complete line of video data before the data is available for read-out by an aggregator. Each buffer connects to two aggregators, but only one aggregator (as programmed by the user) can read a line of data out of the buffer at a time. Once data is read out, it cannot be read out a second time by the same aggregator or by the other aggregator. However, in a time-domain multiplexed fashion, both aggregators can be programmed to read from same buffer. Up to four pipes can be aggregated by one aggregator.

Data is read out from line memory on a first-come, first-served basis. When a complete line of video data has filled a line memory, it is read out. The order in which the line memories reach filled status is the order in which they are read out.

Video data can be routed according to DT or VC, based on the source CSI-2 packet's DT/VC, or by a DT/VC assigned or reassigned by the MAX9296A. For example, data in Pipe X with VC0 can be programmed to be read out by Aggregator A, while data in Pipe X with VC1 can be programmed to be read out by Aggregator B.

The aggregator forwards the line of video from the line buffer and video synchronization data to its associated CSI-2 controller for packet generation. Packets can be output on the controller's port or replicated by routing them to the other port. For example, CSI-2 controller A can output packets on D-PHY Port A or also route them for output on D-PHY Port B.

A D-PHY port can only accept packets from one controller; it cannot aggregate packets from the two controllers.

To prevent buffer overflow, the CSI-2 port data rate needs to be programmed to a value that is greater than or equal to the incoming data rate. Programming the output rate to be faster than the bandwidth of the incoming video increases packet spacing (LP time between packets).

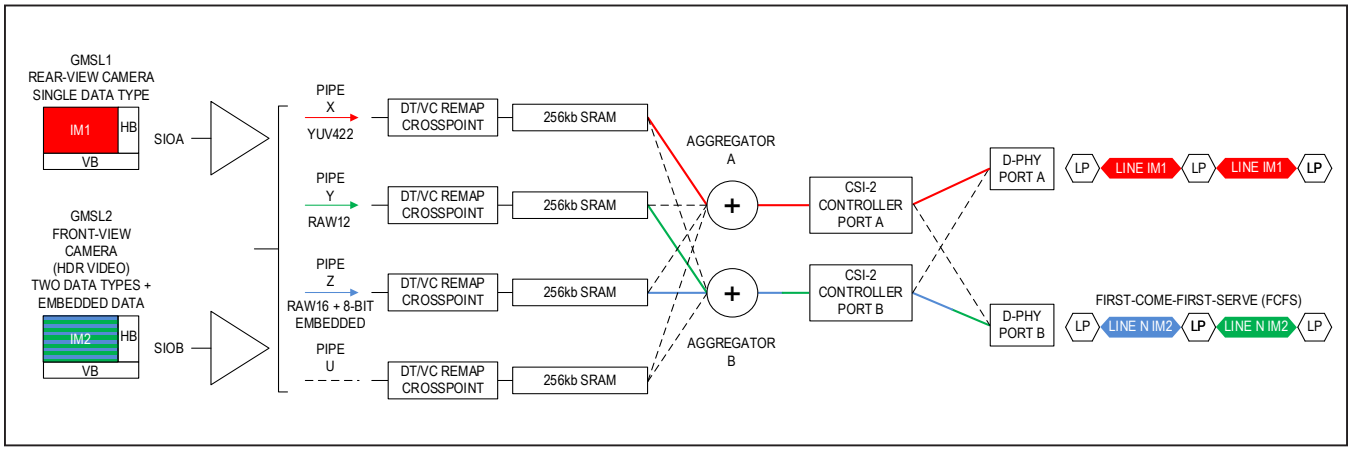

Figure 27. GMSL1 and GMSL2 Camera Video Output on Separate Ports

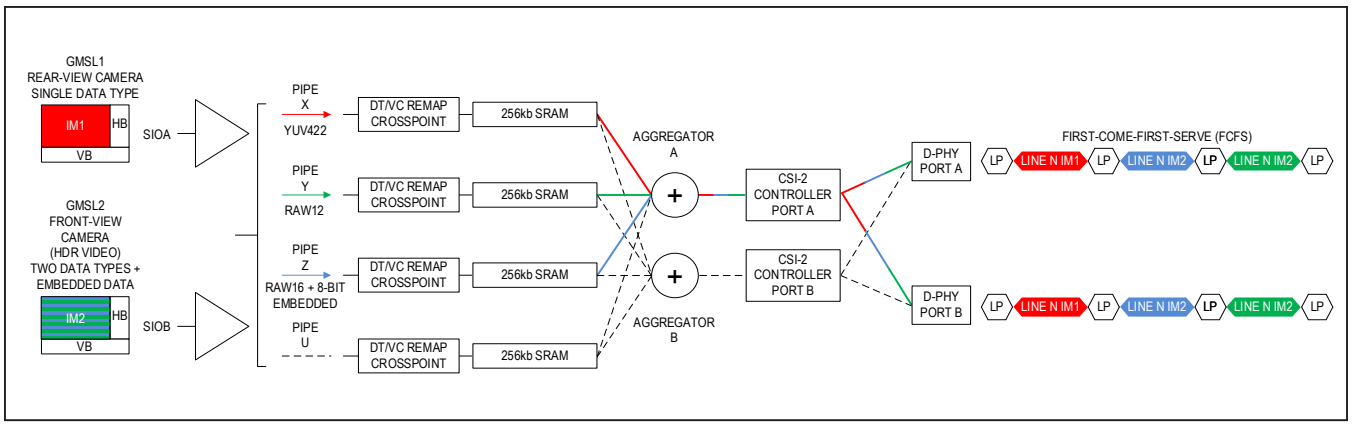

Figure 28. GMSL1 and GMSL2 Camera Video Aggregated and Replicated

Video Line CRC

A CRC32 polynomial is used to generate a 32-bit code at the end of each DE (data enable) or DV (data valid) pulse (DE is default; DV can be selected instead by register). The code is transferred to the receiver (deserializer) side using info frames. The CRC checker generates the same code on the receiver side and checks if the generated and received CRC codes are the same. If not, it asserts an error. The CRC check is done at every falling edge of DE (or DV when selected) on the receiver side, even if the info frame is not received.

Eye-Opening Monitor

The eye-opening monitor (EOM) enables GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error-free, but have less link margin than desired. This allows the customer to proactively react to deteriorating cable performance before any link errors occur.

GMSL2 devices can measure the horizontal or vertical eye-opening of the equalizer's output. The measurement is activated automatically at a rate of approximately 1Hz once a link is active. The EOM block compares the data sampled at the center of the eye with a sample that is offset in phase for the horizontal EOM or offset in voltage for the vertical EOM. The eye-opening is then reported, and the EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

Watermarking

The watermarking block allows users to detect a frozen-frame failure in a frame-based processing system between the generator and detector. This feature is specifically targeted to detect frozen frames caused by SoCs in safety-critical applications. It does not detect frozen frames that occur before the watermark generator or after the watermark detector.

GMSL2 devices contain both a watermark generator and watermark detector. This allows both serializers and deserializers to insert a watermark or detect a watermark in a safety-relevant video stream. The watermark generator inserts a time-varying watermark that is highly redundant and robust to image processing and display stream compression. The watermark detector looks for this time-varying watermark, and failure to see all of the generated watermarks indicates a frozen-frame failure in a frame-based processing system between the generator and detector. Upon detection of this error condition, the watermark detector can generate an interrupt and/or blank the output video, returning the display to a safe state in less than 500ms.

Vertical and Data Enable or Data Valid Sync Outputs

The MAX9296A can output the vertical sync (VS) and data enable/data valid (DE/DV) of a video stream for monitoring of video timing by a processor. This feature provides access to VS and DE/DV signals not available directly at the CSI-2 output. VS and/or DE/DV output are alternate functions of MFP2 and MFP3.

PRBS

Video PRBS

The video channel has a PRBS generator in the serializer and a PRBS checker in the deserializer for testing the video channel operation. The video PRBS generator can work with the PCLK recovered by the serializer from an HDMI, parallel, or MIPI input. An external PCLK can also be provided to a designated GPIO pin to run the video PRBS generator.

Note that all link bandwidth is not used by the video channel alone in GMSL2 mode, so it is possible to have a bit error on the link that does not cause a video PRBS error.

Link PRBS

The GMSL PHY has a link PRBS feature for testing link integrity for every link bit. In this mode, the link is not established as in normal operation, but instead the link integrity test is performed in both directions of the link simultaneously using a PRBS-7 pattern. This feature is feasible only when the user has simultaneous local control-channel access to both ends of the link. Contact the factory for programming procedures regarding link PRBS mode.

CSI-2 Port

Packets are generated according to the MIPI CSI-2 v1.3 protocol specification and the MIPI D-PHY v1.2 transmitter physical layer specification (refer to these MIPI standards for details). The CSI-2 controllers in the MAX9296A have been upgraded to include the CSI-2 v2.0 virtual channel extension for D-PHY to allow 16 virtual channels instead of the 4 virtual channels specified in the CSI-2 v1.3 specification.

Within a port, any number of data lanes can be enabled (one, two, three, or four lanes). To ease PCB layout, swapping of data lanes and swapping of the polarity of the differential signals within a lane are supported. For example, the position of data lane 3 can be exchanged with the position of data lane 2 (lane swap), and the inverting and noninverting outputs of data lane 1 can be swapped (polarity swap).

Initial and periodic deskew pattern generation by the D-PHY port is supported (deskew is required for data-lane bit rates > 1.5Gbps and optional for bit rates ≤ 1.5Gbps).

The default D-PHY lane rate is 1.5Gbps/lane. The lane rate can be changed in 100Mbps steps with simple register programming. More involved register programming allows smaller step changes in the lane rate.

An unused D-PHY port or CSI-2 controller can be individually powered down to save power.

When a port is programmed to use fewer than four data lanes, the unused lanes should be left open.

Applications Information

Control Channel Programming

GMSL2 device registers are accessed and configured only through the main I²C/UART interface.

Host-to-Peripheral Main I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, main and pass-through I²C operation is the same. An I²C tunnel across the GMSL2 link connects the host's I²C master to the peripheral's I²C slave. This logically connects separated I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I²C master connects to a GMSL2 device I²C slave, and the peripheral I²C slave connects to a GMSL2 device I²C master.

For example, when the host I²C master transacts on one side of the link (local side), data is forwarded to the other side (remote side) by the I²C slave of the local-side GMSL2 device. Data is then received by the I²C master of the remote-side GMSL2 device, which in turn generates the same I²C transaction with the peripheral slave I²C. The remote-side GMSL2 device sends back any I²C data expected by the local side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between master and slave and to allow time for data to be forwarded and received across the serial link. The host I²C master and peripheral I²C slave must support clock stretching by the GMSL2 device.

SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address auto-increments).

Device Address

Each device on the I2C UART control channel must have a unique address. The GMSL2 device address is set to one of several 7-bit addresses according to the voltage level of the ADD or CFG pins at power up. See the *CFG Latch at Power-Up Pins* section. Note that device address can be changed after power-up by writing to the DEV_ADDR register.

Main I2C Host-to-GMSL2 Device Communication

The host I2C master has access to GMSL2 serializer and deserializer registers. The host can program GMSL2 device registers to change the pass-through I2C/UART interface from I2C to UART.

Main UART

When the main I2C/UART is configured as UART, there are two operating modes: base and bypass.

UART Base Mode

Base mode is the means by which the microcontroller communicates with the serializer and deserializer where registers in these and peripheral devices can be accessed. Base mode is typically enabled by default at power-up. In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL2 UART packet protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings). The device addresses of the serializer and deserializer in this mode are programmable.

In base mode, the serializer, deserializer, and peripheral registers can be written and read using the half-duplex GMSL2 UART protocol. Base mode is enabled by default at power-up.

Figure 31 shows the UART protocol for writing and reading in base mode.

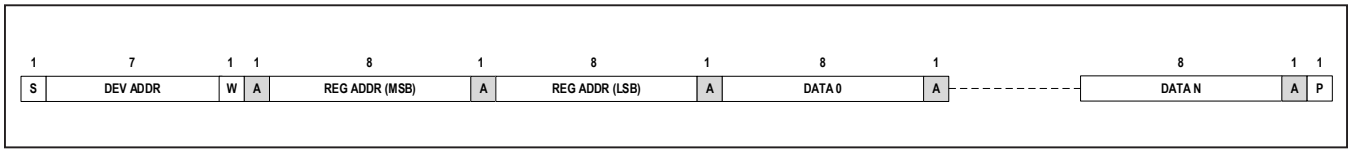

Figure 29. I2C Write Packet Format

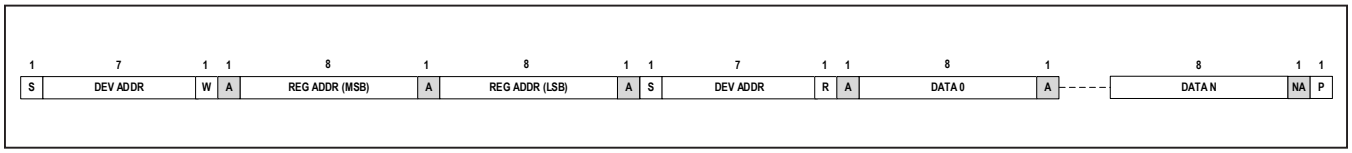

Figure 30. I2C Read Packet Format

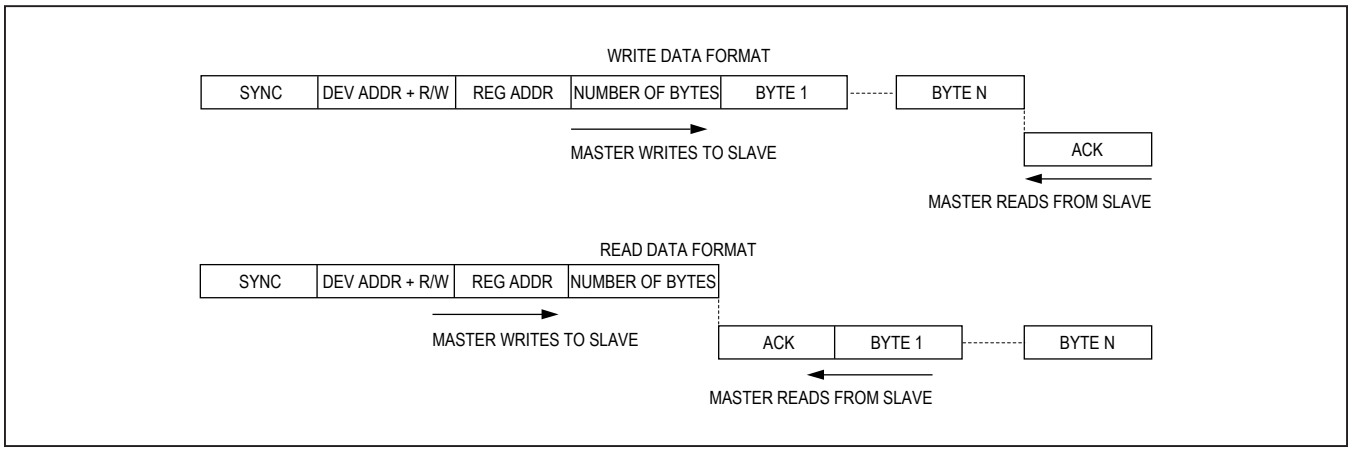

Figure 31. UART Protocol for Base Mode

UART Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the µC, and the µC communicates only with the peripherals using its own defined UART protocol. The µC cannot access the serializer/deserializer's registers in this mode. The UART transitions are simply sent over the GMSL link. Ignoring UART transactions prevents inadvertent misprogramming of serializer and deserializer registers. The device addresses of the serializer and deserializer in this mode are not programmable.

Switching between UART Base and Bypass Modes

There are two ways to switch between base mode and bypass mode: by register programming or by using the mode select (MS) pin.

Two modes can be set by programming: temporary or permanent. In temporary mode, bypass mode is active only as long as there is UART activity. When there is no UART activity for a selected timeout, both devices exit bypass mode and the bit is automatically cleared. In permanent mode, the devices stay in bypass mode until the next power down.

When set by the MS pin, a high level puts the device into bypass mode. A low level puts the device in base mode. MS is set on-the-fly and is not latched on power-up.

UART Frame Format

Regular UART frames with an even parity bit are used to carry one byte of data each. A frame consists of a low start bit followed by eight data bits, a parity bit, and a high stop bit. The parity bit is high if the number of ones in 8 bit data is odd, otherwise, it is low. There must be at least one high stop bit. If the next frame is in the same packet, there can be at most four high bits from the end of the stop bit to the beginning of the next start bit. When a parity bit error occurs, the packet, starting from the frame with the error, is discarded. The start of each frame is always a high-to-low transition (i.e., the stop bit is high and the start bit is low). The phase of the internal UART bit clock is adjusted using the start bit of each frame. The framer calibrates the length of one UART bit in terms of the internal oscillator clock using the synchronization frame (i.e., the first frame of a UART packet transmission). In bypass mode, the parity bit is enabled by default, but the frames are not checked for parity errors. Either even or odd parity can be used. The parity bit is passed along with UART data transmissions; the data recipient must perform error checking. The parity bit can optionally be disabled before entering bypass mode. Note that the bit rate in bypass mode must be the same bit rate last used in base mode.

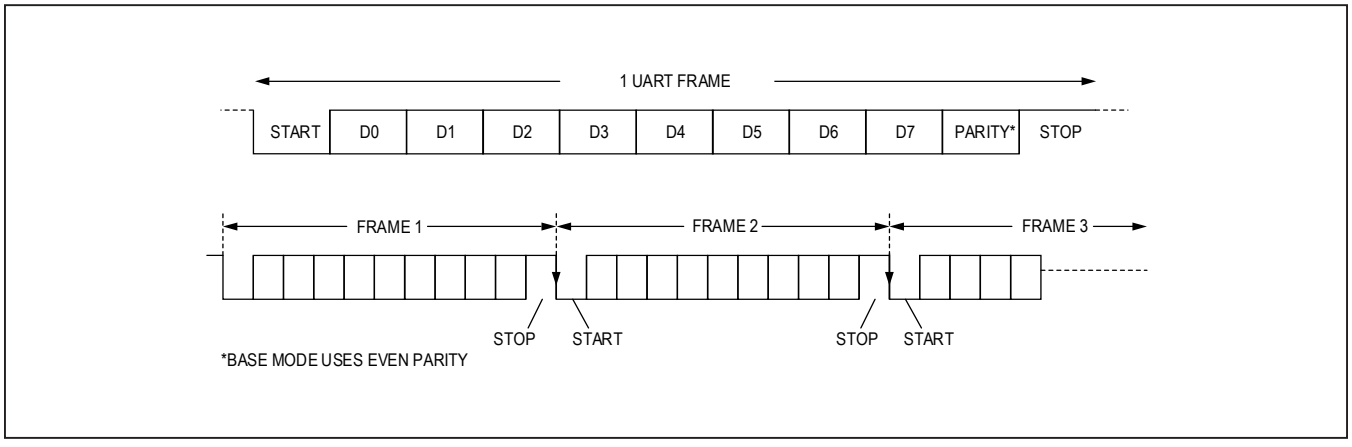

Figure 32. UART Data Format for Base Mode

Synchronization Frame

The serializer/deserializer must calibrate internal bit length counters with the UART bit rate for proper recovery of UART frames. The uC sends a sync frame (a regular UART frame with the value 0x79) as the first frame of each data packet. The sync frame allows the addressed device to calibrate bit lengths in terms of the device's internal 150 MHz clock. Sync frames must be properly detected before the subsequent frames of the packet can be correctly received. When the line stays high for at least 32 bits, the packet boundary is reset and the framer begins waiting for the next sync frame.

Acknowledge Frame

When a packet is successfully received, the addressed device responds with an acknowledge frame to inform the µC that no errors were detected in the transmitted packet. The acknowledge frame is sent after the last bit of the valid packet has been received. The acknowledge frame is a regular UART frame (value 0xC3). Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent.

Write Packet

A write packet consists of a five byte packet header followed by one or more data bytes. A packet is recognized as a write packet when the LSB of the device address frame is 0. The addressed device responds with an acknowledge frame if no errors were detected while receiving the packet. Byte Count indicates the number of data bytes to be written and this number cannot be zero.

See Figure 35.

Read Packet

A read packet consists of five bytes. The LSB of the device address frame is 1 for read packets. If no errors were detected while receiving a valid read packet, the addressed device responds with an acknowledge frame followed by one or more data bytes. Byte Count indicates the number of data bytes to be read and this number cannot be zero.

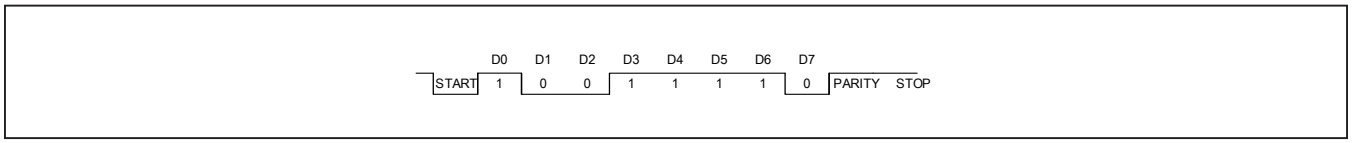

Figure 33. UART Synchronization Frame

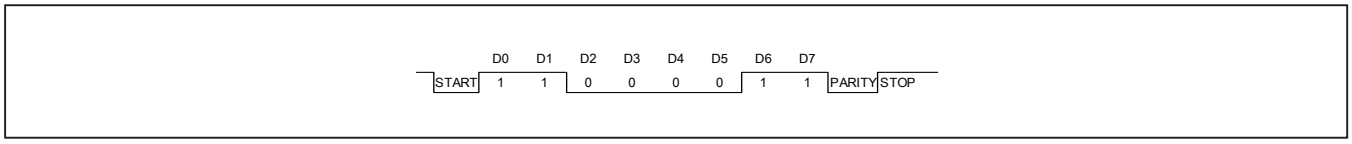

Figure 34. UART Acknowledge Frame

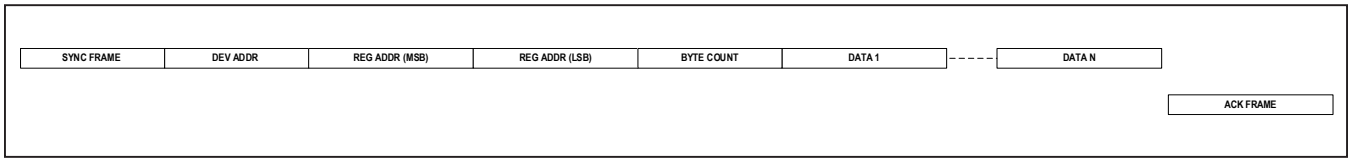

Figure 35. UART Write Packet Format

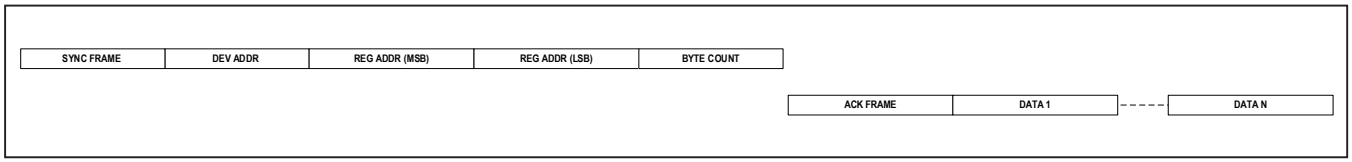

Figure 36. UART Read Packet Format

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX9296AGTM/V+	-40°C to +105°C	48 TQFN-EP	MAXIM
MAX9296AGTM/V+T	-40°C to +105°C	48 TQFN-EP	MAXIM
MAX9296AGTM/VY+	-40°C to +105°C	48 TQFN-SW-EP	MAXIM
MAX9296AGTM/VY+T	-40°C to +105°C	48 TQFN-SW-EP	MAXIM

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V Denotes an automotive qualified product.

Y Denotes wettable flank.

EP = Exposed pad.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/18	Initial release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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Appendix A: Register Map and Tables

Reserved, Unused, and Read-Only Register Bits

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and should not be modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits, and finally write the new byte to the register (Read/Replace/Write).

In this document, default values are provided for read-only register bits. Read-only bit states are changed at powerup according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

TABLE OF CONTENTS

Register Map

MAX9296A Dual 1 x 4 CSI-2 GMSL2/GMSL1 Deserializer

ADDRESS	NAME	MSB							LSB
DEV									
0x00	REG0[7:0]	DEV_ADDR[6:0]							CFG_BLOCK
0x01	REG1[7:0]	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
0x02	REG2[7:0]	VID_EN_U	VID_EN_Z	VID_EN_Y	VID_EN_X	–	–	–	–
0x03	REG3[7:0]	LOCK_CFG	PT_SWAP	UART_2_EN	UART_1_EN	–	–	–	–
0x05	REG5[7:0]	LOCK_EN	ERRB_EN	–	–	PU_LF3	PU_LF2	PU_LF1	PU_LF0
0x06	REG6[7:0]	–	–	–	I2CSEL	–	–	–	–
0x0D	REG13[7:0]	DEV_ID[7:0]							
0x0E	REG14[7:0]	–	–	–	–	DEV_REV[3:0]			
0x0F	REG15[7:0]	–	–	SPEED_CPBL[1:0]		DV_CPBL	DUAL_CPBL	SPLTR_CPBL	HDCP_CPBL
0x26	REG26[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		
0x27	REG27[7:0]	–	LF_3[2:0]			–	LF_2[2:0]		
OVERLAP									
TCTRL									
0x09	PWR1[7:0]	OVERTEMP	–	–	–	–	–	–	–
0x0C	PWR4[7:0]	–	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	–	–	–	–
0x10	CTRL0[7:0]	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	REG_ENABLE	LINK_CFG[1:0]	
0x11	CTRL1[7:0]	–	–	–	BACK_COMP_SPLTR	–	CXTP_B	–	CXTP_A
0x12	CTRL2[7:0]	IBLEED_OFF	–	–	REG_MNL	–	–	–	–
0x13	CTRL3[7:0]	–	–	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	–
0x18	INTR0[7:0]	–	–	–	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	INTR1[7:0]	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
0x1A	INTR2[7:0]	PHY_INT_OEN_	PHY_INT_OEN_	REM_ERR_OEN	MEM_INT_ERR_	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_	DEC_ERR_OEN_

ADDRESS	NAME	MSB							LSB
		B	A		OEN			B	A
0x1B	INTR3[7:0]	PHY_INT_B	PHY_INT_A	REM_ERR_FLAG	MEM_INT_ERR_FLAG	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x1C	INTR4[7:0]	EOM_ERR_OEN_B	EOM_ERR_OEN_A	–	–	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
0x1D	INTR5[7:0]	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	–	–	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
0x1E	INTR6[7:0]	VDDCMP_INT_OEN	PORZ_INT_OEN	VDDBAD_INT_OEN	FSYNC_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	–	VID_PXL_CRC_ERR_OEN
0x1F	INTR7[7:0]	VDDCMP_INT_FLAG	PORZ_INT_FLAG	VDDBAD_INT_FLAG	–	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	–	VID_PXL_CRC_ERR
0x20	INTR8[7:0]	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x21	INTR9[7:0]	ERR_RX_EN	ERR_RX_RECVED	–	ERR_RX_ID[4:0]				
0x22	CNT0[7:0]	DEC_ERR_A[7:0]							
0x23	CNT1[7:0]	DEC_ERR_B[7:0]							
0x24	CNT2[7:0]	IDLE_ERR[7:0]							
0x25	CNT3[7:0]	PKT_CNT[7:0]							
GMSL									
0x28	TX0[7:0]	–	–	–	–	–	–	–	–
0x2A	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2B	TX3[7:0]	–	–	–	–	–	TIMEOUT[2:0]		
0x2C	RX0[7:0]	PKT_CNT_LBW[1:0]		–	–	PKT_CNT_SEL[3:0]			
0x2F	RX3[7:0]	PRBS_SYNCED_B	SYNC_LOCKED_B	WBLOCK_B	FAILLOCK_B	PRBS_SYNCED_A	SYNC_LOCKED_A	WBLOCK_A	FAILLOCK_A
0x30	GPIOA[7:0]	GPIO_RX_FAST_BIDIR_EN	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
0x31	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
CC									
0x40	I2C_0[7:0]	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x41	I2C_1[7:0]	–	MST_BT[2:0]			–	MST_TO[2:0]		
0x42	I2C_2[7:0]	SRC_A[6:0]							–
0x43	I2C_3[7:0]	DST_A[6:0]							–
0x44	I2C_4[7:0]	SRC_B[6:0]							–

ADDRESS	NAME	MSB							LSB
0x45	I2C_5[7:0]	DST_B[6:0]							–
0x46	I2C_6[7:0]	–	–	–	–	I2C_AUTO_CFG	–	–	–
0x47	I2C_7[7:0]	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
0x48	UART_0[7:0]	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
0x49	UART_1[7:0]	BITLEN_LSB[7:0]							
0x4A	UART_2[7:0]	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
0x4C	I2C_PT_0[7:0]	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
0x4D	I2C_PT_1[7:0]	–	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
0x4E	I2C_PT_2[7:0]	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
0x4F	UART_PT_0[7:0]	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
CFGH VIDEO_X									
0x50	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGH VIDEO_Y									
0x51	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGH VIDEO_Z									
0x52	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGH VIDEO_U									
0x53	RX0[7:0]	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
CFGI INFOFR									
0x60	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x61	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x63	TR3[7:0]	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x64	TR4[7:0]	RX_SRC_SEL[7:0]							
CFGL SPI									
0x68	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x69	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x6B	TR3[7:0]	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		

ADDRESS	NAME	MSB							LSB
0x6C	TR4[7:0]	RX_SRC_SEL[7:0]							
0x6D	ARQ0[7:0]	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	EN	–	–	–
0x6E	ARQ1[7:0]	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x6F	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC CC									
0x70	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x71	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x73	TR3[7:0]	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x74	TR4[7:0]	RX_SRC_SEL[7:0]							
0x75	ARQ0[7:0]	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	EN	–	–	–
0x76	ARQ1[7:0]	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x77	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL GPIO									
0x78	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x79	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x7B	TR3[7:0]	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x7C	TR4[7:0]	RX_SRC_SEL[7:0]							
0x7D	ARQ0[7:0]	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	EN	–	–	–
0x7E	ARQ1[7:0]	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x7F	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC IIC_X									
0x80	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x81	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x83	TR3[7:0]	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x84	TR4[7:0]	RX_SRC_SEL[7:0]							
0x85	ARQ0[7:0]	ARQ_AU	ACK_CN	MATCH_	ACK_SR	EN	–	–	–

ADDRESS	NAME	MSB							LSB
		TO_CFG	T	SRC_ID	C_ID				
0x86	ARQ1[7:0]	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x87	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC IIC_Y									
0x88	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x89	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x8B	TR3[7:0]	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
0x8C	TR4[7:0]	RX_SRC_SEL[7:0]							
0x8D	ARQ0[7:0]	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	EN	–	–	–
0x8E	ARQ1[7:0]	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x8F	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
VID_RX X									
0x100	VIDEO_RX0[7:0]	LCRC_ERR	–	–	–	–	LINE_CRC_SEL	LINE_CRC_EN	DIS_PKT_DET
0x103	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x108	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	–	–	–	–
0x10A	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	–	–	–	–	–	–
0x10E	INFO_RX1[7:0]	SPEED_LIM[1:0]		–	–	–	–	–	–
VID_RX Y									
0x112	VIDEO_RX0[7:0]	LCRC_ERR	–	–	–	–	LINE_CRC_SEL	LINE_CRC_EN	DIS_PKT_DET
0x115	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x11A	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	–	–	–	–
0x11C	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	–	–	–	–	–	–
0x120	INFO_RX1[7:0]	SPEED_LIM[1:0]		–	–	–	–	–	–
VID_RX Z									
0x124	VIDEO_RX0[7:0]	LCRC_E	–	–	–	–	LINE_C	LINE_C	DIS_PKT

ADDRESS	NAME	MSB							LSB
		RR					RC_SEL	RC_EN	_DET
0x127	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x12C	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	–	–	–	–
0x12E	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	–	–	–	–	–	–
0x132	INFO_RX1[7:0]	SPEED_LIM[1:0]		–	–	–	–	–	–
VID_RX U									
0x136	VIDEO_RX0[7:0]	LCRC_ERR	–	–	–	–	LINE_CRC_SEL	LINE_CRC_EN	DIS_PKT_DET
0x139	VIDEO_RX3[7:0]	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
0x13E	VIDEO_RX8[7:0]	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	–	–	–	–
0x140	VIDEO_RX10[7:0]	–	MASK_VIDEO_DE	–	–	–	–	–	–
0x144	INFO_RX1[7:0]	SPEED_LIM[1:0]		–	–	–	–	–	–
SPI									
0x170	SPI_0[7:0]	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
0x171	SPI_1[7:0]	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
0x172	SPI_2[7:0]	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
0x173	SPI_3[7:0]	SPIM_SS_DLY_CLKS[7:0]							
0x174	SPI_4[7:0]	SPIM_SCK_LO_CLKS[7:0]							
0x175	SPI_5[7:0]	SPIM_SCK_HI_CLKS[7:0]							
0x176	SPI_6[7:0]	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
0x177	SPI_7[7:0]	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
0x178	SPI_8[7:0]	REQ_HOLD_OFF_TO[7:0]							
WM									
0x190	WM_0[7:0]	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
0x192	WM_2[7:0]	–	–	–	–	HsyncPol	VsyncPol	WM_NPFILT[1:0]	
0x193	WM_3[7:0]	–	WM_TH[6:0]						
0x194	WM_4[7:0]	–	–	WM_YUV_IN[1:0]		WM_COLORADJ	–	WM_MASKMODE[1:0]	

ADDRESS	NAME	MSB							LSB
0x195	WM_5[7:0]	–	–	–	–	–	–	WM_DETOUT	WM_ERROR
0x196	WM_6[7:0]	WM_TIMER[7:0]							
0x1AE	WM_WREN_0[7:0]	WM_WREN_L[7:0]							
0x1AF	WM_WREN_1[7:0]	WM_WREN_H[7:0]							
VRX X									
0x1C0	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1C1	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1C2	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1C3	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1C4	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1C5	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1C6	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x1C7	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1C8	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1C9	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x1CA	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1CB	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x1CC	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x1CD	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x1CE	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x1CF	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x1D0	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x1D1	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x1D2	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x1D3	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x1D4	CROSS_20[7:0]	–	CROSS2	CROSS2	CROSS20[4:0]				

ADDRESS	NAME	MSB							LSB
			0_I	0_F					
0x1D5	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x1D6	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x1D7	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x1D8	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x1D9	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x1DA	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x1DB	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1DC	VPRBS[7:0]	–	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
0x1DD	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x1DE	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x1DF	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX Y									
0x1E0	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x1E1	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x1E2	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x1E3	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x1E4	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x1E5	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x1E6	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x1E7	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x1E8	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x1E9	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x1EA	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x1EB	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				

ADDRESS	NAME	MSB							LSB
0x1EC	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x1ED	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x1EE	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x1EF	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x1F0	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x1F1	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x1F2	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x1F3	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x1F4	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x1F5	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x1F6	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x1F7	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x1F8	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x1F9	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x1FA	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x1FB	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1FC	VPRBS[7:0]	–	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
0x1FD	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x1FE	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x1FF	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX Z									
0x200	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x201	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x202	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x203	CROSS_3[7:0]	–	CROSS3	CROSS3	CROSS3[4:0]				

ADDRESS	NAME	MSB							LSB
			_I	_F					
0x204	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x205	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x206	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x207	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x208	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x209	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x20A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x20B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x20C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x20D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x20E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x20F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x210	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x211	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x212	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x213	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x214	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x215	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x216	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x217	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x218	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x219	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x21A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				

ADDRESS	NAME	MSB							LSB
0x21B	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x21C	VPRBS[7:0]	–	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
0x21D	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x21E	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x21F	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
VRX U									
0x220	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x221	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x222	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x223	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x224	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x225	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x226	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x227	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x228	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x229	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x22A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x22B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x22C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x22D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x22E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x22F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
0x230	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x231	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x232	CROSS_18[7:0]	–	CROSS1	CROSS1	CROSS18[4:0]				

ADDRESS	NAME	MSB							LSB
			8_I	8_F					
0x233	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x234	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x235	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x236	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x237	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x238	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x239	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x23A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x23B	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x23C	VPRBS[7:0]	–	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
0x23D	CROSS_27[7:0]	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
0x23E	CROSS_28[7:0]	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
0x23F	CROSS_29[7:0]	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
GPIO0 0									
0x2B0	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B1	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B2	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	–	GPIO_RX_ID[4:0]				
GPIO1 1									
0x2B3	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B4	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B5	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO2 2									
0x2B6	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2B7	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2B8	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				

ADDRESS	NAME	MSB							LSB
GPIO3 3									
0x2B9	GPIO_A[7:0]	RES_CFG	TX_PRIO	–	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BA	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2BB	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO4 4									
0x2BC	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BD	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	–	–	–	–	–
0x2BE	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO5 5									
0x2BF	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C0	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C1	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO6 6									
0x2C2	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C3	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C4	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO7 7									
0x2C5	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C6	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C7	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO8 8									
0x2C8	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C9	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CA	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO9 9									
0x2CB	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CC	GPIO_B[7:0]	PULL_UPDN_SEL[1		OUT_TY	GPIO_TX_ID[4:0]				

ADDRESS	NAME	MSB							LSB
		:0]		PE					
0x2CD	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO10 10									
0x2CE	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CF	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		–	GPIO_TX_ID[4:0]				
0x2D0	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO11 11									
0x2D1	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D2	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D3	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
GPIO12 12									
0x2D4	GPIO_A[7:0]	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D5	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D6	GPIO_C[7:0]	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
CMU									
0x304	CMU4[7:0]	A_SPEED[1:0]		B_SPEED[1:0]		–	–	C_SPEED[1:0]	
BACKTOP									
0x308	BACKTOP1[7:0]	CSIPLLU_LOCK	CSIPLLZ_LOCK	CSIPLLY_LOCK	CSIPLLX_LOCK	LINE_SPL2	LINE_SPL1	–	BACKTOP_EN
0x312	BACKTOP11[7:0]	cmd_overflow4	cmd_overflow3	cmd_overflow2	cmd_overflow1	–	LMO_Z	LMO_Y	–
0x313	BACKTOP12[7:0]	soft_bpp_x[4:0]					BACKTOP_MEM_CRC_ERR	CSI_OUT_EN	–
0x314	BACKTOP13[7:0]	soft_vc_y[3:0]				soft_vc_x[3:0]			
0x315	BACKTOP14[7:0]	soft_vc_u[3:0]				soft_vc_z[3:0]			
0x316	BACKTOP15[7:0]	soft_dt_y_h[1:0]		soft_dt_x[5:0]					
0x317	BACKTOP16[7:0]	soft_dt_z_h[3:0]				soft_dt_y_l[3:0]			
0x318	BACKTOP17[7:0]	soft_dt_u[5:0]						soft_dt_z_l[1:0]	
0x319	BACKTOP18[7:0]	soft_bpp_z_h[2:0]			soft_bpp_y[4:0]				
0x31A	BACKTOP19[7:0]	–	soft_bpp_u[4:0]					soft_bpp_z_l[1:0]	
0x31B	BACKTOP20[7:0]	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x31C	BACKTOP21[7:0]	bpp8dblu	bpp8dblz	bpp8dbly	bpp8dblx	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x31D	BACKTOP22[7:0]	override_	override_	phy0_csi	phy0_csi_tx_dpll_predef_freq[4:0]				

ADDRESS	NAME	MSB							LSB
		bpp_vc_dty	bpp_vc_dtx	_tx_dpll_fb_fraction_predef_en					
0x31E	BACKTOP23[7:0]	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x31F	BACKTOP24[7:0]	bpp8dblu_mode	bpp8dblz_mode	bpp8dbly_mode	bpp8dblx_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x320	BACKTOP25[7:0]	override_bpp_vc_dtu	override_bpp_vc_dtz	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
0x321	BACKTOP26[7:0]	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x322	BACKTOP27[7:0]	yuv_8_10_mux_mode4	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x323	BACKTOP28[7:0]	–	–	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				
0x324	BACKTOP29[7:0]	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x325	BACKTOP30[7:0]	BACKTOP_W_FRAME	–	–	–	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x326	BACKTOP31[7:0]	–	–	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
0x327	BACKTOP32[7:0]	bpp10dblu_mode	bpp10dblz_mode	bpp10dbly_mode	bpp10dblx_mode	bpp10dblu	bpp10dblz	bpp10dbly	bpp10dblx
0x328	BACKTOP33[7:0]	–	–	–	–	bpp12dblu	bpp12dblz	bpp12dbly	bpp12dblx
MIPI_PHY									
0x330	MIPI_PHY0[7:0]	force_csi_out_en	–	–	–	–	–	–	–
0x331	MIPI_PHY1[7:0]	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	
0x332	MIPI_PHY2[7:0]	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
0x333	MIPI_PHY3[7:0]	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
0x334	MIPI_PHY4[7:0]	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
0x335	MIPI_PHY5[7:0]	t_clk_prep[1:0]		phy1_pol_map[2:0]		phy0_pol_map[2:0]			
0x336	MIPI_PHY6[7:0]	phy_cp1	phy_cp0	phy3_pol_map[2:0]		phy2_pol_map[2:0]			
0x338	MIPI_PHY8[7:0]	t_lpxesc[2:0]			–	–	–	–	–
0x339	MIPI_PHY9[7:0]	phy_cp0_dst[1:0]		–	–	–	–	–	phy_cp0_overflow
0x33A	MIPI_PHY10[7:0]	phy_cp0_src[1:0]		–	–	–	–	–	phy_cp0

ADDRESS	NAME	MSB							LSB
									_underflow
0x33B	MIPI_PHY11[7:0]	phy_cp1_dst[1:0]		–	–	–	–	–	phy_cp1_overflow
0x33C	MIPI_PHY12[7:0]	phy_cp1_src[1:0]		–	–	–	–	–	phy_cp1_underflow
FSYNC									
0x3E0	FSYNC_0[7:0]	EN_OFLOW_RST_FS	–	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
0x3E1	FSYNC_1[7:0]	–	–	–	–	FSYNC_PER_DIV[3:0]			
0x3E2	FSYNC_2[7:0]	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]			
0x3E3	FSYNC_3[7:0]	P_VAL_L[7:0]							
0x3E4	FSYNC_4[7:0]	–	–	P_VAL_SIGN	P_VAL_H[4:0]				
0x3E5	FSYNC_5[7:0]	FSYNC_PERIOD_L[7:0]							
0x3E6	FSYNC_6[7:0]	FSYNC_PERIOD_M[7:0]							
0x3E7	FSYNC_7[7:0]	FSYNC_PERIOD_H[7:0]							
0x3E8	FSYNC_8[7:0]	FRM_DIFF_ERR_THR_L[7:0]							
0x3E9	FSYNC_9[7:0]	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
0x3EA	FSYNC_10[7:0]	OVLP_WINDOW_L[7:0]							
0x3EB	FSYNC_11[7:0]	EN_FSIN_LAST	–	–	OVLP_WINDOW_H[4:0]				
0x3F0	FSYNC_16[7:0]	FSYNC_ERR_CNT[7:0]							
0x3F1	FSYNC_17[7:0]	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
0x3F2	FSYNC_18[7:0]	CALC_FRM_LEN_L[7:0]							
0x3F3	FSYNC_19[7:0]	CALC_FRM_LEN_M[7:0]							
0x3F4	FSYNC_20[7:0]	CALC_FRM_LEN_H[7:0]							
0x3F5	FSYNC_21[7:0]	FRM_DIFF_L[7:0]							
0x3F6	FSYNC_22[7:0]	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
MIPI_TX 0									
0x40B	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x40C	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x40D	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x40E	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x40F	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x410	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x411	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x412	MIPI_TX18[7:0]	MAP_DST_2[7:0]							

ADDRESS	NAME	MSB							LSB
0x413	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x414	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x415	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x416	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x417	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x418	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x419	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x41A	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x41B	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x41C	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x41D	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x41E	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x41F	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x420	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x421	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x422	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x423	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x424	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x425	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x426	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x427	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x428	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x429	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x42A	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x42B	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x42C	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x42D	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x42E	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x42F	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x430	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x431	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x433	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
MIPI_TX 1									
0x441	MIPI_TX1[7:0]	MODE[7:0]							
0x442	MIPI_TX2[7:0]	STATUS[7:0]							
0x443	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							

ADDRESS	NAME	MSB							LSB
0x444	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x445	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x446	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x447	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x448	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x449	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x44A	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		–		–	CSI_VCX_EN	CSI2_TWAKEUP_H[2:0]	
0x44B	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x44C	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x44D	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x44E	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x44F	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x450	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x451	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x452	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x453	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x454	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x455	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x456	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x457	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x458	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x459	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x45A	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x45B	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x45C	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x45D	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x45E	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x45F	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x460	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x461	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x462	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x463	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x464	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x465	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x466	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x467	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x468	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x469	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x46A	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x46B	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							

ADDRESS	NAME	MSB							LSB
0x46C	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x46D	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x46E	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x46F	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x470	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x471	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x472	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x473	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
MIPI_TX 2									
0x481	MIPI_TX1[7:0]	MODE[7:0]							
0x482	MIPI_TX2[7:0]	STATUS[7:0]							
0x483	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x484	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x485	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x486	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x487	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x488	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x489	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x48A	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		–	–	CSI_VCX_EN	CSI2_TWAKEUP_H[2:0]		
0x48B	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x48C	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x48D	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x48E	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x48F	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x490	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x491	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x492	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x493	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x494	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x495	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x496	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x497	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x498	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x499	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x49A	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x49B	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							

ADDRESS	NAME	MSB							LSB
0x49C	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x49D	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x49E	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x49F	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x4A0	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x4A1	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x4A2	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x4A3	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x4A4	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x4A5	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x4A6	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x4A7	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x4A8	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x4A9	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x4AA	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x4AB	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x4AC	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x4AD	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x4AE	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x4AF	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x4B0	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x4B1	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x4B2	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x4B3	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
MIPI_TX 3									
0x4CB	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x4CC	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x4CD	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x4CE	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x4CF	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x4D0	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x4D1	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x4D2	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x4D3	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x4D4	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x4D5	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							

ADDRESS	NAME	MSB							LSB
0x4D6	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x4D7	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x4D8	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x4D9	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x4DA	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x4DB	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x4DC	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x4DD	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x4DE	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x4DF	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x4E0	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x4E1	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x4E2	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x4E3	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x4E4	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x4E5	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x4E6	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x4E7	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x4E8	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x4E9	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x4EA	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x4EB	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x4EC	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x4ED	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x4EE	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x4EF	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x4F0	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x4F1	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x4F3	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
MIPI_TX_EXT 0									
0x500	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x501	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x502	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x503	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x504	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x505	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–

ADDRESS	NAME	MSB							LSB
0x506	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x507	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x508	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x509	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x50A	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x50B	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x50C	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x50D	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x50E	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x50F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 1									
0x510	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x511	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x512	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x513	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x514	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x515	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x516	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x517	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x518	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x519	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x51A	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x51B	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x51C	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x51D	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x51E	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x51F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 2									
0x520	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x521	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x522	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x523	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x524	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x525	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x526	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x527	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x528	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x529	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x52A	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x52B	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x52C	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–

ADDRESS	NAME	MSB							LSB
0x52D	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x52E	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x52F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 3									
0x530	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x531	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x532	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x533	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x534	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x535	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x536	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x537	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x538	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x539	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x53A	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x53B	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x53C	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x53D	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x53E	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x53F	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MISC									
0x548	UART_PT_0[7:0]	BITLEN_PT_1_L[7:0]							
0x549	UART_PT_1[7:0]	–	–	BITLEN_PT_1_H[5:0]					
0x54A	UART_PT_2[7:0]	BITLEN_PT_2_L[7:0]							
0x54B	UART_PT_3[7:0]	–	–	BITLEN_PT_2_H[5:0]					
0x550	I2C_PT_4[7:0]	SRC_A_1[6:0]							–
0x551	I2C_PT_5[7:0]	DST_A_1[6:0]							–
0x552	I2C_PT_6[7:0]	SRC_B_1[6:0]							–
0x553	I2C_PT_7[7:0]	DST_B_1[6:0]							–
0x554	I2C_PT_8[7:0]	SRC_A_2[6:0]							–
0x555	I2C_PT_9[7:0]	DST_A_2[6:0]							–
0x557	I2C_PT_11[7:0]	DST_B_2[6:0]							–
0x559	BW_MEAS_0[7:0]	BW_USE_THR[7:0]							
0x55A	BW_MEAS_1[7:0]	–	–	–	–	BW_USE_OEN	BW_INT	BW_USE_LINK	BW_USE_LT
0x55C	CNT4[7:0]	VID_PXL_CRC_ERR0[7:0]							
0x55D	CNT5[7:0]	VID_PXL_CRC_ERR1[7:0]							
0x55E	CNT6[7:0]	VID_PXL_CRC_ERR2[7:0]							
0x55F	CNT7[7:0]	VID_PXL_CRC_ERR3[7:0]							
GMSL1 A									
0xB02	GMSL1_2[7:0]	–	–	–	–	–	–	SRNG[1:0]	

ADDRESS	NAME	MSB							LSB
0xB04	GMSL1_4[7:0]	–	OUTENB	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
0xB05	GMSL1_5[7:0]	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xB06	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xB07	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xB08	GMSL1_8[7:0]	–	–	GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xB0D	GMSL1_D[7:0]	I2C_LOC_ACK	–	–	–	–	HS_TRACK_FSYNC	–	–
0xB0E	GMSL1_E[7:0]	DET_THR[7:0]							
0xB0F	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xB10	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xB11	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xB12	GMSL1_12[7:0]	–	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xB13	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xB14	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xB15	GMSL1_15[7:0]	DET_ERR[7:0]							
0xB16	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xB17	GMSL1_17[7:0]	I2C_TIMED_OUT_GMSL1	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xB18	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xB19	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xB1A	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xB1B	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xB1C	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xB1D	GMSL1_1D[7:0]	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
0xB20	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xB21	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xB22	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							

ADDRESS	NAME	MSB							LSB
0xB23	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xB96	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					DIS_HIBW_E	CONV_GMSL1_EN	DBL_ALIGN_TO
0xBCA	GMSL1_CA[7:0]	–	–	–	–	–	PHASELOCK	WBLOCK_G1	DATAOK
0xBCB	GMSL1_CB[7:0]	–	–	–	–	–	–	–	LOCKED_G1
0xBD1	GMSL1_D1[7:0]	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
GMSL1 B									
0xC02	GMSL1_2[7:0]	–	–	–	–	–	–	SRNG[1:0]	
0xC04	GMSL1_4[7:0]	–	OUTENB	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
0xC05	GMSL1_5[7:0]	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xC06	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xC07	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xC08	GMSL1_8[7:0]	–	–	GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xC0D	GMSL1_D[7:0]	I2C_LOC_ACK	–	–	–	–	HS_TRACK_FSYNC	–	–
0xC0E	GMSL1_E[7:0]	DET_THR[7:0]							
0xC0F	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xC10	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xC11	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xC12	GMSL1_12[7:0]	–	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xC13	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xC14	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xC15	GMSL1_15[7:0]	DET_ERR[7:0]							
0xC16	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xC17	GMSL1_17[7:0]	I2C_TIMED_OUT_GMSL1	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xC18	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							

ADDRESS	NAME	MSB							LSB
0xC19	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xC1A	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xC1B	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xC1C	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xC1D	GMSL1_1D[7:0]	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
0xC20	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xC21	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xC22	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xC23	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xC96	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					DIS_HIBW_E	CONV_GMSL1_EN	DBL_ALIGN_TO
0xCCA	GMSL1_CA[7:0]	–	–	–	–	–	PHASELOCK	WBLOCK_G1	DATAOK
0xCD1	GMSL1_D1[7:0]	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
GMSL1_COMMON									
0xF00	GMSL1_EN[7:0]	–	–	–	–	–	–	LINK_EN_B	LINK_EN_A
0xF01	GMSL1_UART[7:0]	–	–	–	–	–	–	GMSL1_UART_ARB_TO	GMSL1_UART_ARB_EN
0xF02	COMMON1[7:0]	–	–	–	–	–	–	REM_ACK_ACKED_G1_B	REM_ACK_ACKED_G1_A
0xF03	GMSL1_ERR_OEN[7:0]	–	–	–	–	–	–	G1_B_ERR_OEN	G1_A_ERR_OEN
0xF04	GMSL1_ERR_FLAG[7:0]	–	–	–	–	–	–	G1_B_ERR_FLAG	G1_A_ERR_FLAG
0xF05	I2C_0[7:0]	–	–	G1_SLV_SH[1:0]		–	G1_SLV_TO[2:0]		
0xF06	I2C_1[7:0]	EN_I2C_LOOPBACK	G1_MST_BT[2:0]			–	G1_MST_TO[2:0]		
0xF07	I2C_2[7:0]	G1_SRC_A[6:0]							–
0xF08	I2C_3[7:0]	G1_DST_A[6:0]							–
0xF09	I2C_4[7:0]	G1_SRC_B[6:0]							–
0xF0A	I2C_5[7:0]	G1_DST_B[6:0]							–
SPI_CC_WR									
0x1300	SPI_CC_WR_[7:0]	–	–	–	–	–	–	–	–
SPI_CC_RD									
0x1380	SPI_CC_RD_[7:0]	–	–	–	–	–	–	–	–
RLMS A									

ADDRESS	NAME	MSB							LSB
0x1403	RLMS3[7:0]	AdaptEn	–	–	–	–	–	–	–
0x1404	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1405	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1406	RLMS6[7:0]	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1407	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1434	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1435	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1437	RLMS37[7:0]	–	–	–	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1439	RLMS39[7:0]	EyeMonErrCntH[7:0]							
0x143A	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x143B	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x143D	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x143E	RLMS3E[7:0]	ErrChPhSecTA	ErrChPhSec[6:0]						
0x143F	RLMS3F[7:0]	ErrChPhPriTA	ErrChPhPri[6:0]						
0x1458	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1459	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x145B	RLMS5B[7:0]	–	ErrChVTh[6:0]						
0x1464	RLMS64[7:0]	–	–	–	–	–	–	TxSSCMode[1:0]	
0x1470	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						
0x1471	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1472	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1473	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1475	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1476	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1495	RLMS95[7:0]	TxAmplManEn	–	TxAmplMan[5:0]					
0x14A4	RLMSA4[7:0]	AEQ_PER_MULT[1:0]	AEQ_PER[5:0]						
0x14AC	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
0x14AD	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						

ADDRESS	NAME	MSB							LSB
0x14AE	RLMSAE[7:0]	ErrChPhSecTAFR1G5	ErrChPhSecFR1G5[6:0]						
0x14AF	RLMSAF[7:0]	ErrChPhPriTAFR1G5	ErrChPhPriFR1G5[6:0]						
0x14B0	RLMSB0[7:0]	ErrChPhSecTASR1G5	ErrChPhSecSR1G5[6:0]						
0x14B1	RLMSB1[7:0]	ErrChPhPriTASR1G5	ErrChPhPriSR1G5[6:0]						
0x14B2	RLMSB2[7:0]	ErrChPhSecTASRG75	ErrChPhSecSRG75[6:0]						
0x14B3	RLMSB3[7:0]	ErrChPhPriTASRG75	ErrChPhPriSRG75[6:0]						
0x14B4	RLMSB4[7:0]	ErrChPhSecTASRG375	ErrChPhSecSRG375[6:0]						
0x14B5	RLMSB5[7:0]	ErrChPhPriTASRG375	ErrChPhPriSRG375[6:0]						
0x14B6	RLMSB6[7:0]	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
0x14B7	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
0x14C4	RLMSC4[7:0]	–	–	–	–	–	RevFast	–	–
RLMS B									
0x1503	RLMS3[7:0]	AdaptEn	–	–	–	–	–	–	–
0x1504	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1505	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1506	RLMS6[7:0]	EOM_PV_MODE	EOM_RST_THR[6:0]						
0x1507	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x1534	RLMS34[7:0]	EyeMonPerCntL[7:0]							
0x1535	RLMS35[7:0]	EyeMonPerCntH[7:0]							
0x1537	RLMS37[7:0]	–	–	–	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
0x1539	RLMS39[7:0]	EyeMonErrCntH[7:0]							

ADDRESS	NAME	MSB							LSB
0x153A	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x153B	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x153D	RLMS3D[7:0]	ErrChPh[6:0]							ErrChPhTogEn
0x153E	RLMS3E[7:0]	ErrChPhSecTA	ErrChPhSec[6:0]						
0x153F	RLMS3F[7:0]	ErrChPhPriTA	ErrChPhPri[6:0]						
0x1558	RLMS58[7:0]	–	ErrChVTh1[6:0]						
0x1559	RLMS59[7:0]	–	ErrChVTh0[6:0]						
0x155B	RLMS5B[7:0]	–	ErrChVTh[6:0]						
0x1564	RLMS64[7:0]	–	–	–	–	–	–	TxSSCMode[1:0]	
0x1570	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						
0x1571	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1572	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1573	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1574	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1575	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1576	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x1595	RLMS95[7:0]	TxAmplManEn	–	TxAmplMan[5:0]					
0x15A4	RLMSA4[7:0]	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
0x15AC	RLMSAC[7:0]	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
0x15AD	RLMSAD[7:0]	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
0x15AE	RLMSAE[7:0]	ErrChPhSecTAFR1G5	ErrChPhSecFR1G5[6:0]						
0x15AF	RLMSAF[7:0]	ErrChPhPriTAFR1G5	ErrChPhPriFR1G5[6:0]						
0x15B0	RLMSB0[7:0]	ErrChPhSecTASR1G5	ErrChPhSecSR1G5[6:0]						
0x15B1	RLMSB1[7:0]	ErrChPhPriTASR1G5	ErrChPhPriSR1G5[6:0]						
0x15B2	RLMSB2[7:0]	ErrChPhSecTASRG75	ErrChPhSecSRG75[6:0]						
0x15B3	RLMSB3[7:0]	ErrChPhPriTASR	ErrChPhPriSRG75[6:0]						

ADDRESS	NAME	MSB							LSB
		G75							
0x15B4	RLMSB4[7:0]	ErrChPhSecTASRG375	ErrChPhSecSRG375[6:0]						
0x15B5	RLMSB5[7:0]	ErrChPhPriTASRG375	ErrChPhPriSRG375[6:0]						
0x15B6	RLMSB6[7:0]	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
0x15B7	RLMSB7[7:0]	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
0x15C4	RLMSC4[7:0]	–	–	–	–	–	RevFast	–	–
DPLL CSI2									
0x1D03	DPLL_3[7:0]	–	–	–	–	–	config_spread_bit_ratio[2:0]		
DPLL CSI3									
0x1E03	DPLL_3[7:0]	–	–	–	–	–	config_spread_bit_ratio[2:0]		

Register Details

REG0 (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1001000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device I²C Address. Default address is specified by CFG0 pin as described in the device datas sheet.	0b0000000: I²C write/read address is 0x00/0x01 0b0000001: I²C write/read address is 0x02/0x03 .: . .: . 0b1001000: I²C write/read address is 0x90/0x91 0b1001010: I²C write/read address is 0x94/0x95 0b1001100: I²C write/read address is 0x98/0x99 0b1101000: I²C write/read address is 0xD0/0xD1 0b1101010: I²C write/read address is 0xD4/0xD5 0b1101100: I²C write/read address is 0xD8/0xD9 0b0101000: I²C write/read address is 0x50/0x51 0b0101010: I²C write/read address is 0x54/0x55 .: . .: . 0b1111111: I²C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block. When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration.	0b0: Not Blocked 0b1: Blocked

REG1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	IIC_2_EN	IIC_1_EN	DIS_LOCAL_CC	DIS_REM_CC	TX_RATE[1:0]		RX_RATE[1:0]	
Reset	0x0	0x0	0b0	0b0	0x0		0x2	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
IIC_2_EN	7	Enable pass-through I2C Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: I2C pass-through Channel 2 disabled 0b1: I2C pass-through Channel 2 enabled
IIC_1_EN	6	Enable pass-through I2C Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: I2C pass-through Channel 1 disabled 0b1: I2C pass-through Channel 1 enabled
DIS_LOCAL_CC	5	Disable control channel connection to RX/SDA and TX/SCL pins	0b0: RX/SDA and TX/XCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_CC	4	Disable remote control channel link over GMSL2 connection	0b0: Remote control channel enabled 0b1: Remote control channel disabled
TX_RATE	3:2	Transmitter rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE	1:0	Receiver rate (when changed, becomes active after next link reset) Default value is set by CXTP pin at power-up: 6Gbps when CXTP = 1 (Coax cable) and 3Gbps when CXTP = 0 (Twisted-pair cable)	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

REG2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	VID_EN_U	VID_EN_Z	VID_EN_Y	VID_EN_X	–	–	–	–
Reset	0b1	0b1	0b1	0b1	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_U	7	Video enable	0b0: Video transmit Channel U disabled 0b1: Video transmit Channel U enabled
VID_EN_Z	6	Video enable	0b0: Video transmit Channel Z disabled 0b1: Video transmit Channel Z enabled
VID_EN_Y	5	Video enable	0b0: Video transmit Channel Y disabled 0b1: Video transmit Channel Y enabled
VID_EN_X	4	Video enable	0b0: Video transmit Channel X disabled 0b1: Video transmit Channel X enabled

REG3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	LOCK_CFG	PT_SWAP	UART_2_EN	UART_1_EN	–	–	–	–
Reset	0b0	0x1	0b0	0b1	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_CFG	7	Configure LOCK pin behavior	0b0: GMSL2 link locked 0b1: GMSL2 link locked and MIPI output started
PT_SWAP	6	Swap I2C/UART pass-through device pin assignments.	0b0: Do not swap pin assignments 0b1: Swap pin assignments
UART_2_EN	5	Enable pass-through UART Channel 2 (SDA2/RX2, SCL2/TX2)	0b0: Pass-through UART Channel 2 disabled 0b1: Pass-through UART Channel 2 enabled
UART_1_EN	4	Enable pass-through UART Channel 1 (SDA1/RX1, SCL1/TX1)	0b0: Pass-through UART Channel 1 disabled 0b1: Pass-through UART Channel 1 enabled

REG5 (0x5)

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	–	–	PU_LF3	PU_LF2	PU_LF1	PU_LF0
Reset	0x1	0x1	–	–	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enable LOCK output	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enable ERRB output	0b0: ERRB output disabled 0b1: ERRB output enabled
PU_LF3	3	Power-up line fault monitor 3	0b0: Line fault monitor 3 disabled 0b1: Line fault monitor 3 enabled
PU_LF2	2	Power-up line fault monitor 2	0b0: Line fault monitor 2 disabled 0b1: Line fault monitor 2 enabled
PU_LF1	1	Power-up line fault monitor 1	0b0: Line fault monitor 1 disabled 0b1: Line fault monitor 1 enabled
PU_LF0	0	Power-up line fault monitor 0	0b0: Line fault monitor 0 disabled 0b1: Line fault monitor 0 enabled

REG6 (0x6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	I2CSEL	–	–	–	–
Reset	–	–	–	0b0	–	–	–	–
Access Type	–	–	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2CSEL	4	I2C / UART selection	0b0: UART

BITFIELD	BITS	DESCRIPTION	DECODE
		Bit is set according to the latched CFG0 pin value at power-up.	0b1: I²C

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0x90							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device identifier	0x94: MAX9296A

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DEV_REV[3:0]			
Reset	–	–	–	–	0x00			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device revision	0xX: Revision number

REG15 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SPEED_CPBL[1:0]		DV_CPBL	DUAL_CPBL	SPLTR_CPBL	HDCP_CPBL
Reset	–	–	0x0		0b0	0b0	0b0	0b0
Access Type	–	–	Read Only		Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPEED_CPBL	5:4	Video resolution capability	0b00: No PCLK frequency limit 0b01: PCLK is limited to 240MHz 0b10: PCLK is limited to 160MHz 0b11: PCLK is limited to 104MHz
DV_CPBL	3	Dual-view video capability	0b0: Dual-view video splitting is not available on this device 0b1: Dual-view video splitting is available on this device
DUAL_CPBL	2	Dual-link capability	0b0: Dual-link mode is not available on this device 0b1: Dual-link mode is available on this device
SPLTR_CPBL	1	Splitter mode capability	0b0: Splitter mode is not available on this device 0b1: Splitter mode is available on this device
HDCP_CPBL	0	HDCP capability	0b0: HDCP not enabled on this device 0b1: HDCP enabled on this device

REG26 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line fault status of wire connected to LMN1 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_0	2:0	Line fault status of wire connected to LMN0 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

REG27 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_3[2:0]			–	LF_2[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3	6:4	Line fault status of wire connected to LMN3 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short
LF_2	2:0	Line fault status of wire connected to LMN2 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal operation 0b011: Line open 0b1XX: Line-to-line short

PWR1 (0x9)

BIT	7	6	5	4	3	2	1	0
Field	OVERTEMP	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Read Only	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
OVERTEMP	7	Temperature monitor overtemp indicator. Trip temperature Ttrip set by SET_TEMP1P0[1:0] in CMU6	0x0: T < Ttrip 0x1: T > Ttrip

PWR4 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	–	DIS_LOCAL_WAKE	WAKE_EN_B	WAKE_EN_A	–	–	–	–
Reset	–	0b0	0b0	0b1	–	–	–	–
Access Type	–	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local µC from SDA_RX pin	0b0: Local wake-up disabled 0b1: Local wake-up enabled
WAKE_EN_B	5	Enable wake-up by remote chip connected to Link B	0b0: Link B remote wake-up disabled 0b1: Link B remote wake-up enabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to Link A	0b0: Link A remote wake-up disabled 0b1: Link A remote wake-up enabled

CTRL0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	AUTO_LINK	SLEEP	REG_ENABLE	LINK_CFG[1:0]	
Reset	0b0	0b0	0b0	0b1	0b0	0x0	0b01	
Access Type	Write, Read	Write, Read	Write Clears All, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Writing a 1 to this bit resets the device (including all blocks) and resets registers to their default values. This is equivalent to toggling the PWDNB pin. The bit self clears when written to.	0b0: No action 0b1: Activate chip reset
RESET_LINK	6	Reset whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT	5	Reset whole data path (keep register settings) one shot. Write 1 to activate reset, bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path
AUTO_LINK	4	Automatically select link configuration (single A, single B or dual). Splitter mode is not automatic. For splitter mode, set LINK_CFG = 0b11.	0b0: Disable automatic link configuration 0b1: Enable automatic link configuration
SLEEP	3	Activate sleep mode	0b0: Sleep mode disabled 0b1: Sleep mode enabled
REG_ENABLE	2	VDD LDO regulator enable	0b0: VDD LDO regulator disabled (bypassed) when REG_MNL=1 0b1: VDD LDO regulator enabled when REG_ENABLE=1 and REG_MNL=1. When VDD=1.2V, first set REG_ENABLE=1, and then write REG_MNL=1
LINK_CFG	1:0	In conjunction with AUTO_LINK, this bitfield selects the link configuration per the decode	0b00: If AUTO_LINK = 0, Dual link selected. If AUTO_LINK = 1, Link mode is automatically

BITFIELD	BITS	DESCRIPTION	DECODE
		table.	selected 0b01: If AUTO_LINK = 0, Link A is selected. If AUTO_LINK = 1, Link mode is automatically selected 0b10: If AUTO_LINK = 0, Link B is selected. If AUTO_LINK = 1, Link mode is automatically selected 0b11: Splitter mode

CTRL1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BACK_COMP_SPLTR	–	CXTP_B	–	CXTP_A
Reset	–	–	–	0x0	–	0b0	–	0b0
Access Type	–	–	–	Write, Read	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BACK_COMP_SPLTR	4	Enable splitter mode compatibility	0b0: Compatibility disabled 0b1: Compatibility enabled
CXTP_B	2	Coax/twisted-pair cable select for Link B Bit is set according to the latched CXTP pin value at power-up	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/twisted-pair cable select for Link A Bit is set according to the latched CXTP pin value at power-up	0b0: Shielded twisted-pair drive 0b1: Coax drive

CTRL2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	IBLEED_OFF	–	–	REG_MNL	–	–	–	–
Reset	0x0	–	–	0b0	–	–	–	–
Access Type	Write, Read	–	–	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
IBLEED_OFF	7	Turn off regulator bleeder current	0b0: Regulator bleeder current on 0b1: Regulator bleeder current off
REG_MNL	4	Enable regulator manual mode to allow regulator to be forced on or off via REG_ENABLE	0b0: Normal mode 0b1: Regulator manual mode

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	–	–	LINK_MODE[1:0]		LOCKED	ERROR	CMU_LOCKED	–
Reset	–	–	0x1		0b0	0b0	0b0	–
Access Type	–	–	Read Only		Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_MODE	5:4	Active link mode	0b00: Dual link 0b01: Link A 0b10: Link B 0b11: Splitter mode
LOCKED	3	GMSL2 link locked (bidirectional)	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock multiplier unit (CMU) locked	0b0: CMU not locked 0b1: CMU locked

INTR0 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	–	–	–	–	0b0	0x0		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A, DEC_ERR_B, and IDLE_ERR registers after ERRB pin is asserted for 1µs	0b0: Auto reset disabled 0b1: Auto reset enabled
DEC_ERR_THR	2:0	Decoding and idle error reporting threshold. DEC_ERR_FLAG_A is asserted when DEC_ERR_A ≥ DEC_ERR_THR. DEC_ERR_FLAG_B is asserted when DEC_ERR_B ≥ DEC_ERR_THR. IDLE_ERR_FLAG is asserted when IDLE_ERR ≥ DEC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

INTR1 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	PKT_CNT_THR[2:0]		
Reset	0x0				0b0	0x0		
Access Type	Write, Read				Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet count multiplier exponent. See the description of PKT_CNT bitfield (register CNT3).	0bXXX: PKT_CNT exponent
AUTO_CNT_RST_EN	3	Automatically reset PKT_CNT bitfield (register CNT3) after ERRB pin is asserted for 1µs	0b0: Auto reset disabled 0b1: Auto reset enabled
PKT_CNT_THR	2:0	Packet count reporting threshold. See PKT_CNT bitfield description (register CNT3). PKT_CNT_FLAG is asserted when PKT_CNT ≥ PKT_CNT_THR.	0b000: 1 packet 0b001: 2 packets 0b010: 4 packets 0b011: 8 packets 0b100: 16 packets 0b101: 32 packets 0b110: 64 packets 0b111: 128 packets

INTR2 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	PHY_INT_OEN_B	PHY_INT_OEN_A	REM_ERR_OEN	MEM_INT_ERR_OEN	LFLT_INT_OEN	IDLE_ERR_OEN	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0x0	0x1	0b0	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PHY_INT_OEN_B	7	Enable reporting of PHY interrupt (PHY_INT_B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PHY_INT_OEN_A	6	Enable reporting of PHY interrupt (PHY_INT_A) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
REM_ERR_OEN	5	Enable reporting of remote error status (REM_ERR) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MEM_INT_ERR_OEN	4	Enable memory error status reporting on ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LFLT_INT_OEN	3	Enable reporting of line fault interrupt (LFLT_INT) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enable reporting of idle word errors (IDLE_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_B	1	Enable reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enable reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	PHY_INT_B	PHY_INT_A	REM_ERR_FLAG	MEM_INT_ERR_FLAG	LFLT_INT	IDLE_ERR_FLAG	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0x0	0x0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PHY_INT_B	7	PHY Interrupt of Link B. See registers I2C_PT_0 (0x4C), I2C_PT_1 (0x4D), I2C_PT_2 (0x4E), and UART_PT_0 (0x4F).	0b0: No Link B PHY interrupt 0b1: Link B PHY interrupt
PHY_INT_A	6	PHY Interrupt of Link A. See registers I2C_PT_0 (0x4C), I2C_PT_1 (0x4D), I2C_PT_2 (0x4E), and UART_PT_0 (0x4F).	0b0: No Link A PHY interrupt 0b1: Link A PHY interrupt
REM_ERR_FLAG	5	Received remote side error status (inverse of remote side ERRB pin level)	0b0: No remote side error 0b1: Remote side error
MEM_INT_ERR_FLAG	4	Memory error flag	0x0: No memory error occurred 0x1: Memory error occurred
LFLT_INT	3	Line fault interrupt. Asserted when either of the line fault monitors indicates a fault status. See bitfields LF_0 and LF_1 in REG26 (0x26) for details.	0b0: No line fault 0b1: Line fault
IDLE_ERR_FLAG	2	Idle word error flag. Asserted when IDLE_ERR ≥ DEC_ERR_THR	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_B	1	Decoding error flag for Link B. Asserted when DEC_ERR_B ≥ DEC_ERR_THR	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	Decoding error flag for Link A. Asserted when DEC_ERR_A ≥ DEC_ERR_THR	0b0: Flag not asserted 0b1: Flag asserted

INTR4 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_OEN_B	EOM_ERR_OEN_A	–	–	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	WM_ERR_OEN
Reset	0b0	0b0	–	–	0b1	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_B	7	Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_B) for Link B at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
EOM_ERR_OEN_A	6	Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enable reporting of packet count flag (PKT_CNT_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
WM_ERR_OEN	0	Enable reporting of watermark errors (WM_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	–	–	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	WM_ERR_FLAG
Reset	0b0	0b0	–	–	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	–	–	Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_B	7	Eye-opening is below configured threshold for Link B	0b0: No EOM error on Link B 0b1: EOM error on Link B
EOM_ERR_FLAG_A	6	Eye-opening is below configured threshold for Link A	0b0: No EOM error on Link A 0b1: EOM error on Link A
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag. Asserted when any of the selected channels ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ retransmission event flag. Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN register bit.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet count flag. Asserted when PKT_CNT ≥ PKT_CNT_THR	0b0: Flag not asserted 0b1: Flag asserted
WM_ERR_FLAG	0	Watermark error flag. Asserted when a watermark error is detected	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	PORZ_INT_OEN	VDDBAD_INT_OEN	FSYNC_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	–	VID_PXL_CRC_ERR_OEN
Reset	0b0	0b0	0b0	0b1	0b1	0b1	–	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_OEN	7	Enable reporting of VDDCMP interrupt (VDDCMP_INT_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PORZ_INT_OEN	6	Enable reporting of PORZ interrupt (PORZ_INT_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VDDBAD_INT_OEN	5	Enable reporting of VDDBAD interrupt (VDDBAD_INT_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
FSYNC_ERR_OEN	4	Enable reporting of frame sync errors (FSYNC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
LCRC_ERR_OEN	3	Enable reporting of video line CRC errors (LCRC_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
VPRBS_ERR_OEN	2	Enable reporting of video PRBS errors (VPRBS_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_OEN	0	Video pixel CRC error counter interrupt output enable	0x0: Error counter interrupt output not enabled 0x1: Error counter interrupt output enabled

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	PORZ_INT_FLAG	VDDBAD_INT_FLAG	–	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	–	VID_PXL_CRC_ERR
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0x0
Access Type	Read Only	Read Only	Read Only	–	Read Only	Read Only	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VDDCMP_INT_FLAG	7	VDDCMP interrupt flag	0b0: Flag not asserted 0b1: Flag asserted
PORZ_INT_FLAG	6	PORZ interrupt flag	0b0: Flag not asserted 0b1: Flag asserted
VDDBAD_INT_FLAG	5	VDD STATUS interrupt	0b0: Flag not asserted 0b1: Flag asserted
LCRC_ERR_FLAG	3	Video line CRC error flag, asserted when a video line CRC error is detected	0b0: Flag not asserted 0b1: Flag asserted
VPRBS_ERR_FLAG	2	Video PRBS error flag, asserted when VPRBS_ERR > 0	0b0: Flag not asserted 0b1: Flag asserted
VID_PXL_CRC_ERR	0	Video pixel CRC error counter interrupt	0x0: Error counter interrupt output not enabled 0x1: Error counter interrupt output enabled

INTR8 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b1	–	–	0x1F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmit local error status (inverse of ERRB pin level) to remote side through GPIO channel	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

INTR9 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	ERR_RX_RECVED	–	ERR_RX_ID[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Received remote error status (inverse of ERRB pin level) through GPIO channel	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_RECVED	6	Received ERR_RX value	0b0: ERR_RX value not received 0b1: ERR_RX value received
ERR_RX_ID	4:0	GPIO ID used for receiving ERR_RX	0bXXXXX: Value of GPIO ID for receiving ERR_TX

CNT0 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of decoding (disparity) errors detected at Link A. Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

CNT1 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_B	7:0	Number of decoding (disparity) errors detected at Link B. Resets after reading or with the rising edge of LOCK.	0xXX: Number of Link B decoding errors detected

CNT2 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle word errors detected.	0xXX: Number of idle word errors detected

BITFIELD	BITS	DESCRIPTION	DECODE
		Reset after reading or with the rising edge of LOCK.	

CNT3 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type. Packet type is selected with PKT_CNT_SEL register. Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT\_CNT\_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT\_CNT\_EXP}$). When max value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

TX2 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024
ERRG_RATE	5:4	Error generator average bit error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits
ERRG_BURST	3:1	Error generator burst error length	0b000: 1 error 0b001: 2 errors 0b010: 3 errors 0b011: 4 errors 0b100: 8 errors 0b101: 12 errors 0b110: 16 errors 0b111: 20 errors
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TIMEOUT[2:0]		
Reset	–	–	–	–	–	0b100		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	ARQ timeout duration multiplier. Multiplies a timeout base constant to set the ARQ timeout. The timeout base is set by the reverse channel link rate (RX_RATE) as follows: RX_RATE Timeout Base 187.5Mbps 8µs	0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base

RX0 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	–	PKT_CNT_SEL[3:0]			
Reset	0b00		–	–	0x0			
Access Type	Write, Read		–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Selects the sub-type of low-bandwidth packets to count at PKT_CNT bitfield in register CNT3 (0x25)	0b00: Count LBW data packets only 0b01: Count LBW acknowledge packets only 0b10: Count LBW data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT bitfield in register CNT3 (0x25). The selected packet type must be supported by the device.	0x0: None 0x1: VIDEO 0x2: AUDIO 0x3: INFO Frame 0x4: SPI 0x5: I^2C 0x6: UART 0x7: GPIO 0x8: AHDCP 0x9: RGMII 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All 0xF: Unknown and packets with error

RX3 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_SYNCED_B	SYNC_LOCKED_B	WBLOCK_B	FAILLOCK_B	PRBS_SYNCED_A	SYNC_LOCKED_A	WBLOCK_A	FAILLOCK_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Clears All	Read Only	Read Only	Read Only	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_SYNCED_B	7	Link PRBS is synced to incoming data (Link B)	0b0: Link PRBS not synced to incoming data 0b1: Link PRBS synced to incoming data
SYNC_LOCKED_B	6	Sync tracking locked (Link B)	0b0: Sync tracking is not locked 0b1: Sync tracking is locked
WBLOCK_B	5	Word boundary locked (Link B)	0b0: Word boundary not locked 0b1: Word boundary locked
FAILLOCK_B	4	Failed word boundary lock (latched) (Link B)	0b0: Word boundary lock did not fail 0b1: Word boundary lock failed
PRBS_SYNCED_A	3	Link PRBS is synced to incoming data	0b0: Link PRBS not synced to incoming data 0b1: Link PRBS synced to incoming data
SYNC_LOCKED_A	2	Sync tracking locked (Link A)	0b0: Sync tracking is not locked 0b1: Sync tracking is locked
WBLOCK_A	1	Word boundary locked (Link A)	0b0: Word boundary not locked 0b1: Word boundary locked
FAILLOCK_A	0	Failed word boundary lock (latched) (Link A)	0b0: Word boundary lock did not fail 0b1: Word boundary lock failed

GPIOA (0x30)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_RX_FAST_BIDIR_EN	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0b1	0b000001					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_FAST_BIDIR_EN	7	GPIO fast direction switch for bidirectional IO	0b0: Fast direction switch disabled 0b1: Fast direction switch enabled
GPIO_TX_CASC	6	Allow multiple pin transitions to be transmitted in the same packet	0b0: Multiple pin transitions not allowed 0b1: Multiple pin transitions allowed
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x31)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b001000					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time to create a packet after a GPIO transition. This allows different GPIO input transitions to be grouped into a single packet, thereby increasing GPIO bandwidth efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

I2C_0 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I²C-to-I²C master bit rate setting. Configures the I²C bit rate used by the internal I²C master (in the device on remote side from the external I²C master) Set this according to the I²C speed mode.	0b00: Set for I²C Fast-mode Plus speed 0b01: Set for I²C Fast-mode speed 0b10: Set for I²C Standard-mode speed 0b11: Reserved
SLV_TO	2:0	I²C-to-I²C slave timeout setting. Internal GMSL2 I²C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	–	0x5			–	0x6		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I²C-to-I²C master bit rate setting. Configures the I²C bit rate used by the internal I²C master (in the device on remote side from the external I²C master) Set this according to the I²C speed mode.	0b000: 9.92Kbps - Set for I²C Standard-mode speed 0b001: 33.2Kbps - Set for I²C Standard-mode speed 0b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO	2:0	I²C-to-I²C master timeout setting. Internal GMSL2 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I²C address translator source A. When I²C device address matches I²C SRC_A, internal I²C master (on remote side) replaces the device address by I²C DST_A	0bXXXXXXX: Value of I²C SRC_A

I2C_3 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I²C address translator destination A. See the description of I²C SRC_A bitfield in register I2C_2 (0x42).	0bXXXXXXX: Value of I²C DST_A

I2C_4 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I^2C address translator source B. When I^2C device address matches I^2C SRC_B, internal I^2C master (on remote side) replaces the device address by I^2C DST_B	0bXXXXXXX: Value of I^2C SRC_B

I2C_5 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I^2C address translator destination B. See the description of I^2C SRC_B bitfield in register I2C_4 (0x44).	0bXXXXXXX: Value of I^2C DST_B

I2C_6 (0x46)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2C_AUTO_CFG	–	–	–
Reset	–	–	–	–	0x1	–	–	–
Access Type	–	–	–	–	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_AUTO_CFG	3	When set to 1, I^2C-to-I^2C number of links is determined based on splitter mode automatically. In splitter mode, response from two I^2C channels are expected, otherwise response from one I^2C channel is expected.	0b0: Number of I^2C-to-I^2C links set by I2C_SRC_CNT[2:0] bits 0b1: Splitter mode automatically determines the number of I^2C-to-I^2C links

I2C_7 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	UART_RX_OVERFLOW	UART_TX_OVERFLOW	–	–	–	I2C_TIMED_OUT	REM_ACK_ACKED	REM_ACK_RECVED
Reset	0x0	0x0	–	–	–	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
UART_RX_OVERFLOW	7	UART Rx FIFO overflow	0b0: No overflow occurred 0b1: Overflow occurred
UART_TX_OVERFLOW	6	UART Tx FIFO overflow	0b0: No overflow occurred 0b1: Overflow occurred
I2C_TIMED_OUT	2	Internal I²C-to-I²C slave or master has timed out while receiving packet from remote device	0b0: Timeout has not occurred 0b1: Timeout has occurred
REM_ACK_ACKED	1	Inverse of the I²C acknowledge bit received from remote side	0b0: I²C acknowledge bit received as 1 0b1: I²C acknowledge bit received as 0
REM_ACK_RECVED	0	I²C acknowledge bit for any I²C byte is received from remote side for the previous I²C packet.	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

UART_0 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	ARB_TO_LEN[1:0]		REM_MS_EN	LOC_MS_EN	BYPASS_DIS_PAR	BYPASS_TO[1:0]		BYPASS_EN
Reset	0x1		0x0	0x0	0x0	0x1		0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ARB_TO_LEN	7:6	UART Rx source arbitration timeout duration. UART Rx processes packets from a single UART source at a time. If UART RX receives no UART packages during the specified duration, it selects the next UART source..	0b00: 1ms 0b01: 2ms 0b10: 8ms 0b11: 32ms
REM_MS_EN	5	Enables UART bypass mode control by remote GPIO pin. When set, remote chip's GPIO is used as MS pin (UART Mode Select). When MS is high, chip is in bypass mode, otherwise chip is in base mode.	0b0: UART bypass mode not controlled by remote MS pin 0b1: UART bypass mode controlled by remote MS pin
LOC_MS_EN	4	Enables UART bypass mode control by local GPIO pin. Set to use GPIO2 pin as MS pin (UART Mode Select). When MS is high, chip is in bypass mode, otherwise chip is in base mode.	0b0: UART bypass mode not controlled by local MS pin 0b1: UART bypass mode controlled by local MS pin
BYPASS_DIS_PAR	3	Selects whether to receive and send parity bit in bypass mode	0b0: Receive and send parity bit in bypass mode 0b1: Do not receive and send parity bit in bypass mode
BYPASS_TO	2:1	UART soft bypass timeout duration. When set to 0b11, BYPASS_EN is never cleared, so the device stays in bypass mode until next power down.	0b00: 2ms 0b01: 8ms 0b10: 32ms 0b11: Disabled
BYPASS_EN	0	Enables UART soft bypass mode. Bypass mode remains active as long as there is UART activity. When there is no UART activity for selected duration (configured by BYPASS_TO register), device exits bypass mode and the bit is automatically cleared.	0b0: UART soft bypass mode disabled 0b1: UART soft bypass mode enabled

UART_1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_LSB[7:0]							
Reset	0x96							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_LSB	7:0	UART detected bit length, low 8 bits	0xXX: UART detected bit length (lower 8 bits)

UART_2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	OUT_DELAY[1:0]		BITLEN_MSB[5:0]					
Reset	0x2		0x0					
Access Type	Write, Read		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
OUT_DELAY	7:6	UART initial output delay. In base mode. The first received UART byte of a packet (sync or acknowledge frame) is delayed by the configured number of bit times in order to output the UART frames of the same packet back to back on remote side.	0b00: 0 bits 0b01: 4 bits 0b10: 8 bits 0b11: 1 bit
BITLEN_MSB	5:0	UART detected bit length, high 6 bits	0bXXXXXX: UART detected bit length (upper 6 bits)

I2C_PT_0 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_PT[1:0]		–	SLV_TO_PT[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_PT	5:4	Pass-through I^2C-to-I^2C slave setup and hold time setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I^2C slave. Set this according to the I^2C speed mode:	0b00: Set for I^2C Fast-mode Plus speed 0b01: Set for I^2C Fast-mode speed 0b10: Set for I^2C Standard-mode speed 0b11: Reserved
SLV_TO_PT	2:0	Pass-through I^2C-to-I^2C slave timeout setting. Internal GMSL2 I^2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_PT_1 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	–	MST_BT_PT[2:0]			–	MST_TO_PT[2:0]		
Reset	–	0x5			–	0x6		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_PT	6:4	Pass-through I²C-to-I²C master bit rate setting. Configures the I²C bit rate used by the internal I²C master (in the device on remote side from the external I²C master). Set this according to the I²C speed mode.	0b000: 9.92Kbps - Set for I²C Standard-mode speed 0b001: 33.2Kbps - Set for I²C Standard-mode speed 0b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO_PT	2:0	Pass-through I²C-to-I²C master timeout setting. Internal GMSL2 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_PT_2 (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	XOVER_EN_2	I2C_TIMED_OUT_2	REM_ACK_ACKED_2	REM_ACK_RECVED_2	XOVER_EN_1	I2C_TIMED_OUT_1	REM_ACK_ACKED_1	REM_ACK_RECVED_1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Only	Read Only	Read Only	Write, Read	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
XOVER_EN_2	7	Connects pass-through I²C/UART Channel 2 to main control channel on remote side	0x0: Do not connect pass-through I²C/UART Channel 2 to main control channel 0x1: Connect pass-through I²C/UART Channel 2 to main control channel
I2C_TIMED_OUT_2	6	In pass-through I²C Channel 2, internal I²C-to-I²C slave or master has timed out while receiving packet from remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED_2	5	In pass-through I²C Channel 2, inverse of the I²C acknowledge bit received from remote side	0x0: I²C acknowledge bit received as 1 0x1: Inverse I²C acknowledge bit received as 0
REM_ACK_RECVED_2	4	In pass-through I²C Channel 2, I²C acknowledge bit for any I²C byte is received	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

BITFIELD	BITS	DESCRIPTION	DECODE
		from remote side for the previous I²C packet.	
XOVER_EN_1	3	Connects pass-through I²C/UART Channel 1 to main control channel on remote side	0x0: Do not connect pass-through I²C/UART Channel 1 to main control channel 0x1: Connect pass-through I²C/UART Channel 1 to main control channel
I2C_TIMED_OUT_1	2	In pass-through I²C Channel 1, internal I²C-to-I²C slave or master has timed out while receiving packet from remote device	0x0: Timeout has not occurred 0x1: Timeout has occurred
REM_ACK_ACKED_1	1	In pass-through I²C Channel 1, inverse of the I²C acknowledge bit received from remote side.	0x0: I²C acknowledge bit received as 1 0x1: Inverse I²C acknowledge bit received as 0
REM_ACK_RECVED_1	0	In pass-through I²C Channel 1, I²C acknowledge bit for any I²C byte is received from remote side for the previous I²C packet.	0b0: I²C acknowledge bit not received 0b1: I²C acknowledge bit received

UART_PT_0 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_MAN_CFG_2	DIS_PAR_2	UART_RX_OVERFLOW_2	UART_TX_OVERFLOW_2	BITLEN_MAN_CFG_1	DIS_PAR_1	UART_RX_OVERFLOW_1	UART_TX_OVERFLOW_1
Reset	0b1	0b0	0b0	0b0	0b1	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Read Clears All	Read Clears All	Write, Read	Write, Read	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_MAN_CFG_2	7	Uses the custom UART bit rate (selected by the BITLEN_PT_2_L and BITLEN_PT_2_H registers) in pass-through UART Channel 1	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_2	6	Disables parity bit in pass-through UART Channel 2	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_2	5	Pass-through UART Rx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred
UART_TX_OVERFLOW_2	4	Pass-through UART Tx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred
BITLEN_MAN_CFG_1	3	Uses the custom UART bit rate (selected by the BITLEN_PT_1_L and BITLEN_PT_1_H registers) in pass-through UART Channel 1	0b0: Use standard bit rate 0b1: Use custom bit rate
DIS_PAR_1	2	Disables parity bit in pass-through UART Channel 1	0b0: Parity bit enabled 0b1: Parity bit disabled
UART_RX_OVERFLOW_1	1	Pass-through UART Rx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred
UART_TX_OVERFLOW_1	0	Pass-through UART Tx FIFO overflow	0x0: No overflow occurred 0x1: Overflow occurred

RX0 (0x50)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0x0	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	Receive packet CRC enable	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Receive packets with selected stream ID	0bXX: Receive packets with this stream ID

RX0 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0x1	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	Receive packet CRC enable	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Receive packets with selected stream ID	0bXX: Receive packets with this stream ID

RX0 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0x2	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	Receive packet CRC enable	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Receive packets with selected stream ID	0bXX: Receive packets with this stream ID

RX0 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN	–	–	–	–	–	STR_SEL[1:0]	
Reset	0b0	–	–	–	–	–	0x3	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN	7	Receive packet CRC enable	0b0: No CRC on received packets 0b1: Received packets have CRC and checking is enabled
STR_SEL	1:0	Receive packets with selected stream ID	0bXX: Receive packets with this stream ID

TR0 (0x60, 0x68, 0x78)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	–	–	0x0		0x0	
Access Type	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjust the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[3:2] setting

TR1 (0x61, 0x69, 0x71, 0x79, 0x81, 0x89)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/ 10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base bandwidth value

TR3 (0x63, 0x6B, 0x73, 0x7B, 0x83, 0x8B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	TX_SPLT_MASK_B	TX_SPLT_MASK_A	–	TX_SRC_ID[2:0]		
Reset	–	–	0x1	0x1	–	0x0		
Access Type	–	–	Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SPLT_MASK_B	5	In splitter mode: When 0, packets from this port are NOT transmitted from port B, otherwise packets are transmitted from port B.	0b0: Packets are not transmitted over GMSLB in splitter mode 0b1: Packets are transmitted over GMSLB in splitter mode
TX_SPLT_MASK_A	4	In splitter mode: When 0, packets from this port are NOT transmitted from port A, otherwise packets are transmitted from port A.	0b0: Packets are not transmitted over GMSLA in splitter mode 0b1: Packets are transmitted over GMSLA in splitter mode
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default values of the two MSBs are set by the CFG pins. Default value of the LSB is 0.	0bXXX: Source ID for packets from this channel

TR4 (0x64, 0x6C, 0x74, 0x7C, 0x84, 0x8C)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received . . 0xFF: Packets from all source IDs received

ARQ0 (0x6D, 0x75, 0x7D, 0x85, 0x8D)

BIT	7	6	5	4	3	2	1	0
Field	ARQ_AUTO_CFG	ACK_CNT	MATCH_SRC_ID	ACK_SRC_ID	EN	–	–	–
Reset	0b1	0b0	0b0	0b1	0b1	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ_AUTO_CFG	7	When this bit = 1, ARQ settings are automatically selected based on splitter mode.	0b0: ARQ settings are based on selections in ACK_SRC_ID and MATCH_SRC_ID bitfields 0b1: ARQ settings are automatically selected
ACK_CNT	6	When ARQ_AUTO_CFG = 0, this bit selects whether to wait for one acknowledge packet or two acknowledge packets for each transmitted data packet.	0b0: Wait for one acknowledge packet 0b1: Wait for two acknowledge packets
MATCH_SRC_ID	5	Acknowledge packet source ID checking method	0: All received acknowledge packets are accepted 1: Acknowledge packet is accepted if SRC_ID of the received acknowledge packet matches TX_SRC_ID register
ACK_SRC_ID	4	Selects what to use as SRC_ID in transmitted acknowledge packets	0: Use SRC_ID of the received data packet 1: Use TX_SRC_ID register
EN	3	Enables ARQ	0b0: ARQ disabled 0b1: ARQ enabled

ARQ1 (0x6E, 0x76, 0x7E, 0x86, 0x8E)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			–	–	0b1	0b0
Access Type	–	Write, Read			–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ will stop retransmitting after this many attempts for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ max retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin	0b0: ARQ max retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ max retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x6F, 0x77, 0x7F, 0x87, 0x8F)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

TR0 (0x70, 0x80, 0x88)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	–	–	PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	–	–	0x0		0x0	
Access Type	Write, Read	Write, Read	–	–	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority used for this channel	0b00: Current channel priority is used 0b01: Increase current channel priority 0b10: Decrease current channel priority 0b11: Reset to channel PRIO_VAL[3:2] setting

VIDEO_RX0 (0x100, 0x112, 0x124, 0x136)

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	–	–	–	–	LINE_CRC_SEL	LINE_CRC_EN	DIS_PKT_DET
Reset	0x0	–	–	–	–	0b0	0b1	0b0
Access Type	Read Clears All	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video line CRC error flag	0b0: No video line CRC detected 0b1: Video line CRC detected
LINE_CRC_SEL	2	Line CRC trigger selection	0b0: Use DE 0b1: Use HS

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_EN	1	Video line CRC enable	0b0: Video line CRC disabled 0b1: Video line CRC enabled
DIS_PKT_DET	0	Disable packet detector. If the video is restarted with a different BPP when the packet detector is disabled, toggle this register or the video receive enable register to make sure the video link restarts	0b0: Packet detector enabled 0b1: Packet detector disabled

VIDEO_RX3 (0x103, 0x115, 0x127, 0x139)

BIT	7	6	5	4	3	2	1	0
Field	–	HD_TR_MODE	DLOCKED	VLOCKED	HLOCKED	DTRACKEN	VTRACKEN	HTRACKEN
Reset	–	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HD_TR_MODE	6	HS, DE tracking enable full periodic pattern	0b0: Allow only partial periodic HS, DE 0b1: Allow partial periodic and full periodic HS, DE
DLOCKED	5	DE tracking locked	0b0: DE tracking not locked 0b1: DE tracking locked
VLOCKED	4	VS tracking locked	0b0: VS tracking not locked 0b1: VS tracking locked
HLOCKED	3	HS tracking locked	0b0: HS tracking not locked 0b1: HS tracking locked
DTRACKEN	2	DE tracking enable (Disable if FSYNC = 1). The system observes DE pulses and, when it locks on the pattern, compensates for a limited number of missing pulses or suppress glitches.	0b0: DE tracking disabled 0b1: DE tracking enabled
VTRACKEN	1	VS tracking enable (Disable if FSYNC = 1). The system observes VS pulses and, when it locks on the pattern, compensates for a limited number of missing pulses or suppress glitches.	0b0: VS tracking disabled 0b1: VS tracking enabled
HTRACKEN	0	HS tracking enable (Disable if FSYNC = 1). The system observes HS pulses and, when it locks on the pattern, compensates for a limited number of missing pulses or suppress glitches.	0b0: HS tracking disabled 0b1: HSYNC tracking enabled

VIDEO_RX8 (0x108, 0x11A, 0x12C, 0x13E)

BIT	7	6	5	4	3	2	1	0
Field	VID_BLK_LEN_ERR	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	–	–	–	–
Reset	0b0	0b0	0b0	0b0	–	–	–	–
Access Type	Read Clears All	Read Only	Read Only	Read Clears All	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VID_BLK_LEN_ERR	7	Video Rx block length error detected	0b0: No error detected 0b1: Video Rx block length error detected
VID_LOCK	6	Video pipeline locked	0b0: Video pipeline not locked 0b1: Video pipeline locked
VID_PKT_DET	5	Sufficient video Rx packet throughput detected	0b0: Not enough throughput 0b1: Sufficient throughput detected
VID_SEQ_ERR	4	Video Rx sequence error happened	0b0: No error detected 0b1: Error detected

VIDEO_RX10 (0x10A, 0x11C, 0x12E, 0x140)

BIT	7	6	5	4	3	2	1	0
Field	–	MASK_VIDEO_DE	–	–	–	–	–	–
Reset	–	0x0	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MASK_VIDEO_DE	6	Mask video with DE	0x0: Do not mask video with DE 0x1: Mask video with DE

INFO_RX1 (0x10E, 0x120, 0x132, 0x144)

BIT	7	6	5	4	3	2	1	0
Field	SPEED_LIM[1:0]		–	–	–	–	–	–
Reset	0x0		–	–	–	–	–	–
Access Type	Read Only		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
SPEED_LIM	7:6	Received speed limitation

SPI_0 (0x170)

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_ID[1:0]		SPI_CC_TRG_ID[1:0]		SPI_IGNR_ID	SPI_CC_EN	MST_SLVN	SPI_EN
Reset	0x0		0x0		0x1	0x0	0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_ID	7:6	Program to local ID if filtering packets based on header ID	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3
SPI_CC_TRG_ID	5:4	ID for GMSL2 header in SPI control channel bridge mode	0b00: ID = 0 0b01: ID = 1 0b10: ID = 2 0b11: ID = 3

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_IGNR_ID	3	Selects if SPI should use or ignore header ID to decide on packet acceptance	0b0: Accept only packets with proper ID 0b1: Ignore ID and accept all packets
SPI_CC_EN	2	Enables control channel SPI bridge function	0b0: SPI bridge disabled 0b1: SPI bridge enabled
MST_SLVN	1	Selects if SPI is master or slave	0b0: SPI slave 0b1: SPI master
SPI_EN	0	Enables SPI channel	0b0: SPI channel disabled 0b1: SPI channel enabled

SPI_1 (0x171)

BIT	7	6	5	4	3	2	1	0
Field	SPI_LOC_N[5:0]						SPI_BASE_PRIO[1:0]	
Reset	0x07						0x1	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_LOC_N	7:2	Sets the packet size ((2N + 1) bytes) for GMSL2 SPI packets. If this is programmed to a value greater than 7, ARQ of the SPI channel must be disabled.	0b000000: Packet size is 1 byte 0b000001: Packet size is 3 bytes . . 0b111111: Packet size is 127 bytes
SPI_BASE_PRIO	1:0	Starting GMSL2 request priority advances by 1 (capacity permitting) if Tx buffer is over half full.	0b00: Priority 0 (low) 0b01: Priority 1 0b10: Priority 2 0b11: Priority 3

SPI_2 (0x172)

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF[2:0]			FULL_SCK_SETUP	SPI_MOD3_F	SPI_MOD3	SPIM_SS2_ACT_H	SPIM_SS1_ACT_H
Reset	0x0			0x0	0x0	0x0	0x1	0x1
Access Type	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF	7:5	Holds off GMSL2 request until this number of extra bytes are received on SPI port	0b00: No extra bytes 0b01: 1 extra byte 0b10: 2 extra bytes 0b11: 3 extra bytes
FULL_SCK_SETUP	4	Samples MISO after half or full SCK period	0b0: MISO sampled after half-SCK period 0b1: MISO sampled after full-SCK period
SPI_MOD3_F	3	Allows the supression of an extra SCK prior to SS deassertion when SPI mode 3 is selected	0b0: Extra SCK present prior to SS deassertion when in SPI mode 3 0b1: Extra SCK suppressed prior to SS deassertion when in SPI mode 3
SPI_MOD3	2	Selects SPI mode 0 or 3	0b0: SPI mode 0 0b1: SPI mode 3
SPIM_SS2_	1	Sets the polarity for SS2 when the SPI is a	0b0: Slave select 2 is active low

BITFIELD	BITS	DESCRIPTION	DECODE
ACT_H		master	0b1: Slave select 2 is active high
SPIM_SS1_ACT_H	0	Sets the polarity for SS1 when the SPI is a master	0b0: Slave select 1 is active low 0b1: Slave select 1 is active high

SPI_3 (0x173)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SS_DLY_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SS_DLY_CLKS	7:0	Number of 300MHz clocks to delay between: 1) Assertion of SS and start of SCK pulses 2) End of SCK pulses and deassertion of SS 3) Deassertion of SS and reassertion of SS (if necessary)	0xXX: Number of clock delays

SPI_4 (0x174)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_LO_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_LO_CLKS	7:0	Number of 300MHz clocks for SCK low time	0xXX: Number of clocks for SCK low time

SPI_5 (0x175)

BIT	7	6	5	4	3	2	1	0
Field	SPIM_SCK_HI_CLKS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SPIM_SCK_HI_CLKS	7:0	Number of 300MHz clocks for SCK high time	0xXX: Number of clocks for SCK high time

SPI_6 (0x176)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BNE	SPIS_RWN	SS_IO_EN_2	SS_IO_EN_1	BNE_IO_EN	RWN_IO_EN
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BNE	5	Alternates GPU status register to use for BNE status if GPIO is not avaiable	0b0: Buffer empty 0b1: Buffer not empty
SPIS_RWN	4	Alternates GPU control register to use for Rd/WrN control if GPIO is not available.	0b0: Write 0b1: Read
SS_IO_EN_2	3	Enables GPIO for use as slave select 2 output	0b0: GPIO not used for SPI SS2 function 0b1: GPIO used for SPI SS2 function
SS_IO_EN_1	2	Enables GPIO for use as slave select 1 output	0b0: GPIO not used for SPI SS1 function 0b1: GPIO used for SPI SS1 function
BNE_IO_EN	1	Enables GPIO for use as BNE output for SPI data available status	0b0: GPIO not used for SPI BNE function 0b1: GPIO used for SPI BNE function
RWN_IO_EN	0	Enables GPIO for use as RO input for control of SPI data movement	0b0: GPIO not used for SPI RO function 0b1: GPIO used for SPI RO function

SPI_7 (0x177)

BIT	7	6	5	4	3	2	1	0
Field	SPI_RX_OVRFLW	SPI_TX_OVRFLW	–	SPIS_BYTE_CNT[4:0]				
Reset	0b0	0b0	–	0x0				
Access Type	Read Clears All	Read Clears All	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
SPI_RX_OVRFLW	7	SPI Rx buffer overflow flag	0b0: No SPI Rx buffer overflow 0b1: SPI Rx buffer overflow
SPI_TX_OVRFLW	6	SPI Tx buffer overflow flag	0b0: No SPI Tx buffer overflow 0b1: SPI Tx buffer overflow
SPIS_BYTE_CNT	4:0	Number of SPI data bytes available for reading from Rx buffer.	0bXXXXX: Number of bytes available

SPI_8 (0x178)

BIT	7	6	5	4	3	2	1	0
Field	REQ_HOLD_OFF_TO[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
REQ_HOLD_OFF_TO	7:0	Timeout delay (in 100nS increments) for GMSL2 request hold off (0 is disable).	0xXX: Number of 100nS delay increments for GMSL2 request hold off

WM_0 (0x190)

BIT	7	6	5	4	3	2	1	0
Field	WM_LEN	WM_MODE[2:0]			WM_DET[1:0]		–	WM_EN
Reset	0x0	0x0			0x0		–	0x0
Access Type	Write, Read	Write, Read			Write, Read		–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WM_LEN	7	Watermark length	0b0: 32-bit 0b1: 63-bit
WM_MODE	6:4	Watermark mode	0b000: Insert WM-/WM+ every frame, temporal dither enabled 0b001: Reserved 0b010: Insert WM0/WM1 every frame, temporal dither enabled, polarity disabled (Error generation mode) 0b011: Insert WM0/WM1 every frame, do not reset WM, temporal dither enabled 0b100: Insert WM0/WM1 every frame, temporal dither disabled 0b101: Reserved 0b110: Reserved 0b111: Reserved
WM_DET	3:2	Watermark detection/generation	0b00: Insert watermark in video stream 0b01: Detect watermark and remove from outgoing video stream 0b10: Reserved 0b11: Reserved
WM_EN	0	Watermark enable	0b0: Watermarking disabled 0b1: Watermarking enabled

WM_2 (0x192)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HsyncPol	VsyncPol	WM_NPFILT[1:0]	
Reset	–	–	–	–	0b0	0b0	0x0	
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
HsyncPol	3	HS polarity	0b0: Non-inverting 0x1: Invert
VsyncPol	2	VS polarity	0b0: Non-inverting 0x1: Invert
WM_NPFILT	1:0	Phase accumulator terminal count	0bXX: Phase accumulator terminal count

WM_3 (0x193)

BIT	7	6	5	4	3	2	1	0
Field	–	WM_TH[6:0]						
Reset	–	0x14						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TH	6:0	Matched filter threshold	0bXXXXXXX: Matched filter threshold

WM_4 (0x194)

BIT	7	6	5	4	3	2	1	0
Field	–	–	WM_YUV_IN[1:0]		WM_COLORADJ	–	WM_MASKMODE[1:0]	
Reset	–	–	0x1		0x0	–	0x0	
Access Type	–	–	Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
WM_YUV_IN	5:4	Input color format	0b0: RGB 8-bit color data 0b1: YUV444 8-bits each
WM_COLORADJ	3	Color adjust	0b0: Masked off LSBs of U. Use if temporal dithering is enabled. 0b1: Set U[Ko:0] = 1/2 WM gain. Use this mode if temporal dithering is disabled
WM_MASKMODE	1:0	Sets watermark mask for the device	0b00: Mask if WM is detected 0b01: Mask if WM is detected, blank if error is detected 0b10: Reserved b011: Reserved

WM_5 (0x195)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	WM_DETOUT	WM_ERROR
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
WM_DETOUT	1	Live frame-based detection output	0b0: Watermark not detected 0b1: Watermark detected
WM_ERROR	0	Live active-high watermark error	0b0: No watermark error 0b1: Watermark error active, bit automatically clears when error clears.

WM_6 (0x196)

BIT	7	6	5	4	3	2	1	0
Field	WM_TIMER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_TIMER	7:0	Time in 2 msec steps the frozen frame condition must be observed before an error is generated. 0 = No filter	0xXX: Number of milliseconds

WM_WREN_0 (0x1AE)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_L	7:0	Writes 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise watermark registers are read only.	0xBA: Enables writing to WM registers Others: WM registers remain read only

WM_WREN_1 (0x1AF)

BIT	7	6	5	4	3	2	1	0
Field	WM_WREN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
WM_WREN_H	7:0	Writes 0xBA to WM_WREN_L and 0xDC to WM_WREN_H registers to enable writing to watermark registers. Otherwise watermark registers are read only.	0xDC: Enables writing to WM registers Others: WM registers remain read only

CROSS_0 (0x1C0, 0x1E0, 0x200, 0x220)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0x0	0x0	0x00				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS0_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

CROSS_1 (0x1C1, 0x1E1, 0x201, 0x221)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0x0	0x0	0x01				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1	0bXXXXX: Incoming bit position

CROSS_2 (0x1C2, 0x1E2, 0x202, 0x222)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0x0	0x0	0x02				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2	0bXXXXX: Incoming bit position

CROSS_3 (0x1C3, 0x1E3, 0x203, 0x223)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0x0	0x0	0x03				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3	0bXXXXX: Incoming bit position

CROSS_4 (0x1C4, 0x1E4, 0x204, 0x224)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0x0	0x0	0x04				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4	0bXXXXX: Incoming bit position

CROSS_5 (0x1C5, 0x1E5, 0x205, 0x225)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0x0	0x0	0x05				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5	0bXXXXX: Incoming bit position

CROSS_6 (0x1C6, 0x1E6, 0x206, 0x226)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0x0	0x0	0x06				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6	0bXXXXX: Incoming bit position

CROSS_7 (0x1C7, 0x1E7, 0x207, 0x227)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0x0	0x0	0x07				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7	0bXXXXX: Incoming bit position

CROSS_8 (0x1C8, 0x1E8, 0x208, 0x228)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0x0	0x0	0x08				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8	0bXXXXX: Incoming bit position

CROSS_9 (0x1C9, 0x1E9, 0x209, 0x229)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0x0	0x0	0x09				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9	0bXXXXX: Incoming bit position

CROSS_10 (0x1CA, 0x1EA, 0x20A, 0x22A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0x0	0x0	0x0A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS10	4:0	Maps incoming bit position set by this field to	0bXXXXX: Incoming bit position

BITFIELD	BITS	DESCRIPTION	DECODE
		the outgoing bit position 10	

CROSS_11 (0x1CB, 0x1EB, 0x20B, 0x22B)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0x0	0x0	0x0B				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11	0bXXXXX: Incoming bit position

CROSS_12 (0x1CC, 0x1EC, 0x20C, 0x22C)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0x0	0x0	0x0C				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12	0bXXXXX: Incoming bit position

CROSS_13 (0x1CD, 0x1ED, 0x20D, 0x22D)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0x0	0x0	0x0D				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13	0bXXXXX: Incoming bit position

CROSS_14 (0x1CE, 0x1EE, 0x20E, 0x22E)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0x0	0x0	0x0E				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14	0bXXXXX: Incoming bit position

CROSS_15 (0x1CF, 0x1EF, 0x20F, 0x22F)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0x0	0x0	0x0F				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15	0bXXXXX: Incoming bit position

CROSS_16 (0x1D0, 0x1F0, 0x210, 0x230)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0x0	0x0	0x10				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16	0bXXXXX: Incoming bit position

CROSS_17 (0x1D1, 0x1F1, 0x211, 0x231)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0x0	0x0	0x11				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17	0bXXXXX: Incoming bit position

CROSS_18 (0x1D2, 0x1F2, 0x212, 0x232)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0x0	0x0	0x12				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS18_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18	0bXXXXX: Incoming bit position

CROSS_19 (0x1D3, 0x1F3, 0x213, 0x233)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0x0	0x0	0x13				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19	0bXXXXX: Incoming bit position

CROSS_20 (0x1D4, 0x1F4, 0x214, 0x234)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0x0	0x0	0x14				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20	0bXXXXX: Incoming bit position

CROSS_21 (0x1D5, 0x1F5, 0x215, 0x235)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0x0	0x0	0x15				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21	0bXXXXX: Incoming bit position

CROSS_22 (0x1D6, 0x1F6, 0x216, 0x236)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0x0	0x0	0x16				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22	0bXXXXX: Incoming bit position

CROSS_23 (0x1D7, 0x1F7, 0x217, 0x237)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0x0	0x0	0x17				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23	0bXXXXX: Incoming bit position

CROSS_HS (0x1D8, 0x1F8, 0x218, 0x238)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
Reset	–	0x0	0x0	0x18				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_HS_I	6	Inverts CROSS_HS	0b0: Do not invert bit 0b1: Invert bit
CROSS_HS_F	5	Forces CROSS_HS to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_HS	4:0	Maps selected internal signal to HS	0bXXXXX: Incoming bit position

CROSS_VS (0x1D9, 0x1F9, 0x219, 0x239)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
Reset	–	0x0	0x0	0x19				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_VS_I	6	Inverts CROSS_VS	0b0: Do not invert bit 0b1: Invert bit
CROSS_VS_F	5	Forces CROSS_VS to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_VS	4:0	Maps selected internal signal to VS	0bXXXXX: Incoming bit position

CROSS_DE (0x1DA, 0x1FA, 0x21A, 0x23A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
Reset	–	0x0	0x0	0x1A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_DE_I	6	Inverts CROSS_DE	0b0: Do not invert bit 0b1: Invert bit
CROSS_DE_F	5	Forces Cross_DE to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_DE	4:0	Maps selected internal signal to DE	0bXXXXX: Incoming bit position

PRBS_ERR (0x1DB, 0x1FB, 0x21B, 0x23B)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERR	7:0	Video PRBS error counter. Clears on read.	0xXX: Number of video PRBS errors since last read

VPRBS (0x1DC, 0x1FC, 0x21C, 0x23C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VPRBS_FAIL	VPRBS_CHK_EN	–	–	–	VIDEO_LOCK
Reset	–	–	0b0	0b0	–	–	–	0b0
Access Type	–	–	Read Only	Write, Read	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_FAIL	5	Video PRBS check pass/fail	0b0: Video PRBS check passed 0b1: Video check failed
VPRBS_CHK_EN	4	Enables video PRBS checker	0b0: Video PRBS checker disabled 0b1: Video PRBS checker enabled
VIDEO_LOCK	0	Video channel is locked and outputting valid video data	0b0: Video channel not locked 0b1: Video channel locked

CROSS_27 (0x1DD, 0x1FD, 0x21D, 0x23D)

BIT	7	6	5	4	3	2	1	0
Field	ALT_CROSSBAR	CROSS27_I	CROSS27_F	CROSS27[4:0]				
Reset	0b0	0b0	0b0	0b11011				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_CROSSBAR	7	Selects whether to use the crossbar in the VRX block or the alternative crossbar in the RDP	0x0: Use crossbar in VRX block 0x1: Use crossbar in RDP
CROSS27_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS27_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS27	4:0	Maps selected internal signal to CrossX	0bXXXXX: Incoming bit position

CROSS_28 (0x1DE, 0x1FE, 0x21E, 0x23E)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS28_I	CROSS28_F	CROSS28[4:0]				
Reset	–	0b0	0b0	0b11100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS28_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS28_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS28	4:0	Maps selected internal signal to CrossX	0bXXXXX: Incoming bit position

CROSS_29 (0x1DF, 0x1FF, 0x21F, 0x23F)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS29_I	CROSS29_F	CROSS29[4:0]				
Reset	–	0b0	0b0	0b11101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS29_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS29_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS29	4:0	Maps selected internal signal to CrossX	0bXXXXX: Incoming bit position

GPIO_A (0x2B0)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2B1)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x00				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2B2)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	–	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	–	0x00				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B3)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2B4)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x01				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2B5)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x01				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, res_cfg and pull_updn_sel are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B6)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2B7)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x02				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2B8)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x02				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2B9)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	–	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	–	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	–	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2BA)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x03				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2BB)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x03				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2BC)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2BD)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	–	–	–	–	–
Reset	0x2		0b1	–	–	–	–	–
Access Type	Write, Read		Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull

GPIO_C (0x2BE)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x04				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2BF)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0

BITFIELD	BITS	DESCRIPTION	DECODE
			0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C0)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x05				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C1)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x05				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, res_cfg and pull_updn_sel are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C2)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C3)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x06				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C4)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x06				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C5)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C6)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x07				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C7)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x07				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C8)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C9)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x08				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2CA)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x08				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2CB)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2CC)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x09				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2CD)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x09				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2CE)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2CF)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		–	GPIO_TX_ID[4:0]				
Reset	0x2		–	0x0A				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D0)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x0A				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D1)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D2)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x0B				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D3)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x0B				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D4)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	TX_PRIO	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_PRIO	6	Priority for GPIO scheduling	0b0: Low priority 0b1: High priority
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Disables GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D5)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x0C				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D6)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	–	–	GPIO_RX_ID[4:0]				
Reset	0x0	–	–	0x0C				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Overrides non-GPIO port function IO setting. When set, RES_CFG and PULL_UPDN_SEL are effective when pin is configured as non GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

CMU4 (0x304)

BIT	7	6	5	4	3	2	1	0
Field	A_SPEED[1:0]		B_SPEED[1:0]		–	–	C_SPEED[1:0]	
Reset	0x2		0x3		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
A_SPEED	7:6	Control A_SPEED group edge rate. First value is for VDDIO = 1.8V, second value is for VDDIO = 3.3V	0x0: 2ns, 1ns 0x1: 4ns, 2ns 0x2: 8ns, 4ns 0x3: 16ns, 8ns
B_SPEED	5:4	Control B_SPEED group edge rate. First value is for VDDIO = 1.8V, second value is for VDDIO = 3.3V	0x0: 2ns, 1ns 0x1: 4ns, 2ns 0x2: 8ns, 4ns 0x3: 16ns, 8ns
C_SPEED	1:0	Control C_SPEED group edge rate. First value is for VDDIO = 1.8V, second value is for VDDIO = 3.3V	0x0: 2ns, 1ns 0x1: 4ns, 2ns 0x2: 8ns, 4ns 0x3: 16ns, 8ns

BACKTOP1 (0x308)

BIT	7	6	5	4	3	2	1	0
Field	CSIPLLU_LOCK	CSIPLLZ_LOCK	CSIPLLY_LOCK	CSIPLLX_LOCK	LINE_SPL2	LINE_SPL1	–	BACKTOP_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	–	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLLU_LOCK	7	CSI U PLL locked	0b0: CSI2 U PLL not locked 0b1: CSI2 U PLL locked

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLLZ_LOCK	6	CSI Z PLL locked	0b0: CSI2 Z PLL not locked 0b1: CSI2 Z PLL locked
CSIPLLY_LOCK	5	CSI Y PLL locked	0b0: CSI2 Y PLL not locked 0b1: CSI2 Y PLL locked
CSIPLLX_LOCK	4	CSI X PLL locked	0b0: CSI2 X PLL not locked 0b1: CSI2 X PLL locked
LINE_SPL2	3	Line-based distribution to line memories for Video Pipe Z	0b0: Disable line-based distribution to line memories for Video Pipe Z 0b1: Enable line-based distribution to line memories for Video Pipe Z
LINE_SPL1	2	Line-based distribution to line memories for Video Pipe X	0b0: Disable line-based distribution to line memories for Video Pipe X 0b1: Enable line-based distribution to line memories for Video Pipe X
BACKTOP_EN	0	Backtop write logic enable	0b0: Disable writes to BACKTOP register block 0b1: Enable writes to BACKTOP register block

BACKTOP11 (0x312)

BIT	7	6	5	4	3	2	1	0
Field	cmd_overflow4	cmd_overflow3	cmd_overflow2	cmd_overflow1	–	LMO_Z	LMO_Y	–
Reset	0b0	0b0	0b0	0b0	–	0b0	0b0	–
Access Type	Read Only	Read Only	Read Only	Read Only	–	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_overflow4	7	Command FIFO overflow detection	0b0: No overflow detected 0b1: Overflow detected
cmd_overflow3	6	Command FIFO overflow detection	0b0: No overflow detected 0b1: Overflow detected
cmd_overflow2	5	Command FIFO overflow detection	0b0: No overflow detected 0b1: Overflow detected
cmd_overflow1	4	Command FIFO overflow detection	0b0: No overflow detected 0b1: Overflow detected
LMO_Z	2	Pipeline Z line memory overflow sticky register	0b0: Pipeline Z no line memory overflow 0b1: Pipeline Z line memory overflow
LMO_Y	1	Pipeline Y line memory overflow sticky register	0b0: Pipeline Y no line memory overflow 0b1: Pipeline Y line memory overflow

BACKTOP12 (0x313)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_x[4:0]					BACKTOP_MEM_CRC_ERR	CSI_OUT_EN	–
Reset	0x00					0x0	0b1	–
Access Type	Write, Read					Read Only	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_x	7:3	Software defined BPP for pipeline X	0x8: Datatypes = x2A, x10-12, x31-37 0xA: Datatypes = x2B 0xC: Datatypes = x2C 0xE: Datatypes = x2D 0x10: Datatypes = x22, x1E, x2E 0x12: Datatypes = x23 0x14: Datatypes = x1F, x2F 0x18: Datatypes = x24, x30
BACKTOP_MEM_CRC_ERR	2	Backtop memory CRC error flag	0b0: No CRC error occurred 0b1: CRC error occurred
CSI_OUT_EN	1	Enables CSI output	0b0: CSI output disabled 0x1: CSI output enabled

BACKTOP13 (0x314)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_y[3:0]				soft_vc_x[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_y	7:4	Software defined virtual channel for pipeline Y	0xX: Software defined virtual channel for pipeline Y
soft_vc_x	3:0	Software defined virtual channel for pipeline X	0xX: Software defined virtual channel for pipeline X

BACKTOP14 (0x315)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_u[3:0]				soft_vc_z[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_u	7:4	Software defined virtual channel for pipeline U	0xX: Software defined virtual channel for pipeline U
soft_vc_z	3:0	Software defined virtual channel for pipeline Z	0xX: Software defined virtual channel for pipeline Z

BACKTOP15 (0x316)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_y_h[1:0]		soft_dt_x[5:0]					
Reset	0x0		0x00					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_y_h	7:6	High bits of software defined data type for	0bXX: High bits of software defined data type for

BITFIELD	BITS	DESCRIPTION	DECODE
		pipeline Y	pipeline Y
soft_dt_x	5:0	Software defined data type for pipeline X	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8bit 0x1F: YUV422 10bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12 BIT 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP16 (0x317)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_z_h[3:0]				soft_dt_y_l[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_z_h	7:4	High bits of software defined data type for pipeline Z	0xX: High bits of software defined data type for pipeline Z
soft_dt_y_l	3:0	Low bits of software defined data type for pipeline Y	0xX: Low bits of software defined data type for pipeline Y

BACKTOP17 (0x318)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_u[5:0]						soft_dt_z_l[1:0]	
Reset	0x00						0x0	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_u	7:2	Software defined data type for pipeline U	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8bit 0x1F: YUV422 10bit 0x22: RGB565

BITFIELD	BITS	DESCRIPTION	DECODE
			0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12 BIT 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_z_l	1:0	Low bits of software defined data type for pipeline Z	0xX: Low bits of software defined data type for pipeline Z

BACKTOP18 (0x319)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_z_h[2:0]			soft_bpp_y[4:0]				
Reset	0x0			0x00				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_z_h	7:5	High bits of software defined BPP for pipeline Z	0xX: High bits of software defined BPP for pipeline Z
soft_bpp_y	4:0	Software defined BPP for pipeline Y	0x8: Datatypes = x2A, x10-12, x31-37 0xA: Datatypes = x2B 0xC: Datatypes = x2C 0xE: Datatypes = x2D 0x10: Datatypes = x22, x1E, x2E 0x12: Datatypes = x23 0x14: Datatypes = x1F, x2F 0x18: Datatypes = x24, x30

BACKTOP19 (0x31A)

BIT	7	6	5	4	3	2	1	0
Field	–	soft_bpp_u[4:0]					soft_bpp_z_l[1:0]	
Reset	–	0x00					0x0	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_u	6:2	Software defined BPP for pipeline U	0x8: Datatypes = x2A, x10-12, x31-37 0xA: Datatypes = x2B 0xC: Datatypes = x2C 0xE: Datatypes = x2D 0x10: Datatypes = x22, x1E, x2E

BITFIELD	BITS	DESCRIPTION	DECODE
			0x12: Datatypes = x23 0x14: Datatypes = x1F, x2F 0x18: Datatypes = x24, x30
soft_bpp_z_l	1:0	Low bits of software defined BPP for pipeline Z	0bXX: Low bits of software defined BPP for pipeline Z

BACKTOP20 (0x31B)

BIT	7	6	5	4	3	2	1	0
Field	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software override value for CSI PHY0 frequency fine tuning	0xXX: PHY0 frequency fine tuning override low byte

BACKTOP21 (0x31C)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dblu	bpp8dblz	bpp8dbly	bpp8dblx	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dblu	7	BPP = 8 processed as 16-bit color enable for pipeline U	0b0: Do not process BPP = 8 as 16-bit color 0b1: Process BPP = 8 as 16-bit color
bpp8dblz	6	BPP = 8 processed as 16-bit color enable for pipeline Z	0b0: Do not process BPP = 8 as 16-bit color 0b1: Process BPP = 8 as 16-bit color
bpp8dbly	5	BPP = 8 processed as 16-bit color enable for pipeline Y	0b0: Do not process BPP = 8 as 16-bit color 0b1: Process BPP = 8 as 16-bit color
bpp8dblx	4	BPP = 8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP = 8 as 16-bit color 0b1: Process BPP = 8 as 16-bit color
phy0_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software override value for PHY0 frequency fine tuning	0xX: PHY0 frequency fine tuning override high nibble

BACKTOP22 (0x31D)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dty	override_bpp_vc_dtx	phy0_csi_tx_dpll_fb_fraction_predef_en	phy0_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dty	7	Software override enable for BPP, VC and DT	0b0: Software overide for BPP, VC and DT disabled 0x1: Software overide for BPP, VC and DT enabled
override_bpp_vc_dtx	6	Software override enable for BPP, VC and DT	0b0: Software overide for BPP, VC and DT disabled 0x1: Software overide for BPP, VC and DT enabled
phy0_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY0 software override disable for frequency fine tuning	0b0: Software overide for frequency fine tuning enabled 0x1: Software overide for frequency fine tuning disabled
phy0_csi_tx_dpll_predef_freq	4:0	CSI PHY0 output frequency in multiples of 100Mhz	0bXXXXX: CSI PHY0 output frequency (*100MHz)

BACKTOP23 (0x31E)

BIT	7	6	5	4	3	2	1	0
Field	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software override value for CSI PHY1 frequency fine tuning	0xXX: PHY1 frequency fine tuning override low byte

BACKTOP24 (0x31F)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dblu_mode	bpp8dblz_mode	bpp8dbly_mode	bpp8dblx_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dblu_mode	7	Enable 8-bit write alternate map to RAMs for pipeline U	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp8dblz_mode	6	Enable 8-bit write alternate map to RAMs for pipeline Z	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp8dbly_mode	5	Enable 8-bit write alternate map to RAMs for pipeline Y	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp8dblx_mode	4	Enable 8-bit write alternate map to RAMs for pipeline X	0b0: Write alternative map disabled 0x1: Write alternative map enabled
phy1_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software override value for PHY1 frequency fine tuning	0xX: PHY1 frequency fine tuning override high nibble

BACKTOP25 (0x320)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dtu	override_bpp_vc_dtz	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dtu	7	Software override enable for BPP, VC and DT	0b0: Software overide for BPP, VC and DT disabled 0x1: Software overide for BPP, VC and DT enabled
override_bpp_vc_dtz	6	Software override enable for BPP, VC and DT	0b0: Software overide for BPP, VC and DT disabled 0x1: Software overide for BPP, VC and DT enabled
phy1_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY1 software override disable for frequency fine tuning	0b0: Software overide for frequency fine tuning enabled 0x1: Software overide for frequency fine tuning disabled
phy1_csi_tx_dpll_predef_freq	4:0	CSI PHY1 output frequency in multiples of 100Mhz	0bXXXXX: CSI PHY1 output frequency (*100MHz)

BACKTOP26 (0x321)

BIT	7	6	5	4	3	2	1	0
Field	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software override value for CSI PHY2 frequency fine tuning	0xXX: PHY2 frequency fine tuning override low byte

BACKTOP27 (0x322)

BIT	7	6	5	4	3	2	1	0
Field	yuv_8_10_mux_mode4	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode4	7	Mode 4 yuv422 8/10 bit muxed mode support	0x0: Disable yuv422 8/10 bit muxed mode support 0x1: Enable yuv422 8/10 bit muxed mode support

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode3	6	Mode 3 yuv422 8/10 bit muxed mode support	0x0: Disable yuv422 8/10 bit muxed mode support 0x1: Enable yuv422 8/10 bit muxed mode support
yuv_8_10_mux_mode2	5	Mode 2 yuv422 8/10 bit muxed mode support	0x0: Disable yuv422 8/10 bit muxed mode support 0x1: Enable yuv422 8/10 bit muxed mode support
yuv_8_10_mux_mode1	4	Mode 1 yuv422 8/10 bit muxed mode support	0x0: Disable yuv422 8/10 bit muxed mode support 0x1: Enable yuv422 8/10 bit muxed mode support
phy2_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software override value for PHY2 frequency fine tuning	0xX: PHY2 frequency fine tuning override high nibble

BACKTOP28 (0x323)

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				
Reset	–	–	0b1	0x0F				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY2 software override disable for frequency fine tuning	0b0: Software overide for frequency fine tuning enabled 0x1: Software overide for frequency fine tuning disabled
phy2_csi_tx_dpll_predef_freq	4:0	CSI PHY2 output frequency in multiples of 100Mhz	0bXXXXX: CSI PHY2 output frequency (*100MHz)

BACKTOP29 (0x324)

BIT	7	6	5	4	3	2	1	0
Field	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software override value for CSI PHY3 frequency fine tuning	0xXX: PHY3 frequency fine tuning override low byte

BACKTOP30 (0x325)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP_W_FRAME	–	–	–	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0x0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP_W_FRAME	7	When this register is set, backtop waits for a new frame before generating MIPI packet requests	0b0: Do not wait for a new frame before generating a MIPI packet 0b1: Wait for a new frame before generating a MIPI packet
phy3_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software override value for PHY3 frequency fine tuning	0xXX: PHY3 frequency fine tuning override low byte

BACKTOP31 (0x326)

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
Reset	–	–	0b1	0x0F				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_predef_en	5	CSI PHY3 software override disable for frequency fine tuning	0b0: Software overide for frequency fine tuning enabled 0x1: Software overide for frequency fine tuning disabled
phy3_csi_tx_dpll_predef_freq	4:0	CSI PHY3 output frequency in multiples of 100Mhz	0bXXXXX: CSI PHY3 output frequency (*100MHz)

BACKTOP32 (0x327)

BIT	7	6	5	4	3	2	1	0
Field	bpp10dblu_mode	bpp10dblz_mode	bpp10dbly_mode	bpp10dblx_mode	bpp10dblu	bpp10dblz	bpp10dbly	bpp10dblx
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dblu_mode	7	Enable 8-bit write alternate map to RAMs for pipeline X	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp10dblz_mode	6	Enable 8-bit write alternate map to RAMs for pipeline X	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp10dbly_mode	5	Enable 8-bit write alternate map to RAMs for pipeline X	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp10dblx_mode	4	Enable 8-bit write alternate map to RAMs for pipeline X	0b0: Write alternative map disabled 0x1: Write alternative map enabled
bpp10dblu	3	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color
bpp10dblz	2	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbly	1	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color
bpp10dblx	0	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color

BACKTOP33 (0x328)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	bpp12dblu	bpp12dblz	bpp12dbly	bpp12dblx
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
bpp12dblu	3	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color
bpp12dblz	2	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color
bpp12dbly	1	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color
bpp12dblx	0	BPP=8 processed as 16-bit color enable for pipeline X	0b0: Do not process BPP=8 as 16-bit color 0b1: Process BPP=8 as 16-bit color

MIPI_PHY0 (0x330)

BIT	7	6	5	4	3	2	1	0
Field	force_csi_out_en	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
force_csi_out_en	7	Force CSI output clock for use in MIPI loopback test	0b0: CSI output clock not enabled for MIPI loopback test 0b1: CSI output clock enabled for MIPI loopback test

MIPI_PHY1 (0x331)

BIT	7	6	5	4	3	2	1	0
Field	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_przero	7:6	Typical DPHY data lane HS_prepare + HS_zero timing	0b00: 146ns + 24UI 0b01: 160ns + 24UI 0b10: 173ns + 24UI 0b11: 200ns + 24UI

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_prep	5:4	Typical DPHY data lane HS_prepare timing	0b00: 46.7ns + 4UI 0b01: 53.4ns + 4UI 0b10: 60.0ns + 4UI 0b11: 66.7ns + 4UI
t_clk_trail	3:2	Typical DPHY clock HS_trail timing	0b00: 160ns 0b01: 167ns 0b10: 173ns 0b11: 180ns
t_clk_przero	1:0	Typical DPHY clock lane HS_prepare + HS_zero timing	0b00: 306ns 0b01: 600ns 0b10: 900ns 0b11: 1200ns

MIPI_PHY2 (0x332)

BIT	7	6	5	4	3	2	1	0
Field	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
Reset	0xF				0b00		0b00	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
phy_Stdby_n	7:4	Puts PHY into standby mode if not used to save power	0b1111: All PHYs not in standby 0bXXX0: Put PHY0 in standby mode 0bXX0X: Put PHY1 in standby mode 0bX0XX: Put PHY2 in standby mode 0b0XXX: Put PHY3 in standby mode
t_lpx	3:2	Typical DPHY Tlpx timing	0b00: 53.4ns 0b01: 106.7ns 0b10: 160ns 0b11: 213.4ns
t_hs_trail	1:0	Typical DPHY data lane HS_trail timing	0b00: 66.7ns + 8UI 0b01: 80ns + 8UI 0b10: 93.4ns + 8UI 0b11: 106.7ns + 8UI

MIPI_PHY3 (0x333)

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
Reset	0x4				0xE			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lane_map	7:4	PHY1 to Port A lane mapping in 2x4 configurations Bit[1:0] map PHY1 data lane 0. Bit[3:2] map PHY1 data lane 1.	0bXX00: Map PHY1 D0 to D0 0bXX01: Map PHY1 D0 to D1 0bXX10: Map PHY1 D0 to D2 0bXX11: Map PHY1 D0 to D3 0b00XX: Map PHY1 D1 to D0 0b01XX: Map PHY1 D1 to D1 0b10XX: Map PHY1 D1 to D2

BITFIELD	BITS	DESCRIPTION	DECODE
			0b11XX: Map PHY1 D1 to D3
phy0_lane_map	3:0	PHY0 to Port A lane mapping in 2x4 configurations Bit[1:0] map PHY0 data lane 0. Bit[3:2] map PHY0 data lane 1.	0bXX00: Map PHY0 D0 to D0 0bXX01: Map PHY0 D0 to D1 0bXX10: Map PHY0 D0 to D2 0bXX11: Map PHY0 D0 to D3 0b00XX: Map PHY0 D1 to D0 0b01XX: Map PHY0 D1 to D1 0b10XX: Map PHY0 D1 to D2 0b11XX: Map PHY0 D1 to D3

MIPI_PHY4 (0x334)

BIT	7	6	5	4	3	2	1	0
Field	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
Reset	0xE				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_lane_map	7:4	PHY3 to Port B lane mapping in 2x4 configurations Bit[1:0] map PHY3 data lane 0. Bit[3:2] map PHY3 data lane 1.	0bXX00: Map PHY3 D0 to D0 0bXX01: Map PHY3 D0 to D1 0bXX10: Map PHY3 D0 to D2 0bXX11: Map PHY3 D0 to D3 0b00XX: Map PHY3 D1 to D0 0b01XX: Map PHY3 D1 to D1 0b10XX: Map PHY3 D1 to D2 0b11XX: Map PHY3 D1 to D3
phy2_lane_map	3:0	PHY2 to Port B lane mapping in 2x4 configurations Bit[1:0] map PHY2 data lane 0. Bit[3:2] map PHY2 data lane 1.	0bXX00: Map PHY2 D0 to D0 0bXX01: Map PHY2 D0 to D1 0bXX10: Map PHY2 D0 to D2 0bXX11: Map PHY2 D0 to D3 0b00XX: Map PHY2 D1 to D0 0b01XX: Map PHY2 D1 to D1 0b10XX: Map PHY2 D1 to D2 0b11XX: Map PHY2 D1 to D3

MIPI_PHY5 (0x335)

BIT	7	6	5	4	3	2	1	0
Field	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
Reset	0b00		0b000			0b000		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
t_clk_prep	7:6	Typical DPHY clock lane HS_prepare timing	0b00: 40ns 0b01: 46.7ns 0b10: 53.4ns 0b11: 60ns
phy1_pol_map	5:3	PHY1 lane polarity for clock, D1 and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1

BITFIELD	BITS	DESCRIPTION	DECODE
			0b0XX: Normal polarity for clock lane 0b1XX: Inverse polarity for clock lane
phy0_pol_map	2:0	PHY0 lane polarity for clock, D1 and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane 0b1XX: Inverse polarity for clock lane

MIPI_PHY6 (0x336)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1	phy_cp0	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
Reset	0b0	0b0	0b000			0b000		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1	7	PHY port copy 1	0x0: Disable copy 1 0x1: Enable copy 1
phy_cp0	6	PHY port copy 0	0x0: Disable copy 0 0x1: Enable copy 0
phy3_pol_map	5:3	PHY3 lane polarity for clock, D1 and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane 0b1XX: Inverse polarity for clock lane
phy2_pol_map	2:0	PHY2 lane polarity for clock, D1 and D0. In normal polarity, P is positive, N is negative. In inverse polarity, P is negative, N is positive.	0bXX0: Normal polarity for data lane 0 0bXX1: Inverse polarity for data lane 0 0bX0X: Normal polarity for data lane 1 0bX1X: Inverse polarity for data lane 1 0b0XX: Normal polarity for clock lane 0b1XX: Inverse polarity for clock lane

MIPI_PHY8 (0x338)

BIT	7	6	5	4	3	2	1	0
Field	t_lpxesc[2:0]			–	–	–	–	–
Reset	0b000			–	–	–	–	–
Access Type	Write, Read			–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
t_lpxesc	7:5	Typical DPHY Tlpx timing in escape mode	0b000: 66.67ns 0b001: 80ns 0b010: 100ns 0b011: 133ns 0b100: 200ns 0b101: 400ns 0b110: 1000ns 0b111: 2000ns

MIPI_PHY9 (0x339)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp0_dst[1:0]		–	–	–	–	–	phy_cp0_overflow
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read		–	–	–	–	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp0_dst	7:6	PHY copy 0 destination	0bXX: PHY copy 0 destination
phy_cp0_overflow	0	PHY copy 0 FIFO overflow	0x0: No overflow error 0x1: Overflow error

MIPI_PHY10 (0x33A)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp0_src[1:0]		–	–	–	–	–	phy_cp0_underflow
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read		–	–	–	–	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp0_src	7:6	PHY copy 0 source	0bXX: PHY copy 0 source
phy_cp0_underflow	0	PHY copy 0 FIFO underflow	0x0: No underflow error 0x1: Underflow error

MIPI_PHY11 (0x33B)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1_dst[1:0]		–	–	–	–	–	phy_cp1_overflow
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read		–	–	–	–	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1_dst	7:6	PHY copy 1 destination	0bXX: PHY copy 1 destination
phy_cp1_overflow	0	PHY copy 1 FIFO overflow	0x0: No overflow error 0x1: Overflow error

MIPI_PHY12 (0x33C)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1_src[1:0]		–	–	–	–	–	phy_cp1_underflow
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read		–	–	–	–	–	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1_src	7:6	Phy copy 1 source	0bXX: Phy copy 1 source
phy_cp1_underflow	0	Phy copy 1 FIFO underflow	0x0: No underflow error 0x1: Underflow error

FSYNC_0 (0x3E0)

BIT	7	6	5	4	3	2	1	0
Field	EN_OFLOW_RST_FS	–	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
Reset	0x0	–	0b0	0x0	0x3		0x2	
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
EN_OFLOW_RST_FS	7	Enables link PRBS-7 generator. When enabled, memory overflow resets frame sync generation	0b0: Link PRBS generator disabled 0b1: Link PRBS generator enabled
FSYNC_OUT_PIN	5	Selects pin to output frame sync signal (effective only when bitfield FSYNC_METH = 0b01)	0b0: MFP3 0b1: MFP0
EN_VS_GEN	4	When enabled, VS is generated internally by the frame sync generator (not effective when bitfield FSYNC_MODE = 0b11)	0x0: Internal frame sync does not generate VS 0x1: Internal frame sync generates VS
FSYNC_MODE	3:2	Frame synchronization mode	0b00: Frame sync generation is on. GMSL2 mode: GPIO is not used as FSYNC output GMSL1 mode: FSYNC pin is High-Z 0b01: Frame sync generation is on. GMSL2 mode: GPIO is used as FSYNC output and drives a slave device GMSL1 mode: FSYNC pin drives a slave device 0b10: Frame sync generation is off. GMSL2 mode: GPIO is not used as FSYNC output. GMSL1 mode: FSYNC pin is driven by a master device 0b11: Frame sync generation is off. GMSL2 mode: GPIO is not used as FSYNC output GMSL1 mode: GPI-to-GPO channel can be used for frame sync
FSYNC_METH	1:0	Frame synchronization method	0b00: Manual 0b01: Semi-auto 0b10: Auto 0b11: Reserved

FSYNC_1 (0x3E1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	FSYNC_PER_DIV[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PER_DIV	3:0	Frame sync transmission period in terms of VSYNC periods	0x0: 1 0x1: 2 0x2: 3 0x3: 6 0x4: 8 0x5: 10 0x6: 12 0x7: 16 0x8: 20 0x9: 24 0xA: 32 0xB: 48 0xC: 64 0xD: 80 0xE: 96 0xF: 128

FSYNC_2 (0x3E2)

BIT	7	6	5	4	3	2	1	0
Field	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]			
Reset	0x4			0x0	0x1			
Access Type	Write, Read			Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MST_LINK_SEL	7:5	Master link select for frame sync generation	0b000: Video X 0b001: Video Y 0b010: Video Z 0b011: Video U 0b100: Auto select 0b101: Auto select 0b110: Auto select 0b111: Auto select
K_VAL_SIGN	4	Sign bit of K_VAL	0b0: K_VAL is positive 0b1: K_VAL is negative
K_VAL	3:0	Desired frame sync margin (microseconds, typical) with respect to the VSYNC of the slowest link in auto mode or with respect to the VSYNC of the master link in semi-auto mode.	0x0: 1 0x1: 2 0x2: 3 0x3: 4 0x4: 5 0x5: 6 0x6: 7 0x7: 8 0x8: 10 0x9: 12 0xA: 14 0xB: 16 0xC: 20 0xD: 24 0xE: 28 0xF: 32

FSYNC_3 (0x3E3)

BIT	7	6	5	4	3	2	1	0
Field	P_VAL_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_L	7:0	Low byte of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in auto mode or with respect to the VSYNC of the master link in semi-auto mode	0xXX: Low byte of PCLK cycles frame sync margin

FSYNC_4 (0x3E4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	P_VAL_SIGN	P_VAL_H[4:0]				
Reset	–	–	0x0	0x00				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_SIGN	5	Sign bit of P_VAL	0b0: P_VAL is positive 0b1: P_VAL is negative
P_VAL_H	4:0	High bits of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in auto mode or with respect to the VSYNC of the master link in semi-auto mode	0b00000: High bits of PCLK cycles frame sync margin

FSYNC_5 (0x3E5)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_L	7:0	Low byte of frame sync period in terms of pixel clock (effective when FSYNC_0 (0x3E0) bitfields FSYNC_METH = 0b00 and FSYNC_MODE = 0b0X)	0xXX: Low byte of PCLK cycles in frame period

FSYNC_6 (0x3E6)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_M	7:0	Middle byte of frame sync period in terms of pixel clock (effective when FSYNC_0 (0x3E0) bitfields FSYNC_METH = 0b00 and FSYNC_MODE = 0b0X)	0xXX: Middle byte of PCLK cycles in frame period

FSYNC_7 (0x3E7)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_H	7:0	High byte of frame sync period in terms of pixel clock (effective when FSYNC_0 (0x3E0) bitfields FSYNC_METH = 0b00 and FSYNC_MODE = 0b0X)	0xXX: High byte of PCLK cycles in frame period

FSYNC_8 (0x3E8)

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_ERR_THR_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ERR_THR_L	7:0	Low byte of the error threshold for difference between the earliest and latest VSYNCs in terms of PCLK cycles. The default is 40µs for 96MHz PCLK. The function is disabled when all 13 bits are 0's.	0xXX: Low byte of PCLK cycles in the VSYNC error threshold

FSYNC_9 (0x3E9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
Reset	–	–	–	0x0F				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ ERR_THR_H	4:0	High bits of the error threshold for difference between the earliest and latest VSYNCs in terms of PCLK cycles. The default is 40µs for 96MHz PCLK. The function is disabled when all 13 bits are 0's.	0bXXXXX: High bits of PCLK cycles in the VSYNC error threshold

FSYNC_10 (0x3EA)

BIT	7	6	5	4	3	2	1	0
Field	OVLP_WINDOW_L[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OVLP_WIND OW_L	7:0	Low byte of the overlap window value in terms of PCLK cycles. The default is 60µs for 96MHz PCLK. The function is disabled when all 13 bits are 0's.	0xXX: Low byte of PCLK cycles in the VSYNC overlap window.

FSYNC_11 (0x3EB)

BIT	7	6	5	4	3	2	1	0
Field	EN_FSIN_L AST	–	–	OVLP_WINDOW_H[4:0]				
Reset	0x0	–	–	0x16				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EN_FSIN_LA ST	7	FSIN position	0b0: FSIN can occur anywhere with respect to VS rising edges 0b1: FSIN occurs after all rising edges
OVLP_WIND OW_H	4:0	Low byte of the overlap window value in terms of PCLK cycles. The default is 60µs for 96MHz PCLK. The function is disabled when all 13 bits are 0's.	0bXXXXX: High bits of PCLK cycles in the VSYNC overlap window.

FSYNC_16 (0x3F0)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_ERR _CNT	7:0	Frame sync error counter. Resets to 0 when read or when FSYNC_LOCKED goes high.	0xXX: Frame sync error counter

FSYNC_17 (0x3F1)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
Reset	0x1E					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_TX_ID	7:3	GPIO ID used for transmitting FSYNC signal	0bXXXXX: GPIO ID
FSYNC_ERR_THR	2:0	Frame sync error reporting threshold. FSYNC_ERR_FLAG is asserted when FSYNC_ERR_CNT ≥ FSYNC_ERR_THR.	0bXXX: Frame sync error reporting threshold

FSYNC_18 (0x3F2)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_L	7:0	Low byte of calculated VS period (number of PCLKs) of master link in auto or semi-auto synchronization mode. Use when FSYNC_0 (0x3E0) bitfields FSYNC_METH = 0b10 and FSYNC_MODE = 0b0X.	0xXX: Low byte of PCLKs in VS period in master link auto or semi-auto synchronization mode.

FSYNC_19 (0x3F3)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_M[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_M	7:0	Middle byte of calculated VS period (number of PCLKs) of master link in auto or semi-auto synchronization mode. Use when FSYNC_0 (0x3E0) bitfields FSYNC_METH = 0b10 and FSYNC_MODE = 0b01.	0xXX: Middle byte of PCLKs in VS period in master link auto or semi-auto synchronization mode.

FSYNC_20 (0x3F4)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_H[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_H	7:0	High byte of calculated VS period (number of PCLKs) of master link in auto or semi-auto synchronization mode. Use when FSYNC_0 (0x3E0)bitfields FSYNC_METH = 0b10 and FSYNC_MODE = 0b0X.	0xXX: High byte of PCLKs in VS period in master link auto or semi-auto synchronization mode.

FSYNC_21 (0x3F5)

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_L	7:0	Low byte of the difference between the fastest and the slowest frame in terms of master PCLK cycles	0xXX: Low byte of the difference between the fastest and slowest frame in terms of the master PCLK cycles.

FSYNC_22 (0x3F6)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
Reset	0x0	0x0	0x00					
Access Type	Read Clears All	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_LOSS_OF_LOCK	7	Frame synchronization lost lock flag. Cleared when read	0b0: Frame sync lock not lost 0b1: Frame sync lock lost
FSYNC_LOCKED	6	Frame synchronization lock flag	0b0: Frame sync not locked 0b1: Frame sync locked
FRM_DIFF_H	5:0	High bits of the difference between the fastest and the slowest frame in terms of master PCLK cycles	0bXXXXXX: High bits of number of PCLKs in the difference between the fastest and slowest frame.

MIPI_TX11 (0x40B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched	0xX1: Enable MAP_SRC_0 and MAP_DST_0 registers 0xX2: Enable MAP_SRC_1 and MAP_DST_1 registers 0xX4: Enable MAP_SRC_2 and MAP_DST_2

BITFIELD	BITS	DESCRIPTION	DECODE
		virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	registers 0xX8: Enable MAP_SRC_3 and MAP_DST_3 registers 0x1X: Enable MAP_SRC_4 and MAP_DST_4 registers 0x2X: Enable MAP_SRC_5 and MAP_DST_5 registers 0x4X: Enable MAP_SRC_6 and MAP_DST_6 registers 0x8X: Enable MAP_SRC_7 and MAP_DST_7 registers

MIPI_TX12 (0x40C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable MAP_SRC_8 and MAP_DST_8 registers 0xX2: Enable MAP_SRC_9 and MAP_DST_9 registers 0xX4: Enable MAP_SRC_10 and MAP_DST_10 registers 0xX8: Enable MAP_SRC_11 and MAP_DST_11 registers 0x1X: Enable MAP_SRC_12 and MAP_DST_12 registers 0x2X: Enable MAP_SRC_13 and MAP_DST_13 registers 0x4X: Enable MAP_SRC_14 and MAP_DST_14 registers 0x8X: Enable MAP_SRC_15 and MAP_DST_15 registers

MIPI_TX13 (0x40D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Mapping source register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 0

MIPI_TX14 (0x40E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Mapping destination register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 0

MIPI_TX15 (0x40F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Mapping source register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 1

MIPI_TX16 (0x410)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Mapping destination register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 1

MIPI_TX17 (0x411)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Mapping source register 2. The register is split into two decode segments:	0xXX: VC and DT source for map 2

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX18 (0x412)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Mapping destination register 2. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 2

MIPI_TX19 (0x413)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Mapping source register 3. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 3

MIPI_TX20 (0x414)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Mapping destination register 3. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 3

MIPI_TX21 (0x415)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Mapping source register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 4

MIPI_TX22 (0x416)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Mapping destination register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 4

MIPI_TX23 (0x417)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Mapping source register 5. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 5

MIPI_TX24 (0x418)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Mapping destination register 5. The register is split into two decode segments:	0xXX: VC and DT destination for map 5

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX25 (0x419)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Mapping source register 6. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 6

MIPI_TX26 (0x41A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Mapping destination register 6. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 6

MIPI_TX27 (0x41B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Mapping source register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 7

MIPI_TX28 (0x41C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Mapping destination register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 7

MIPI_TX29 (0x41D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Mapping source register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 8

MIPI_TX30 (0x41E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Mapping destination register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 8

MIPI_TX31 (0x41F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Mapping source register 9. The register is split into two decode segments:	0xXX: VC and DT source for map 9

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX32 (0x420)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Mapping destination register 9. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 9

MIPI_TX33 (0x421)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Mapping source register 10. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 10

MIPI_TX34 (0x422)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Mapping destination register 10. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 10

MIPI_TX35 (0x423)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Mapping source register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 11

MIPI_TX36 (0x424)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Mapping destination register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 11

MIPI_TX37 (0x425)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Mapping source register 12. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 12

MIPI_TX38 (0x426)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Mapping destination register 12. The register is split into two decode segments:	0xXX: VC and DT destination for map 12

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX39 (0x427)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Mapping source register 13. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 13

MIPI_TX40 (0x428)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Mapping destination register 13. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 13

MIPI_TX41 (0x429)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Mapping source register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 14

MIPI_TX42 (0x42A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Mapping destination register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 14

MIPI_TX43 (0x42B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Mapping source register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 15

MIPI_TX44 (0x42C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Mapping destination register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 15

MIPI_TX45 (0x42D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	CSI2 controller destination for MAP_SRC_3 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1

BITFIELD	BITS	DESCRIPTION	DECODE
			0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_2	5:4	CSI2 controller destination for MAP_SRC_2 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_1	3:2	CSI2 controller destination for MAP_SRC_1 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_0	1:0	CSI2 controller destination for MAP_SRC_0 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX46 (0x42E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	CSI2 controller destination for MAP_SRC_7 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_6	5:4	CSI2 controller destination for MAP_SRC_6 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_5	3:2	CSI2 controller destination for MAP_SRC_5 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_4	1:0	CSI2 controller destination for MAP_SRC_4 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX47 (0x42F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	CSI2 controller destination for MAP_SRC_11 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_10	5:4	CSI2 controller destination for MAP_SRC_10 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_9	3:2	CSI2 controller destination for MAP_SRC_9 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_8	1:0	CSI2 controller destination for MAP_SRC_8 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX48 (0x430)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	CSI2 controller destination for MAP_SRC_15 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_14	5:4	CSI2 controller destination for MAP_SRC_14 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_13	3:2	CSI2 controller destination for MAP_SRC_13 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_12	1:0	CSI2 controller destination for MAP_SRC_12 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX49 (0x431)

BIT	7	6	5	4	3	2	1	0
Field	MAP_CON[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	Concatenation register for sync mode settings. The register is split into four decode segments: bit [7] Enable 4WxH or Wx4H bit [6] Reserved bit [5:4] Master video stream number. This is the first line to concatenate. All others follow in order bit [3:0] Each bit selects a video stream to concatenate	0bXXXXXXX1: Concatenate video stream 0 0bXXXXXX1X: Concatenate video stream 1 0bXXXXX1XX: Concatenate video stream 2 0bXXXX1XXX: Concatenate video stream 3 0bXX00XXXX: Select video stream 0 as master 0bXX01XXXX: Select video stream 1 as master 0bXX10XXXX: Select video stream 2 as master 0bXX11XXXX: Select video stream 3 as master 0b0XXXXXXX: Enable Wx4H mode 0b1XXXXXXX: Enable 4WxH mode

MIPI_TX51 (0x433)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
MODE_DT	3	MIPI Tx enable 24-bit packing of 8-bit MIPI UDP	0x0: Disable 24-bit packing of 8-bit MIPI UDP 0x1: Enable 24-bit packing of 8-bit MIPI UDP
ALT_MEM_MAP10	2	Alternative memory map enable for 10-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP8	1	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP12	0	Alternative memory map enable for 12-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

MIPI_TX1 (0x441)

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7:0	MIPI VS short packet counter mode	0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter

MIPI_TX2 (0x442)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	MIPI Tx status. The register is split into three decode segments: bit [0] SYNC mode enable. bit [1] Video sync flag bit [2] Loss of video sync flag	0bXXXXXXX0: SYNC mode disabled 0bXXXXXXX1: SYNC mode enabled 0bXXXXXX0X: Video channels not in-sync 0bXXXXXX1X: Video channels in-sync 0bXXXXX0XX: No loss of video sync 0bXXXXX1XX: Video sync lost after last read of this register or RESET.

MIPI_TX3 (0x443)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	DPHY deskew initial calibration control. The register is split into six decode segments: bit [7] Selects auto-initial deskew calibration on or off bit [6] Reserved bit [5] Any bit change initiates an initial calibration if bit [4] = 1 bit [4] Selects manual initial on or off bit [3] Reserved bit [2:0] Selects initial deskew width	0bXXXXX000: Initial deskew width = 1*32k UI 0bXXXXX001: Initial deskew width = 2*32k UI 0bXXXXX010: Initial deskew width = 3*32k UI 0bXXXXX011: Initial deskew width = 4*32k UI 0bXXXXX100: Initial deskew width = 5*32k UI 0bXXXXX101: Initial deskew width = 6*32k UI 0bXXXXX110: Initial deskew width = 7*32k UI 0bXXXXX111: Initial deskew width = 8*32k UI 0bXXXX0XXX: Reserved 0bXXXX1XXX: Reserved 0bXXX0XXXX: Manual initial off 0bXXX1XXXX: Manual initial on 0bXX0XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bXX1XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bX0XXXXXX: Reserved 0bX1XXXXXX: Reserved 0b0XXXXXXX: Auto initial deskew off 0b1XXXXXXX: Auto initial deskew on

MIPI_TX4 (0x444)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_PER	7:0	DPHY periodic deskew calibration control. The register is split into four decode segments: bit [7] Selects periodic deskew calibration on or off bit [6] Selects generation on rising or falling edge of VS bit [5:3] Selects periodic interval bit [2:0] Selects periodic deskew width	0bXXXXX000: Periodic deskew width = 1k UI 0bXXXXX001: Periodic deskew width = 2k UI 0bXXXXX010: Periodic deskew width = 3k UI 0bXXXXX011: Periodic deskew width = 4k UI 0bXXXXX100: Periodic deskew width = 5k UI 0bXXXXX101: Periodic deskew width = 6k UI 0bXXXXX110: Periodic deskew width = 7k UI 0bXXXXX111: Periodic deskew width = 8k UI 0bXX000XXX: Periodic deskew calibration generated every frame 0bXX001XXX: Periodic deskew calibration generated every 2 frames 0bXX010XXX: Periodic deskew calibration generated every 4 frames 0bXX011XXX: Periodic deskew calibration generated every 8 frames 0bXX100XXX: Periodic deskew calibration generated every 16 frames 0bXX101XXX: Periodic deskew calibration generated every 32 frames 0bXX110XXX: Periodic deskew calibration generated every 64 frames 0bXX111XXX: Periodici deskew calibration generated every 128 frames 0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS 0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS 0b0XXXXXXX: Periodic deskew calibration off 0b1XXXXXXX: Periodic deskew calibration on

MIPI_TX5 (0x445)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_PRE[7:0]							
Reset	0x71							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_PRE	7:0	Number of MIPI byte clocks to wait before enabling HS data	0xXX: Number of MIPI byte clocks

MIPI_TX6 (0x446)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_POST[7:0]							
Reset	0x19							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_POST	7:0	Number of MIPI byte clocks to hold clock active after data	0xXX: Number of MIPI byte clocks

MIPI_TX7 (0x447)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TX_GAP[7:0]							
Reset	0x1C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TX_GAP	7:0	Number of MIPI byte clocks to wait after the HS clock has entered low-power (LP) mode before enabling it again for the next transmission	0xXX: Number of MIPI byte clocks

MIPI_TX8 (0x448)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_L	7:0	Low byte of CSI2 transmit wake-up	0xXX: Number of MIPI byte clocks

MIPI_TX9 (0x449)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_M[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_M	7:0	Middle byte of CSI2 transmit wake-up	0xXX: Number of MIPI byte clocks

MIPI_TX10 (0x44A)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		–	–	CSI_VCX_EN	CSI2_TWAKEUP_H[2:0]		
Reset	0b11		–	–	0b0	0b000		
Access Type	Write, Read		–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	Set number of MIPI data lanes	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes 0b11: Four data lanes
CSI_VCX_E	3	Enables VC extension	0x0: Disable VC extension

BITFIELD	BITS	DESCRIPTION	DECODE
N			0x1: Enable VC extension
CSI2_TWAKEUP_H	2:0	High bits of CSI2 transmit wake-up	0xXX: Number of MIPI byte clocks

MIPI_TX11 (0x44B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable Map_SRC_0 and Map_DST_0 registers 0xX2: Enable MAP_SRC_1 and MAP_DST_1 registers 0xX4: Enable MAP_SRC_2 and MAP_DST_2 registers 0xX8: Enable MAP_SRC_3 and MAP_DST_3 registers 0x1X: Enable MAP_SRC_4 and MAP_DST_4 registers 0x2X: Enable MAP_SRC_5 and MAP_DST_5 registers 0x4X: Enable MAP_SRC_6 and MAP_DST_6 registers 0x8X: Enable MAP_SRC_7 and MAP_DST_7 registers

MIPI_TX12 (0x44C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable MAP_SRC_8 and MAP_DST_8 registers 0xX2: Enable MAP_SRC_9 and MAP_DST_9 registers 0xX4: Enable MAP_SRC_10 and MAP_DST_10 registers 0xX8: Enable MAP_SRC_11 and MAP_DST_11 registers 0x1X: Enable MAP_SRC_12 and MAP_DST_12 registers 0x2X: Enable MAP_SRC_13 and MAP_DST_13 registers 0x4X: Enable MAP_SRC_14 and MAP_DST_14 registers

BITFIELD	BITS	DESCRIPTION	DECODE
			0x8X: Enable MAP_SRC_15 and MAP_DST_15 registers

MIPI_TX13 (0x44D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Mapping source register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 0

MIPI_TX14 (0x44E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Mapping destination register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 0

MIPI_TX15 (0x44F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Mapping source register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 1

MIPI_TX16 (0x450)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Mapping destination register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 1

MIPI_TX17 (0x451)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Mapping source register 2. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 2

MIPI_TX18 (0x452)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Mapping destination register 2. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 2

MIPI_TX19 (0x453)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Mapping source register 3. The register is split into two decode segments:	0xXX: VC and DT source for map 3

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX20 (0x454)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Mapping destination register 3. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 3

MIPI_TX21 (0x455)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Mapping source register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 4

MIPI_TX22 (0x456)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Mapping destination register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 4

MIPI_TX23 (0x457)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Mapping source register 5. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 5

MIPI_TX24 (0x458)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Mapping destination register 5. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 5

MIPI_TX25 (0x459)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Mapping source register 6. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 6

MIPI_TX26 (0x45A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Mapping destination register 6. The register is split into two decode segments:	0xXX: VC and DT destination for map 6

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX27 (0x45B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Mapping source register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 7

MIPI_TX28 (0x45C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Mapping destination register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 7

MIPI_TX29 (0x45D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Mapping source register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 8

MIPI_TX30 (0x45E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Mapping destination register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 8

MIPI_TX31 (0x45F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Mapping source register 9. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 9

MIPI_TX32 (0x460)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Mapping destination register 9. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 9

MIPI_TX33 (0x461)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Mapping source register 10. The register is split into two decode segments:	0xXX: VC and DT source for map 10

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX34 (0x462)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Mapping destination register 10. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 10

MIPI_TX35 (0x463)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Mapping source register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 11

MIPI_TX36 (0x464)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Mapping destination register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 11

MIPI_TX37 (0x465)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Mapping source register 12. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 12

MIPI_TX38 (0x466)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Mapping destination register 12. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 12

MIPI_TX39 (0x467)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Mapping source register 13. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 13

MIPI_TX40 (0x468)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Mapping destination register 13. The register is split into two decode segments:	0xXX: VC and DT destination for map 13

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX41 (0x469)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Mapping source register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 14

MIPI_TX42 (0x46A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Mapping destination register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 14

MIPI_TX43 (0x46B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Mapping source register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 15

MIPI_TX44 (0x46C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Mapping destination register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 15

MIPI_TX45 (0x46D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	CSI2 controller destination for MAP_SRC_3 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_2	5:4	CSI2 controller destination for MAP_SRC_2 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_1	3:2	CSI2 controller destination for MAP_SRC_1 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_0	1:0	CSI2 controller destination for MAP_SRC_0 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX46 (0x46E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	CSI2 controller destination for MAP_SRC_7 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_6	5:4	CSI2 controller destination for MAP_SRC_6 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_5	3:2	CSI2 controller destination for MAP_SRC_5 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_4	1:0	CSI2 controller destination for MAP_SRC_4 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX47 (0x46F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	CSI2 controller destination for MAP_SRC_11 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_10	5:4	CSI2 controller destination for MAP_SRC_10 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_9	3:2	CSI2 controller destination for MAP_SRC_9 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_8	1:0	CSI2 controller destination for MAP_SRC_8 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX48 (0x470)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	CSI2 controller destination for MAP_SRC_15 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1

BITFIELD	BITS	DESCRIPTION	DECODE
			0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_14	5:4	CSI2 controller destination for MAP_SRC_14 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_13	3:2	CSI2 controller destination for MAP_SRC_13 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_12	1:0	CSI2 controller destination for MAP_SRC_12 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX49 (0x471)

BIT	7	6	5	4	3	2	1	0
Field	MAP_CON[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	Concatenation register for sync mode settings. The register is split into four decode segments: bit [7] Enable 4WxH or Wx4H bit [6] Reserved bit [5:4] Master video stream number. This is the first line to concatenate. All others follow in order bit [3:0] Each bit selects a video stream to concatenate	0bXXXXXXX1: Concatenate video stream 0 0bXXXXXX1X: Concatenate video stream 1 0bXXXXX1XX: Concatenate video stream 2 0bXXXX1XXX: Concatenate video stream 3 0bXX00XXXX: Select video stream 0 as master 0bXX01XXXX: Select video stream 1 as master 0bXX10XXXX: Select video stream 2 as master 0bXX11XXXX: Select video stream 3 as master 0b0XXXXXXX: Enable Wx4H mode 0b1XXXXXXX: Enable 4WxH mode

MIPI_TX50 (0x472)

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	Periodic deskew select register. The register is split into three decode segments: bit [7] Select periodic deskew calibration for one or all virtual channels bit [6:5] Reserved bit [4:0] Virtual channel to generate periodic deskew calibration when only one channel is selected by bit [7]	0b0XXXXXXX: Generate periodic calibration deskew calibration on all virtual channels 0b1XX00000: Periodic deskew calibration generated by virtual channel 0 0b1XX00001: Periodic deskew calibration generated by virtual channel 1 0b1XX00010: Periodic deskew calibration generated by virtual channel 2 0b1XX00011: Periodic deskew calibration

BITFIELD	BITS	DESCRIPTION	DECODE
			generated by virtual channel 3 0b1XX00100: Periodic deskew calibration generated by virtual channel 4 0b1XX00101: Periodic deskew calibration generated by virtual channel 5 0b1XX00110: Periodic deskew calibration generated by virtual channel 6 0b1XX00111: Periodic deskew calibration generated by virtual channel 7 0b1XX01000: Periodic deskew calibration generated by virtual channel 8 0b1XX01001: Periodic deskew calibration generated by virtual channel 9 0b1XX01010: Periodic deskew calibration generated by virtual channel 10 0b1XX01011: Periodic deskew calibration generated by virtual channel 11 0b1XX01100: Periodic deskew calibration generated by virtual channel 12 0b1XX01101: Periodic deskew calibration generated by virtual channel 13 0b1XX01110: Periodic deskew calibration generated by virtual channel 14 0b1XX01111: Periodic deskew calibration generated by virtual channel 15

MIPI_TX51 (0x473)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
MODE_DT	3	MIPI Tx enable 24-bit packing of 8-bit MIPI UDP	0x0: Disable 24-bit packing of 8-bit MIPI UDP 0x1: Enable 24-bit packing of 8-bit MIPI UDP
ALT_MEM_MAP10	2	Alternative memory map enable for 10-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP8	1	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP12	0	Alternative memory map enable for 12-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

MIPI_TX1 (0x481)

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7:0	MIPI VS short packet counter mode	0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter

MIPI_TX2 (0x482)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	MIPI TX status. The register is split into three decode segments: bit [0] SYNC mode enable. bit [1] Video sync flag bit [2] Loss of video sync flag	0bXXXXXXX0: SYNC mode disabled 0bXXXXXXX1: SYNC mode enabled 0bXXXXXX0X: Video channels not in-sync 0bXXXXXX1X: Video channels in-sync 0bXXXXX0XX: No loss of video sync 0bXXXXX1XX: Video sync lost after last read of this register or RESET.

MIPI_TX3 (0x483)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	DPHY deskew initial calibration control. The register is split into six decode segments: bit [7] Selects auto-initial deskew calibration on or off bit [6] Reserved bit [5] Any bit change initiates an initial calibration if bit [4] = 1 bit [4] Selects manual initial on or off bit [3] Reserved bit [2:0] Selects initial deskew width	0bXXXXX000: Initial deskew width = 1*32k UI 0bXXXXX001: Initial deskew width = 2*32k UI 0bXXXXX010: Initial deskew width = 3*32k UI 0bXXXXX011: Initial deskew width = 4*32k UI 0bXXXXX100: Initial deskew width = 5*32k UI 0bXXXXX101: Initial deskew width = 6*32k UI 0bXXXXX110: Initial deskew width = 7*32k UI 0bXXXXX111: Initial deskew width = 8*32k UI 0bXXXX0XXX: Reserved 0bXXXX1XXX: Reserved 0bXXX0XXXX: Manual initial off 0bXXX1XXXX: Manual initial on 0bXX0XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration

BITFIELD	BITS	DESCRIPTION	DECODE
			0bXX1XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bX0XXXXXX: Reserved 0bX1XXXXXX: Reserved 0b0XXXXXXX: Auto initial deskew off 0b1XXXXXXX: Auto initial deskew on

MIPI_TX4 (0x484)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_PER	7:0	DPHY periodic deskew calibration control. The register is split into four decode segments: bit [7] Selects periodic deskew calibration on or off bit [6] Selects generation on rising or falling edge of VS bit [5:3] Selects periodic interval bit [2:0] Selects periodic deskew width	0bXXXXX000: Periodic deskew width = 1k UI 0bXXXXX001: Periodic deskew width = 2k UI 0bXXXXX010: Periodic deskew width = 3k UI 0bXXXXX011: Periodic deskew width = 4k UI 0bXXXXX100: Periodic deskew width = 5k UI 0bXXXXX101: Periodic deskew width = 6k UI 0bXXXXX110: Periodic deskew width = 7k UI 0bXXXXX111: Periodic deskew width = 8k UI 0bXX000XXX: Periodic deskew calibration generated every frame 0bXX001XXX: Periodic deskew calibration generated every 2 frames 0bXX010XXX: Periodic deskew calibration generated every 4 frames 0bXX011XXX: Periodic deskew calibration generated every 8 frames 0bXX100XXX: Periodic deskew calibration generated every 16 frames 0bXX101XXX: Periodic deskew calibration generated every 32 frames 0bXX110XXX: Periodic deskew calibration generated every 64 frames 0bXX111XXX: Periodici deskew calibration generated every 128 frames 0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS 0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS 0b0XXXXXXX: Periodic deskew calibration off 0b1XXXXXXX: Periodic deskew calibration on

MIPI_TX5 (0x485)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_PRE[7:0]							
Reset	0x71							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_PRE	7:0	Number of MIPI byte clocks to wait before enabling HS data	0xXX: Number of MIPI byte clocks

MIPI_TX6 (0x486)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_POST[7:0]							
Reset	0x19							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_POST	7:0	Number of MIPI byte clocks to hold clock active after data	0xXX: Number of MIPI byte clocks

MIPI_TX7 (0x487)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TX_GAP[7:0]							
Reset	0x1C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TX_GAP	7:0	Number of MIPI byte clocks to wait after the HS clock has entered low-power (LP) mode before enabling it again for the next transmission	0xXX: Number of MIPI byte clocks

MIPI_TX8 (0x488)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_L	7:0	Low byte of CSI2 transmit wake-up	0xXX: Number of MIPI byte clocks

MIPI_TX9 (0x489)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_M[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAK	7:0	Middle byte of CSI2 transmit wake-up	0xXX: Number of MIPI byte clocks

BITFIELD	BITS	DESCRIPTION	DECODE
EUP_M			

MIPI_TX10 (0x48A)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		–	–	CSI_VCX_EN	CSI2_TWAKEUP_H[2:0]		
Reset	0b11		–	–	0b0	0b000		
Access Type	Write, Read		–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	Set number of MIPI data lanes	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes 0b11: Four data lanes
CSI_VCX_EN	3	Enables VC extension	0x0: Disable VC extension 0x1: Enable VC extension
CSI2_TWAKEUP_H	2:0	High bits of CSI2 transmit wake-up	0xXX: Number of MIPI byte clocks

MIPI_TX11 (0x48B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable MAP_SRC_0 and MAP_DST_0 registers 0xX2: Enable MAP_SRC_1 and MAP_DST_1 registers 0xX4: Enable MAP_SRC_2 and MAP_DST_2 registers 0xX8: Enable MAP_SRC_3 and MAP_DST_3 registers 0x1X: Enable MAP_SRC_4 and MAP_DST_4 registers 0x2X: Enable MAP_SRC_5 and MAP_DST_5 registers 0x4X: Enable MAP_SRC_6 and MAP_DST_6 registers 0x8X: Enable MAP_SRC_7 and MAP_DST_7 registers

MIPI_TX12 (0x48C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable MAP_SRC_8 and MAP_DST_8 registers 0xX2: Enable MAP_SRC_9 and MAP_DST_9 registers 0xX4: Enable MAP_SRC_10 and MAP_DST_10 registers 0xX8: Enable MAP_SRC_11 and MAP_DST_11 registers 0x1X: Enable MAP_SRC_12 and MAP_DST_12 registers 0x2X: Enable MAP_SRC_13 and MAP_DST_13 registers 0x4X: Enable MAP_SRC_14 and MAP_DST_14 registers 0x8X: Enable MAP_SRC_15 and MAP_DST_15 registers

MIPI_TX13 (0x48D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Mapping source register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 0

MIPI_TX14 (0x48E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Mapping destination register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 0

MIPI_TX15 (0x48F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Mapping source register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 1

MIPI_TX16 (0x490)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Mapping destination register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 1

MIPI_TX17 (0x491)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Mapping source register 2. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 2

MIPI_TX18 (0x492)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Mapping destination register 2. The register is split into two decode segments:	0xXX: VC and DT destination for map 2

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX19 (0x493)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Mapping source register 3. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 3

MIPI_TX20 (0x494)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Mapping destination register 3. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 3

MIPI_TX21 (0x495)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Mapping source register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 4

MIPI_TX22 (0x496)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Mapping destination register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 4

MIPI_TX23 (0x497)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Mapping source register 5. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 5

MIPI_TX24 (0x498)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Mapping destination register 5. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 5

MIPI_TX25 (0x499)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Mapping source register 6. The register is split into two decode segments:	0xXX: VC and DT source for map 6

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX26 (0x49A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Mapping destination register 6. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 6

MIPI_TX27 (0x49B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Mapping source register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 7

MIPI_TX28 (0x49C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Mapping destination register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 7

MIPI_TX29 (0x49D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Mapping source register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 8

MIPI_TX30 (0x49E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Mapping destination register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 8

MIPI_TX31 (0x49F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Mapping source register 9. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 9

MIPI_TX32 (0x4A0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Mapping destination register 9. The register is split into two decode segments:	0xXX: VC and DT destination for map 9

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX33 (0x4A1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Mapping source register 10. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 10

MIPI_TX34 (0x4A2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Mapping destination register 10. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 10

MIPI_TX35 (0x4A3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Mapping source register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 11

MIPI_TX36 (0x4A4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Mapping destination register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 11

MIPI_TX37 (0x4A5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Mapping source register 12. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 12

MIPI_TX38 (0x4A6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Mapping destination register 12. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 12

MIPI_TX39 (0x4A7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Mapping source register 13. The register is split into two decode segments:	0xXX: VC and DT source for map 13

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX40 (0x4A8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Mapping destination register 13. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 13

MIPI_TX41 (0x4A9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Mapping source register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 14

MIPI_TX42 (0x4AA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Mapping destination register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 14

MIPI_TX43 (0x4AB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Mapping source register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 15

MIPI_TX44 (0x4AC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Mapping destination register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 15

MIPI_TX45 (0x4AD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	CSI2 controller destination for MAP_SRC_3 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_2	5:4	CSI2 controller destination for MAP_SRC_2 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_1	3:2	CSI2 controller destination for MAP_SRC_1 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_0	1:0	CSI2 controller destination for MAP_SRC_0 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX46 (0x4AE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	CSI2 controller destination for MAP_SRC_7 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_6	5:4	CSI2 controller destination for MAP_SRC_6 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_5	3:2	CSI2 controller destination for MAP_SRC_5 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_4	1:0	CSI2 controller destination for MAP_SRC_4 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX47 (0x4AF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	CSI2 controller destination for MAP_SRC_11 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_10	5:4	CSI2 controller destination for MAP_SRC_10 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_9	3:2	CSI2 controller destination for MAP_SRC_9 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_8	1:0	CSI2 controller destination for MAP_SRC_8 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX48 (0x4B0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	CSI2 controller destination for MAP_SRC_15 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_14	5:4	CSI2 controller destination for MAP_SRC_14 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_13	3:2	CSI2 controller destination for MAP_SRC_13 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_12	1:0	CSI2 controller destination for MAP_SRC_12 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX49 (0x4B1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_CON[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	Concatenation register for sync mode settings. The register is split into four decode segments: bit [7] Enable 4WxH or Wx4H bit [6] Reserved bit [5:4] Master video stream number. This is the first line to concatenate. All others follow in order bit [3:0] Each bit selects a video stream to concatenate	0bXXXXXXX1: Concatenate video stream 0 0bXXXXXX1X: Concatenate video stream 1 0bXXXXX1XX: Concatenate video stream 2 0bXXXX1XXX: Concatenate video stream 3 0bXX00XXXX: Select video stream 0 as master 0bXX01XXXX: Select video stream 1 as master 0bXX10XXXX: Select video stream 2 as master 0bXX11XXXX: Select video stream 3 as master 0b0XXXXXXX: Enable Wx4H mode 0b1XXXXXXX: Enable 4WxH mode

MIPI_TX50 (0x4B2)

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	Periodic deskew select register. The register is split into three decode segments: bit [7] Select periodic deskew calibration for one or all virtual channels bit [6:5] Reserved bit [4:0] Virtual channel to generate periodic deskew calibration when only one channel is selected by bit [7]	0b0XXXXXXX: Generate periodic calibration deskew calibration on all virtual channels 0b1XX00000: Periodic deskew calibration generated by virtual channel 0 0b1XX00001: Periodic deskew calibration generated by virtual channel 1 0b1XX00010: Periodic deskew calibration generated by virtual channel 2 0b1XX00011: Periodic deskew calibration generated by virtual channel 3 0b1XX00100: Periodic deskew calibration generated by virtual channel 4 0b1XX00101: Periodic deskew calibration generated by virtual channel 5 0b1XX00110: Periodic deskew calibration generated by virtual channel 6 0b1XX00111: Periodic deskew calibration generated by virtual channel 7 0b1XX01000: Periodic deskew calibration generated by virtual channel 8 0b1XX01001: Periodic deskew calibration generated by virtual channel 9 0b1XX01010: Periodic deskew calibration generated by virtual channel 10 0b1XX01011: Periodic deskew calibration generated by virtual channel 11 0b1XX01100: Periodic deskew calibration generated by virtual channel 12 0b1XX01101: Periodic deskew calibration generated by virtual channel 13 0b1XX01110: Periodic deskew calibration generated by virtual channel 14 0b1XX01111: Periodic deskew calibration generated by virtual channel 15

MIPI_TX51 (0x4B3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

BITFIELD	BITS	DESCRIPTION	DECODE
MODE_DT	3	MIPI TX enable 24-bit packing of 8-bit MIPI UDP	0x0: Disable 24-bit packing of 8-bit MIPI UDP 0x1: Enable 24-bit packing of 8-bit MIPI UDP
ALT_MEM_MAP10	2	Alternative memory map enable for 10-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP8	1	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP12	0	Alternative memory map enable for 12-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

MIPI_TX11 (0x4CB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable MAP_SRC_0 and MAP_DST_0 registers 0xX2: Enable MAP_SRC_1 and MAP_DST_1 registers 0xX4: Enable MAP_SRC_2 and MAP_DST_2 registers 0xX8: Enable MAP_SRC_3 and MAP_DST_3 registers 0x1X: Enable MAP_SRC_4 and MAP_DST_4 registers 0x2X: Enable MAP_SRC_5 and MAP_DST_5 registers 0x4X: Enable MAP_SRC_6 and MAP_DST_6 registers 0x8X: Enable MAP_SRC_7 and MAP_DST_7 registers

MIPI_TX12 (0x4CC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x and MAP_DPHY_DST_x) for the current video stream. Non matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0xX1: Enable MAP_SRC_8 and MAP_DST_8 registers 0xX2: Enable MAP_SRC_9 and MAP_DST_9 registers 0xX4: Enable MAP_SRC_10 and MAP_DST_10 registers 0xX8: Enable MAP_SRC_11 and MAP_DST_11 registers 0x1X: Enable MAP_SRC_12 and MAP_DST_12

BITFIELD	BITS	DESCRIPTION	DECODE
			registers 0x2X: Enable MAP_SRC_13 and MAP_DST_13 registers 0x4X: Enable MAP_SRC_14 and MAP_DST_14 registers 0x8X: Enable MAP_SRC_15 and MAP_DST_15 registers

MIPI_TX13 (0x4CD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Mapping source register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 0

MIPI_TX14 (0x4CE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Mapping destination register 0. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 0

MIPI_TX15 (0x4CF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Mapping source register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 1

MIPI_TX16 (0x4D0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Mapping destination register 1. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 1

MIPI_TX17 (0x4D1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Mapping source register 2. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 2

MIPI_TX18 (0x4D2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Mapping destination register 2. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 2

MIPI_TX19 (0x4D3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Mapping source register 3. The register is split into two decode segments:	0xXX: VC and DT source for map 3

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX20 (0x4D4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Mapping destination register 3. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 3

MIPI_TX21 (0x4D5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Mapping source register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 4

MIPI_TX22 (0x4D6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Mapping destination register 4. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 4

MIPI_TX23 (0x4D7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Mapping source register 5. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 5

MIPI_TX24 (0x4D8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Mapping destination register 5. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 5

MIPI_TX25 (0x4D9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Mapping source register 6. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 6

MIPI_TX26 (0x4DA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Mapping destination register 6. The register is split into two decode segments:	0xXX: VC and DT destination for map 6

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX27 (0x4DB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Mapping source register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 7

MIPI_TX28 (0x4DC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Mapping destination register 7. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 7

MIPI_TX29 (0x4DD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Mapping source register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 8

MIPI_TX30 (0x4DE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Mapping destination register 8. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 8

MIPI_TX31 (0x4DF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Mapping source register 9. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 9

MIPI_TX32 (0x4E0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Mapping destination register 9. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 9

MIPI_TX33 (0x4E1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Mapping source register 10. The register is split into two decode segments:	0xXX: VC and DT source for map 10

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX34 (0x4E2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Mapping destination register 10. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 10

MIPI_TX35 (0x4E3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Mapping source register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 11

MIPI_TX36 (0x4E4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Mapping destination register 11. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 11

MIPI_TX37 (0x4E5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Mapping source register 12. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 12

MIPI_TX38 (0x4E6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Mapping destination register 12. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 12

MIPI_TX39 (0x4E7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Mapping source register 13. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 13

MIPI_TX40 (0x4E8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Mapping destination register 13. The register is split into two decode segments:	0xXX: VC and DT destination for map 13

BITFIELD	BITS	DESCRIPTION	DECODE
		bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	

MIPI_TX41 (0x4E9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Mapping source register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 14

MIPI_TX42 (0x4EA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Mapping destination register 14. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 14

MIPI_TX43 (0x4EB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Mapping source register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT source for map 15

MIPI_TX44 (0x4EC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Mapping destination register 15. The register is split into two decode segments: bit [7:6] VC - Virtual channel bit [5:0] DT - Data type	0xXX: VC and DT destination for map 15

MIPI_TX45 (0x4ED)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	CSI2 controller destination for MAP_SRC_3 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_2	5:4	CSI2 controller destination for MAP_SRC_2 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_1	3:2	CSI2 controller destination for MAP_SRC_1 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_0	1:0	CSI2 controller destination for MAP_SRC_0 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX46 (0x4EE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	CSI2 controller destination for MAP_SRC_7 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_6	5:4	CSI2 controller destination for MAP_SRC_6 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_5	3:2	CSI2 controller destination for MAP_SRC_5 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_4	1:0	CSI2 controller destination for MAP_SRC_4 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX47 (0x4EF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	CSI2 controller destination for MAP_SRC_11 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_10	5:4	CSI2 controller destination for MAP_SRC_10 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_9	3:2	CSI2 controller destination for MAP_SRC_9 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_8	1:0	CSI2 controller destination for MAP_SRC_8 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX48 (0x4F0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	CSI2 controller destination for MAP_SRC_15 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1

BITFIELD	BITS	DESCRIPTION	DECODE
			0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_14	5:4	CSI2 controller destination for MAP_SRC_14 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_13	3:2	CSI2 controller destination for MAP_SRC_13 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3
MAP_DPHY_DEST_12	1:0	CSI2 controller destination for MAP_SRC_12 and MAP_DST_0 mapping regs	0b00: Map to DPHY0 0b01: Map to DPHY1 0b10: Map to DPHY2 0b11: Map to DPHY3

MIPI_TX49 (0x4F1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_CON[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	Concatenation register for sync mode settings. The register is split into four decode segments: bit [7] Enable 4WxH or Wx4H bit [6] Reserved bit [5:4] Master video stream number. This is the first line to concatenate. All others follow in order bit [3:0] Each bit selects a video stream to concatenate	0bXXXXXXX1: Concatenate video stream 0 0bXXXXXX1X: Concatenate video stream 1 0bXXXXX1XX: Concatenate video stream 2 0bXXXX1XXX: Concatenate video stream 3 0bXX00XXXX: Select video stream 0 as master 0bXX01XXXX: Select video stream 1 as master 0bXX10XXXX: Select video stream 2 as master 0bXX11XXXX: Select video stream 3 as master 0b0XXXXXXX: Enable Wx4H mode 0b1XXXXXXX: Enable 4WxH mode

MIPI_TX51 (0x4F3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
MODE_DT	3	MIPI TX enable 24-bit packing of 8-bit MIPI UDP	0x0: Disable 24-bit packing of 8-bit MIPI UDP 0x1: Enable 24-bit packing of 8-bit MIPI UDP
ALT_MEM_MAP10	2	Alternative memory map enable for 10-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_MAP8	1	Alternative memory map enable for 8-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled
ALT_MEM_MAP12	0	Alternative memory map enable for 12-bit DT	0b0: Alternate memory map disabled 0b1: Alternate memory map enabled

MIPI_TX_EXT0 (0x500)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_0_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT1 (0x501)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_1_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT2 (0x502)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_2_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT3 (0x503)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_3_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT4 (0x504)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_4_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT5 (0x505)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_5_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT6 (0x506)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:5	Mapping register source VC High 3 bits for	0bXXX: Mapping register source VC High 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
_H		extended mode	
MAP_DST_6_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT7 (0x507)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_7_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT8 (0x508)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_8_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT9 (0x509)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_9_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT10 (0x50A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_10_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT11 (0x50B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_11_H	4:2	Mapping register destination VC High 3 bits for extended mode	0bXXX: Mapping register destination VC High 3 bits

MIPI_TX_EXT12 (0x50C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_12_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT13 (0x50D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
3_H		extended mode	
MAP_DST_13_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT14 (0x50E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_14_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT15 (0x50F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_15_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT0 (0x510)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_0_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT1 (0x511)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_1_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT2 (0x512)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_2_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT3 (0x513)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_3_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT4 (0x514)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
_H		extended mode	
MAP_DST_4_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT5 (0x515)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_5_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT6 (0x516)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_6_H	4:2	Mapping register destination VC High 3 bits for extended mode	0bXXX: Mapping register destination VC High 3 bits

MIPI_TX_EXT7 (0x517)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_7_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT8 (0x518)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_8_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT9 (0x519)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_9_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT10 (0x51A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_10_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT11 (0x51B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
1_H		extended mode	
MAP_DST_11_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT12 (0x51C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_12_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT13 (0x51D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_13_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT14 (0x51E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_14_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT15 (0x51F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_15_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT0 (0x520)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0_H	7:5	Mapping registersource VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_0_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT1 (0x521)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_1_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT2 (0x522)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
_H		extended mode	
MAP_DST_2_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT3 (0x523)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_3_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT4 (0x524)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_4_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT5 (0x525)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_5_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT6 (0x526)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_6_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT7 (0x527)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_7_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT8 (0x528)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_8_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT9 (0x529)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
_H		extended mode	
MAP_DST_9_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT10 (0x52A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC hig.h 3 bits
MAP_DST_10_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT11 (0x52B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_11_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT12 (0x52C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_12_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT13 (0x52D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_13_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT14 (0x52E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_14_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT15 (0x52F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_15_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT0 (0x530)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
_H		extended mode	
MAP_DST_0_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT1 (0x531)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_1_H	4:2	Mapping register destination VC High 3 bits for extended mode	0bXXX: Mapping register destination VC High 3 bits

MIPI_TX_EXT2 (0x532)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_2_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT3 (0x533)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_3_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT4 (0x534)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_4_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT5 (0x535)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_5_H	4:2	Mapping register destination VC High 3 bits for extended mode	0bXXX: Mapping register destination VC High 3 bits

MIPI_TX_EXT6 (0x536)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_6_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT7 (0x537)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
_H		extended mode	
MAP_DST_7_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT8 (0x538)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_8_H	4:2	Mapping register destination VC High 3 bits for extended mode	0bXXX: Mapping register destination VC High 3 bits

MIPI_TX_EXT9 (0x539)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC High 3 bits
MAP_DST_9_H	4:2	Mapping register destination VC High 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT10 (0x53A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_10_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT11 (0x53B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11_H	7:5	Mapping register source VC High 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_11_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC High 3 bits

MIPI_TX_EXT12 (0x53C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_12_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT13 (0x53D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_13_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT14 (0x53E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:5	Mapping register source VC high 3 bits for	0bXXX: Mapping register source VC high 3 bits

BITFIELD	BITS	DESCRIPTION	DECODE
4_H		extended mode	
MAP_DST_14_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

MIPI_TX_EXT15 (0x53F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0b000			0b000			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15_H	7:5	Mapping register source VC high 3 bits for extended mode	0bXXX: Mapping register source VC high 3 bits
MAP_DST_15_H	4:2	Mapping register destination VC high 3 bits for extended mode	0bXXX: Mapping register destination VC high 3 bits

UART_PT_0 (0x548)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_1_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_L	7:0	Low byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits) Set BITLEN_MAN_CFG_1 to 1 to use this value.	0xXX: Low byte of custom UART bit length for pass-through UART Channel 1

UART_PT_1 (0x549)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_1_H[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_1_H	5:0	High byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (MSB 6 bits) Set BITLEN_MAN_CFG_1 to 1 to use this value.	0xXX: High byte of custom UART bit length for pass-through UART Channel 1

UART_PT_2 (0x54A)

BIT	7	6	5	4	3	2	1	0
Field	BITLEN_PT_2_L[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_L	7:0	Low byte of custom UART bit length for pass-through UART Channel 2. Set this register to the UART bit length divided by 6.666ns (LSB 8 bits) Set BITLEN_MAN_CFG_2 to 1 to use this value.	0xXX: Low byte of custom UART bit length for pass-through UART Channel 2

UART_PT_3 (0x54B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BITLEN_PT_2_H[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BITLEN_PT_2_H	5:0	High byte of custom UART bit length for pass-through UART Channel 1. Set this register to the UART bit length divided by 6.666ns (MSB 6 bits) Set BITLEN_MAN_CFG_1 to 2 to use this value.	0xXX: High byte of custom UART bit length for pass-through UART Channel 2

I2C_PT_4 (0x550)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_1	7:1	I^2C address translator source A When I^2C device address matches SRC_A_1, internal I^2C master replaces the device address by DST_A_1.	0xXX: I^2C address translator source A

I2C_PT_5 (0x551)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_1	7:1	I²C address translator destination A See the description of SRC_A_1.	0xXX: I²C address translator destination A

I2C_PT_6 (0x552)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_1	7:1	I²C address translator source B When I²C device address matches SRC_B_1, internal I²C master replaces the device address by DST_B_1.	0xXX: I²C address translator source B

I2C_PT_7 (0x553)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_1[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_1	7:1	I²C address translator destination B See the description of SRC_B_1.	0xXX: I²C address translator destination B

I2C_PT_8 (0x554)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_2[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_2	7:1	I²C address translator source A When I²C device address matches SRC_A_2, internal I²C master replaces the device address by DST_A_2.	0xXX: I²C address translator source A

I2C_PT_9 (0x555)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_2[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_2	7:1	I2C address translator destination A See the description of SRC_A_2.	0xXX: I2C address translator destination A

I2C_PT_11 (0x557)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_2[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_2	7:1	I2C address translator destination B See the description of SRC_B_2.	0xXX: I2C address translator destination B

BW_MEAS_0 (0x559)

BIT	7	6	5	4	3	2	1	0
Field	BW_USE_THR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BW_USE_THR	7:0	Bandwith usage threshold When this is non-zero, bandwith usage (utilization) of the GMSL2 output is measured and reported at BW_INT bit and optionally at ERRB pin. Every 256 txclk cycles (every 0.85µs when link is running at 6G), the number of cycles used for packet transmission is counted and it is compared with the 8-bit value of this register. If BW_USE_LT = 0, BW_INT is asserted when usage is greater than the threshold. If BW_USE_LT = 1, BW_INT is asserted when usage is less than the threshold.

BW_MEAS_1 (0x55A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BW_USE_OEN	BW_INT	BW_USE_LINK	BW_USE_LT
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Read Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BW_USE_OEN	3	Set to 1 to output live bandwidth usage comparison at ERRB pin	0b0: Do not output live bandwidth usage comparison 0b1: Output live bandwidth usage comparison
BW_INT	2	Live bandwidth usage comparator output. Active only when BW_USE_LT = 1	0b0: Bandwidth usage is less than threshold 0b1: Bandwidth usage exceeds threshold
BW_USE_LI	1	Selects which link is monitored for bandwidth	0b0: Link A bandwidth usage monitored

BITFIELD	BITS	DESCRIPTION	DECODE
NK		usage. In Single or Reverse Split Link configurations (LINK_MODE=1,2, or 3) the below register decode values apply. In Dual-Link mode, the total of both links is monitored, so the decode values are irrelevant.	0b1: Link B bandwidth usage monitored
BW_USE_LT	0	Determines whether BW_INT is asserted when bandwidth exceeds threshold. See BW_USE_THR description.	0b0: BW_INT not asserted when bandwidth usage exceeds threshold 0b1: BW_INT asserted when bandwidth usage exceeds threshold

CNT4 (0x55C)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR0[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR0	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected in video stream X

CNT5 (0x55D)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR1[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR1	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected in video stream Y

CNT6 (0x55E)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR2[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR2	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected in video stream Z

CNT7 (0x55F)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR3[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR3	7:0	Total number of video pixel CRC errors detected at video streams. Reset after reading or with the rising edge of LOCK.	0xXX: Total number of video pixel CRC errors detected in video stream U

GMSL1_2 (0xB02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SRNG[1:0]	
Reset	–	–	–	–	–	–	0b11	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SRNG	1:0	Serial data rate range	0x0: 0.5 to 1 Gbps 0x1: 1 to 1.5 Gbps 0x2: 1.5 to 4.5 Gbps 0x3: Autodetect

GMSL1_4 (0xB04)

BIT	7	6	5	4	3	2	1	0
Field	–	OUTENB	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
Reset	–	0b0	0b0	–	0b0	–	0b1	0b1
Access Type	–	Write, Read	Write, Read	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OUTENB	6	Disables outputs	0b0: Outputs enabled 0b1: Outputs disabled
PRBSEN	5	PRBS test enable (In HIBW mode set PRBS_TYPE = 0)	0b0: Set device normal operation 0b1: Enable PRBS test
CC_PORT_SEL	3	Selects which I²C/UART port is connected to this link	0b0: Port 0 (SDA0_RX0, SCL0_TX0) 0b1: Port 1 (SDA1_RX1, SCL1_TX1)
REVCCEN	1	Enables reverse control channel from deserializer	0b0: Disable reverse control channel receiver 0b1: Enable reverse control channel receiver
FWDCCEN	0	Enables forward control channel to deserializer	0b0: Disable forward control channel transmitter 0b1: Enable forward control channel transmitter

GMSL1_5 (0xB05)

BIT	7	6	5	4	3	2	1	0
Field	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
Reset	0b0	0x0	0b1	0b1	0x9			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
I2CMETHOD	7	I^2C Method - Skips register address when converting UART to I^2C	0b0: Send the register address during UART-to-I^2C conversion 0b1: Do not send the register address during UART-to- I^2C conversion
NO_REM_MST	6	When set to 1, indicates that there is no I^2C master on remote side so this (local) chip should ignore any I^2C packet initiation (start condition) from remote side	0x0: I^2C master may or may not be present on remote side 0x1: No I^2C master on remote side
HVTR_MODE	5	HV tracking allows continuous HSYNC format	0b0: Use partial periodic HV tracking 0b1: Use partial and full perioodic HV tracking
EN_EQ	4	Enables equalizer for manual and adaptive modes	0b0: Disable equalization 0b1: Enable equalization
EQTUNE	3:0	Equalizer boost level at 750 MHz (effective when adaptive EQ is turned off)	0b0000: 1.6 dB manual EQ setting 0b0001: 2.1 dB manual EQ setting 0b0010: 2.8 dB manual EQ setting 0b0011: 3.5 dB manual EQ setting 0b0100: 4.3 dB manual EQ setting 0b0101: 5.2 dB manual EQ setting 0b0110: 6.3 dB manual EQ setting 0b0111: 7.3 dB manual EQ setting 0b1000: 8.5 dB manual EQ setting 0b1001: 9.7 dB manual EQ setting 0b1010: 11.0 dB manual EQ setting 0b1011: 12.2 dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_6 (0xB06)

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
Reset	0b0	0b1	0b1	0b0	0b1	0b111		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse channel high immunity mode (initial value set by the HIM CFG value at power-up)	0b0: Reverse channel high immunity mode disabled 0b1: Reverse channel high immunity mode enabled
MAX_RT_EN	6	Maximum retransmission limit enable	0b0: Disable maximum retransmission limit

BITFIELD	BITS	DESCRIPTION	DECODE
			0b1: Enable maximum retransmission limit
I2C_RT_EN	5	I²C retransmission enable	0b0: Disable I²C retransmission 0b1: Enable I²C retransmission enable
GPI_COMP_EN	4	GPI skew compensation enable	0b0: Disable GPI skew compensation 0b1: Enable GPI skew compensation
GPI_RT_EN	3	GPI retransmission enable	0b0: Disable GPI retransmission 0b1: Enable GPI retransmission
HV_SRC	2:0	HS_VS bit selection	0b000: Use D18/D19 for HS/VS (use this setting when the serializer is a 3.125Gbps device or if HIBW mode is used; otherwise, this setting is for use with the MAX9273 when DBL = 0 or HVEN = 1) 0b001: Use D14/D15 for HS/VS (for use with the MAX9271/ MAX96705 when DBL = 0 or HVEN = 1) 0b010: Use D12/D13 for HS/VS (for use with the MAX96707 when DBL = 0 or HVEN = 1) 0b011: Use D0/D1 for HS/VS (for use with the MAX9271/ MAX9273/MAX96705/MAX96707 when DBL = 1 and HVEN = 0) 0b100: Reserved 0b101: Reserved 0b110: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96707) 0b111: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96705)

GMSL1_7 (0xB07)

BIT	7	6	5	4	3	2	1	0
Field	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	Double-output mode	0b0: Use single-rate output 0b1: Use double-rate output (2x word rate at 1/2x width)
DRS	6	Data rate select	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
BWS	5	Bus width select: BWS=0, HIBW=0: 24 total bits, 2 bits are used for control, 22 bits are usable by video BWS=0, HIBW=1: 27 total bits, 3 bits are used for control, 24 bits are usable by video BWS=1, HIBW=0: 32 total bits, 2 bits are used for control, 30 bits are usable by video	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)
HIBW	3	High-bandwidth mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS =

BITFIELD	BITS	DESCRIPTION	DECODE
			0)
HVEN	2	HS/VS encoding enable	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel error detection type (this is controllable by pin when LCCEN = 0)	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

GMSL1_8 (0xB08)

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
Reset	–	–	0b1	0b0	–	0b0	0b01	
Access Type	–	–	Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_EN	5	Enables GPI-to-GPO signal transmission to serializer	0b0: Disable GPI-to-GPO transmission 0b1: Enable GPI-to-GPO transmission
EN_FSYNC_TX	4	Enables frame sync signal transmission	0b0: Disable frame sync signal transmission 0b1: Enable frame sync signal transmission
PKTCC_EN	2	Enables packet-based control-channel mode	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode
CC_CRC_LENGTH	1:0	Control channel CRC length	0b00: 1-bit CRC 0b01: 5-bit CRC 0b10: 8-bit CRC 0b11: Reserved

GMSL1_D (0xB0D)

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	–	–	–	–	HS_TRACK_FSYNC	–	–
Reset	0b0	–	–	–	–	0b0	–	–
Access Type	Write, Read	–	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	Enable I^2C-to-I^2C slave local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available
HS_TRACK_FSYNC	2	This bit selects whether to allow infinite-length vertical blanking or to reset HLOCKED with VLOCKED.	0x0: Allow infinite length vertical blanking 0x1: Reset HLOCKED with VLOCKED

GMSL1_E (0xB0E)

BIT	7	6	5	4	3	2	1	0
Field	DET_THR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_THR	7:0	Threshold for detected errors	0xXX: Number of errors for detected error threshold

GMSL1_F (0xB0F)

BIT	7	6	5	4	3	2	1	0
Field	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
Reset	–	0b0	0b0	0b0	0b1	–	–	0b1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_DE_FILT	6	Enable glitch filtering on DE	0b0: Disable DE glitch filtering 0b1: Enable DE glitch filtering
EN_HS_FILT	5	Enable glitch filtering on HS	0b0: Disable HS glitch filtering 0b1: Enable HS glitch filtering
EN_VS_FILT	4	Enable glitch filtering on VS	0b0: Disable VS glitch filtering 0b1: Enable VS glitch filtering
DE_EN	3	Enable processing separate HS and DE signals	0b0: Disable processing HS and DE signals 0b1: Enable processing HS and DE signals
PRBS_TYPE	0	PRBS type select (n HIBW mode, set PRBS_TYPE = 0)	0b0: GMSL legacy style PRBS test 0b1: MAX9272 style PRBS test

GMSL1_10 (0xB10)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
Reset	0b00		0b0	0x1				0b0
Access Type	Write, Read		Write, Read	Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_TYPE	7:6	Reverse channel generated error type	0b00: Random 0b01: Short burst 0b10: Long burst 0b11: Long burst
RCEG_BOUND	5	Reverse channel generated error boundary (Effective when RCEG_TYPE = 0x)	0b0: Errors are unbounded to symbols 0b1: Errors are bounded to symbols
RCEG_ERR_NUM	4:1	Number of RCEG errors generated with each request (Effective when RCEG_TYPE = 0x)	0xX: Number of errors generated per request
RCEG_EN	0	Enable reverse channel error generator	0b0: Disable reverse channel error generator

BITFIELD	BITS	DESCRIPTION	DECODE
			0b1: Enable reverse channel error generator enabled

GMSL1_11 (0xB11)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
Reset	0xF				0b00		0b00	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_RATE	7:4	Error generation rate in terms of bit time = $2^{-(RCEG\_ERR\_RATE+3)}$. (Effective when RCEG_TYPE = 0x)	0x0: Rate is 2^{-3} 0x1: Rate is 2^{-4} 0x2: Rate is 2^{-5} . . 0xF: Rate is 2^{-18}
RCEG_LO_BST_PRB	3:2	Long burst error probability. Effective when RCEG_TYPE = 10.	0b00: 1/1024 0b01: 1/128 0b10: 1/32 0b11: 1/8
RCEG_LO_BST_LEN	1:0	Long burst error length in terms of bit time. Effective when RCEG_TYPE = 10.	0b00: Continuous 0b01: 128 (~150µs) 0b10: 8192 (~9.83ms) 0b11: 1048576 (~1.26s)

GMSL1_12 (0xB12)

BIT	7	6	5	4	3	2	1	0
Field	–	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
Reset	–	0b1	0b01		0b0	–	0b1	0b0
Access Type	–	Write, Read	Write, Read		Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERR_EN	6	Enable reporting of (CC_CRC_ERR_CNT > 0) on the ERRB pin	0b0: Disable reporting of errors on ERRB 0b1: Enable reporting of errors on ERRB
LINE_CRC_LOC	5:4	Video line CRC insertion location	0b00: [1..4] 0x01: [5..8] 0x10: [9..12] 0x11: [13..16]
LINE_CRC_EN_GMSL1	3	Video line CRC enable	0b0: Disable video line CRC 0x1: Enable video line CRC
MAX_RT_ERR_EN	1	Enable reflection of maximum retransmission error on the ERRORB pin	0b0: Disable maximum retransmission error on the ERROR pin 0b1: Enable maximum retransmission error on the ERROR pin
RCEG_ERR_PER_EN	0	Periodic error generation enable. Effective when RCEG_TYPE = 0x.	0b0: Disable periodic error generator 0b1: Enable periodic error generator

GMSL1_13 (0xB13)

BIT	7	6	5	4	3	2	1	0
Field	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
Reset	0b1	0b1	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EN_G1	7	Eye-opening monitor (EOM) enable	0b0: Disable EOM 0x1: Enable EOM
EOM_PER_MODE_G1	6	Eye-opening monitor (EOM) periodic mode select	0b0: Set EOM to use non-periodic mode 0x1: Set EOM to use periodic mode
EOM_MAN_TRG_REQ_G1	5	Eye-opening monitor (EOM) manual trigger request. Valid on the rising edge of this bit when not in periodic mode.	0x0: Do not trigger EOM. 0x1: Manually trigger the EOM
EOM_MIN_THR_G1	4:0	Eye-opening minimum threshold (in terms of percent) for flagging ERRORB pin. (Percentages increment 3.125% per bitfield setting.)	0b00000: Disabled 0b00001: 3.125% 0b00010: 6.25% 0b00011: 9.375 . . 0b11111: 100%

GMSL1_14 (0xB14)

BIT	7	6	5	4	3	2	1	0
Field	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
Reset	0b1	0b0	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_EN	7	Adaptive equalization (AEQ) enable	0b0: Disable AEQ 0x1: Enable AEQ
AEQ_PER_MODE	6	Adaptive equalizer periodic mode select	0b0: Set AEQ to use non-periodic mode 0x1: Set AEQ to use periodic mode
AEQ_MAN_TRG_REQ	5	Enables adaptive equalizer manual fine tune request. Valid on the rising edge of this bit when not in periodic mode.	0x0: Do not trigger AEQ fine tuning 0x1: Manually trigger the AEQ fine tuning
EOM_PER_THR	4:0	Eye-opening threshold to trigger a fine tune operation	0b00000: Eye-opening threshold is disabled 0b10000: 50% eye-opening triggers fine-tune operation OTHER: Reserved

GMSL1_15 (0xB15)

BIT	7	6	5	4	3	2	1	0
Field	DET_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_ERR	7:0	Detected error counter	0xXX: Number of detected errors

GMSL1_16 (0xB16)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_ERR	7:0	PRBS error counter	0xXX: Number of detected PRBS errors

GMSL1_17 (0xB17)

BIT	7	6	5	4	3	2	1	0
Field	I2C_TIMED_OUT_GMSL1	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMED_OUT_GMSL1	7	I^2C channel timed out flag	0b0: I^2C channel not timed out 0b1: I^2C channel timed out
MAX_RT_ERR_I2C	6	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached
PRBS_OK	5	MAX9271/73 compatible PRBS test for link is completed normally. Check PRBS_ERR register for the PRBS success. For other SERDES read PRBS_ERR registers.	0b0: No MAX9271/MAX9273-compatible PRBS test completed 0b1: MAX9271/MAX9273-compatible PRBS test completed normally
GPI_IN	4	GPI pin level	0b0: GPI is input low 0b1: GPI is input high
MAX_RT_ERR_GPI	3	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

GMSL1_18 (0xB18)

BIT	7	6	5	4	3	2	1	0
Field	CC_RETR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_RETR_CNT	7:0	I^2C packet retransmission count	0xXX: Number of I^2C packets retransmitted

GMSL1_19 (0xB19)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-based control channel CRC error counter	0xXX: Number of control channel CRC errors

GMSL1_1A (0xB1A)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_CNT	7:0	Control channel number of generated errors	0xXX: Number of control channel generated errors

GMSL1_1B (0xB1B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LINE_CRC_ERR	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ERR	2	CRC error bit. Latched on error - cleared to 0 when read.	0b0: Video line CRC ok 0b1: Video line CRC mismatch detected

GMSL1_1C (0xB1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	EOM_EYE_WIDTH[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EYE_WIDTH	5:0	Measured eye-opening. Opening width = EOM_EYE_WIDTH/63 x 100%	0b000000: Width is 0% 0b000001: Width is 1/63 x 100% 0b000010: Width is 2/63 x 100% . . 0b11111: Width is 63/63 x 100%

GMSL1_1D (0xB1D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
Reset	–	–	–	0b0	0x0			
Access Type	–	–	–	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBOOST_DET	4	Under boost detected	0b0: Normal Operation 0x1: Underboost (at maximum AEQ gain) detected
AEQ_BST	3:0	Adaptive equalizer boost value. Selected adaptive equalizer value; settings correspond to gain at 750MHz	0b0000: 1.6 dB manual EQ setting 0b0001: 2.1 dB manual EQ setting 0b0010: 2.8 dB manual EQ setting 0b0011: 3.5 dB manual EQ setting 0b0100: 4.3 dB manual EQ setting 0b0101: 5.2 dB manual EQ setting 0b0110: 6.3 dB manual EQ setting 0b0111: 7.3 dB manual EQ setting 0b1000: 8.5 dB manual EQ setting 0b1001: 9.7 dB manual EQ setting 0b1010: 11.0 dB manual EQ setting 0b1011: 12.2 dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_20 (0xB20)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_0	7:0	Bits [7:0] of CRC output for the latest line	0xXX: CRC[7:0] of latest line

GMSL1_21 (0xB21)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_1	7:0	Bits [15:8] of CRC output for the latest line	0xXX: CRC[15:8] of latest line

GMSL1_22 (0xB22)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_2	7:0	Bits [23:16] of CRC output for the latest line	0xXX: CRC[23:16] of latest line

GMSL1_23 (0xB23)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_3	7:0	Bits [31:24] of CRC output for the latest line	0xXX: CRC[31:24] of latest line

GMSL1_96 (0xB96)

BIT	7	6	5	4	3	2	1	0
Field	CONV_GMSL1_DATATYPE[4:0]					DIS_HIBW_E	CONV_GMSL1_EN	DBL_ALIGN_TO
Reset	0b00000					0b0	0b0	0b1
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONV_GMSL1_DATATY	7:3	Convert from GMSL1 color format mapping to GMSL2 CSI transmitter color format	0x0: RGB888 OLDI

BITFIELD	BITS	DESCRIPTION	DECODE
PE			0x1: RGB565 0x2: RGB666 0x3: YUV 422 8-bit Mux mode (use yuv_8_10_mux_mode) 0x4: YUV 422 10-bit Mux mode (use yuv_8_10_mux_mode) 0x5: RAW8 single 0x6: RAW10 single 0x7: RAW12 single 0x8: RAW14 0x9: User-defined Generic 24-bit 0xA: User-defined YUV422 12-bit 0xB: User-defined Generic 8-bit 0xC 0xD 0xE 0xF 0x10: RGB888 VESA 0x11 0x12 0x13: YUV 422 8-bit Normal mode 0x14: YUV 422 10-bit Normal mode 0x15: RAW8 double (use alt_mem_map8) 0x16: RAW10 double (use alt_mem_map10) 0x17: RAW12 double (use alt_mem_map12) 0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E 0x1F
DIS_HIBW_E	2	Disables disparity error detection in HIBW	0b0: Enable disparity error detection 0b1: Disable disparity error detection
CONV_GMSL1_EN	1	Enables conversion from GMSL1 color format mapping to GMSL2 CSI transmitter	0b0: Disable conversion 0b1: Enable conversion
DBL_ALIGN_TO	0	HBM DBL mode type	0b0: DBL-Single mode with alignment 0b1: DBL-DBL mode with no alignment (d)

GMSL1_CA (0xBCA)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PHASELOCK	WBLOCK_G1	DATAOK
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PHASELOCK	2	CDR locked	0b0: CDR not locked 0b1: CDR locked
WBLOCK_G	1	Word boundary detected	0b0: No word boundary detected

BITFIELD	BITS	DESCRIPTION	DECODE
1			0b1: Word boundary detected
DATAOK	0	Data activity detected on the link	0b0: No data activity detected on the link 0b1: Data activity detected on the link

GMSL1_CB (0xBCB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOCKED_G1
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_G1	0	Link locked	0b0: Link not locked 0b1: Link locked

GMSL1_D1 (0xBD1)

BIT	7	6	5	4	3	2	1	0
Field	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
Reset	0x0			0x00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_OUT_ORD	7:5	Internal CNTL_OUT order to pins CNTL4 to CNTL0	0x0: 4, 3, 2, 1, 0 0x1: 3, 2, 1, 0, 4 0x2: 2, 1, 0, 4, 3 0x3: 1, 0, 4, 3, 2 0x4: 0, 1, 2, 3, 4 0x5: 1, 2, 3, 4, 0 0x6: 2, 3, 4, 0, 1 0x7: 3, 4, 0, 1, 2
CNTL_OUT_EN	4:0	CNTL output enable for CNTL 0, 1, 2, 3, 4	0bXXXX0: Disable control output 0 0bXXXX1: Enable control output 0 0bXXX0X: Disable control output 1 0bXXX1X: Enable control output 1 0bXX0XX: Disable control output 2 0bXX1XX: Enable control output 2 0bX0XXX: Disable control output 3 0bX1XXX: Enable control output 3 0b0XXXX: Disable control output 4 0b1XXXX: Enable control output 4

GMSL1_2 (0xC02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SRNG[1:0]	
Reset	–	–	–	–	–	–	0b11	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SRNG	1:0	Serial data rate range	0b00: 0.5 to 1 Gbps 0b01: 1 to 1.5 Gbps 0b10: 1.5 to 4.5 Gbps 0b11: Autodetect

GMSL1_4 (0xC04)

BIT	7	6	5	4	3	2	1	0
Field	–	OUTENB	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
Reset	–	0b0	0b0	–	0b0	–	0b1	0b1
Access Type	–	Write, Read	Write, Read	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OUTENB	6	Disables outputs	0b0: Outputs enabled 0b1: Outputs disabled
PRBSEN	5	PRBS test enable (In HIBW mode set PRBS_TYPE = 0)	0b0: Set device normal operation 0b1: Enable PRBS test
CC_PORT_SEL	3	Selects which I²C/UART port is connected to this link	0b0: Port 0 (SDA0_RX0, SCL0_TX0) 0b1: Port 1 (SDA1_RX1, SCL1_TX1)
REVCCEN	1	Enables reverse control channel from deserializer	0b0: Disable reverse control channel receiver 0b1: Enable reverse control channel receiver
FWDCCEN	0	Enables forward control channel to deserializer	0b0: Disable forward control channel transmitter 0b1: Enable forward control channel transmitter

GMSL1_5 (0xC05)

BIT	7	6	5	4	3	2	1	0
Field	I2CMETHOD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
Reset	0b0	0x0	0b1	0b1	0x9			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
I2CMETHOD	7	I²C Method - Skip register address when converting UART to I²C	0b0: Send the register address during UART-to-I²C conversion 0b1: Do not send the register address during UART-to-I²C conversion
NO_REM_MST	6	Sets to 1 to indicate that there is no I²C master on remote side so this (local) chip should ignore any I²C packet initiation (start condition) from remote side	0b0: I²C master may or may not be present on remote side 0b1: No I²C master on remote side
HVTR_MODE	5	HV tracking allows continuous HSYNC format	0b0: Use partial periodic HV tracking 0b1: Use partial and full perioodic HV tracking
EN_EQ	4	Enables equalizer for manual and adaptive modes	0b0: Disable equalization 0b1: Enable equalization
EQTUNE	3:0	Equalizer boost level at 750 MHz (effective when Adaptive EQ is turned off)	0b0000: 1.6 dB manual EQ setting 0b0001: 2.1 dB manual EQ setting 0b0010: 2.8 dB manual EQ setting

BITFIELD	BITS	DESCRIPTION	DECODE
			0b0011: 3.5 dB manual EQ setting 0b0100: 4.3 dB manual EQ setting 0b0101: 5.2 dB manual EQ setting 0b0110: 6.3 dB manual EQ setting 0b0111: 7.3 dB manual EQ setting 0b1000: 8.5 dB manual EQ setting 0b1001: 9.7 dB manual EQ setting 0b1010: 11.0 dB manual EQ setting 0b1011: 12.2 dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_6 (0xC06)

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
Reset	0b0	0b1	0b1	0b0	0b1	0b111		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse channel high immunity mode (initial value set by the HIM CFG value at power-up)	0b0: Reverse channel high immunity mode disabled 0b1: Reverse channel high immunity mode enabled
MAX_RT_EN	6	Maximum retransmission limit enable	0b0: Disable maximum retransmission limit 0b1: Enable maximum retransmission limit
I2C_RT_EN	5	I^2C retransmission enable	0b0: Disable I^2C retransmission 0b1: Enable I^2C retransmission enable
GPI_COMP_EN	4	GPI skew compensation enable	0b0: Disable GPI skew compensation 0b1: Enable GPI skew compensation
GPI_RT_EN	3	GPI retransmission enable	0b0: Disable GPI retransmission 0b1: Enable GPI retransmission
HV_SRC	2:0	HS_VS bit selection	0b000: Use D18/D19 for HS/VS (use this setting when the serializer is a 3.125Gbps device or if HIBW mode is used; otherwise, this setting is for use with the MAX9273 when DBL = 0 or HVEN = 1) 0b001: Use D14/D15 for HS/VS (for use with the MAX9271/ MAX96705 when DBL = 0 or HVEN = 1) 0b010: Use D12/D13 for HS/VS (for use with the MAX96707 when DBL = 0 or HVEN = 1) 0b011: Use D0/D1 for HS/VS (for use with the MAX9271/ MAX9273/MAX96705/MAX96707 when DBL = 1 and HVEN = 0) 0b100: Reserved 0b101: Reserved 0b110: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96707)

BITFIELD	BITS	DESCRIPTION	DECODE
			0b111: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96705)

GMSL1_7 (0xC07)

BIT	7	6	5	4	3	2	1	0
Field	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	Double-output mode	0b0: Use single-rate output 0b1: Use double-rate output (2x word rate at 1/2x width)
DRS	6	Data rate select	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
BWS	5	Bus width select BWS=0, HIBW=0: 24 total bits, 2 bits are used for control, 22 bits are usable by video BWS=0, HIBW=1: 27 total bits, 3 bits are used for control, 24 bits are usable by video BWS=1, HIBW=0: 32 total bits, 2 bits are used for control, 30 bits are usable by video	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)
HIBW	3	Enables high-bandwidth mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
HVEN	2	HS/VS encoding enable	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel error detection type (this is controllable by pin when LCCEN = 0)	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

GMSL1_8 (0xC08)

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
Reset	–	–	0b1	0b0	–	0b0	0b01	
Access Type	–	–	Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_EN	5	Enables GPI-to-GPO signal transmission to serializer	0b0: Disable GPI-to-GPO transmission 0b1: Enable GPI-to-GPO transmission
EN_FSYNC_TX	4	Enables frame sync signal transmission	0b0: Disable frame sync signal transmission 0b1: Enable frame sync signal transmission
PKTCC_EN	2	Packet-based control channel mode enable	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode
CC_CRC_LE	1:0	Control channel CRC length	0b00: 1-bit CRC

BITFIELD	BITS	DESCRIPTION	DECODE
NGTH			0b01: 5-bit CRC 0b10: 8-bit CRC 0b11: Reserved

GMSL1_D (0xC0D)

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	–	–	–	–	HS_TRACK_FSYNC	–	–
Reset	0b0	–	–	–	–	0b0	–	–
Access Type	Write, Read	–	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	Enables I^2C-to-I^2C slave local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available
HS_TRACK_FSYNC	2	Selects whether to allow infinite-length vertical blanking or to lose HLOCKED with VLOCKED.	0b0: Allow infinite length vertical blanking 0b1: Lose HLOCKED with VLOCKED

GMSL1_E (0xC0E)

BIT	7	6	5	4	3	2	1	0
Field	DET_THR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_THR	7:0	Threshold for detected errors	0xXX: Number of errors for detected error threshold

GMSL1_F (0xC0F)

BIT	7	6	5	4	3	2	1	0
Field	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
Reset	–	0b0	0b0	0b0	0b1	–	–	0b1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_DE_FILT	6	Enables glitch filtering on DE	0b0: Disable DE glitch filtering 0b1: Enable DE glitch filtering
EN_HS_FILT	5	Enables glitch filtering on HS	0b0: Disable HS glitch filtering 0b1: Enable HS glitch filtering
EN_VS_FILT	4	Enables glitch filtering on VS	0b0: Disable VS glitch filtering 0b1: Enable VS glitch filtering
DE_EN	3	Enables processing separate HS and DE	0b0: Disable processing HS and DE signals

BITFIELD	BITS	DESCRIPTION	DECODE
		signals	0b1: Enable processing HS and DE signals
PRBS_TYPE	0	PRBS type select (in HIBW mode, set PRBS_TYPE = 0)	0b0: GMSL legacy style PRBS test 0b1: MAX9272 style PRBS test

GMSL1_10 (0xC10)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
Reset	0b00		0b0	0x1				0b0
Access Type	Write, Read		Write, Read	Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_TYPE	7:6	Reverse channel generated error type	0b00: Random 0b01: Short burst 0b10: Long burst 0b11: Long burst
RCEG_BOUND	5	Reverse channel generated error boundary (Effective when RCEG_TYPE = 0x)	0b0: Errors are unbounded to symbols 0b1: Errors are bounded to symbols
RCEG_ERR_NUM	4:1	Number of RCEG errors generated with each request (Effective when RCEG_TYPE = 0x)	0xX: Number of errors generated per request
RCEG_EN	0	Enables reverse channel error generator	0b0: Disable reverse channel error generator 0b1: Enable reverse channel error generator enabled

GMSL1_11 (0xC11)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
Reset	0xF				0b00		0b00	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_RATE	7:4	Error generation rate in terms of bit time = $2^{-(RCEG\_ERR\_RATE+3)}$. (Effective when RCEG_TYPE = 0x)	0x0: Rate is 2^{-3} 0x1: Rate is 2^{-4} 0x2: Rate is 2^{-5} . . 0xF: Rate is 2^{-18}
RCEG_LO_BST_PRB	3:2	Long burst error probability. Effective when RCEG_TYPE = 10.	0b00: 1/1024 0b01: 1/128 0b10: 1/32 0b11: 1/8
RCEG_LO_BST_LEN	1:0	Long burst error length in terms of bit time. Effective when RCEG_TYPE = 10.	0b00: Continuous 0b01: 128 (~150µs) 0b10: 8192 (~9.83ms) 0b11: 1048576 (~1.26s)

GMSL1_12 (0xC12)

BIT	7	6	5	4	3	2	1	0
Field	–	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
Reset	–	0b1	0b01		0b0	–	0b1	0b0
Access Type	–	Write, Read	Write, Read		Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERR_EN	6	Enables reporting of (CC_CRC_ERR_CNT > 0) on the ERRB pin	0b0: Disable reporting of errors on ERRB 0b1: Enable reporting of errors on ERRB
LINE_CRC_LOC	5:4	Video line CRC insertion location	0b00: [1..4] 0x01: [5..8] 0x10: [9..12] 0x11: [13..16]
LINE_CRC_EN_GMSL1	3	Video line CRC enable	0b0: Disable video line CRC 0x1: Enable video line CRC
MAX_RT_ERR_EN	1	Enables reflection of maximum retransmission error on the ERRORB pin	0b0: Disable maximum retransmission error on the ERROR pin 0b1: Enable maximum retransmission error on the ERROR pin
RCEG_ERR_PER_EN	0	Periodic error generation enable. Effective when RCEG_TYPE = 0x.	0b0: Disable periodic error generator 0b1: Enable periodic error generator

GMSL1_13 (0xC13)

BIT	7	6	5	4	3	2	1	0
Field	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
Reset	0b1	0b1	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EN_G1	7	Enables eye-opening monitor (EOM)	0b0: Disable EOM 0x1: Enable EOM
EOM_PER_MODE_G1	6	Eye-opening monitor (EOM) periodic mode select	0b0: Set EOM to use non-periodic mode 0x1: Set EOM to use periodic mode
EOM_MAN_TRG_REQ_G1	5	Eye-opening monitor (EOM) manual trigger request. Valid on the rising edge of this bit when not in periodic mode.	0x0: Do not trigger EOM. 0x1: Manually trigger the EOM
EOM_MIN_THR_G1	4:0	Eye-opening minimum threshold (in terms of percent) for flagging ERRORB pin. (Percentages increment 3.125% per bitfield setting.)	0b00000: Disabled 0b00001: 3.125% 0b00010: 6.25% 0b00011: 9.375 . . 0b11111: 100%

GMSL1_14 (0xC14)

BIT	7	6	5	4	3	2	1	0
Field	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
Reset	0b1	0b0	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_EN	7	Adaptive equalization enable	0b0: Disable AEQ 0x1: Enable AEQ
AEQ_PER_MODE	6	Adaptive equalizer periodic mode select	0b0: Set AEQ to use nonperiodic mode 0x1: Set AEQ to use periodic mode
AEQ_MAN_TRG_REQ	5	Adaptive equalizer manual fine tune request enable. Valid on the rising edge of this bit when not in periodic mode.	0x0: Do not trigger AEQ fine tuning 0x1: Manually trigger the AEQ fine tuning
EOM_PER_THR	4:0	Eye-opening threshold to trigger a fine tune operation	0b00000: Eye-opening threshold is disabled 0b10000: 50% eye opening triggers fine-tune operation OTHER: Reserved

GMSL1_15 (0xC15)

BIT	7	6	5	4	3	2	1	0
Field	DET_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_ERR	7:0	Detected error counter	0xXX: Number of detected errors

GMSL1_16 (0xC16)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_ERR	7:0	PRBS error counter	0xXX: Number of detected PRBS errors

GMSL1_17 (0xC17)

BIT	7	6	5	4	3	2	1	0
Field	I2C_TIMED_OUT_GMSL1	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
Reset	0b0	0b0	0b0	0b0	0b0	–	–	–
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMED_OUT_GMSL1	7	I^2C channel timed out flag	0b0: I^2C channel not timed out 0b1: I^2C channel timed out
MAX_RT_ERR_I2C	6	Maximum retransmission error flag. Cleared when read.	0b0: No control channel retransmission error 0b1: Control channel retransmission maximum limit reached
PRBS_OK	5	MAX9271/73 compatible PRBS test to determine if link completed normally. Check PRBS_ERR register for PRBS success. For other SERDES read PRBS_ERR registers.	0b0: No MAX9271/MAX9273-compatible PRBS test completed 0b1: MAX9271/MAX9273-compatible PRBS test completed normally
GPI_IN	4	GPI pin level	0b0: GPI is input low 0b1: GPI is input high
MAX_RT_ERR_GPI	3	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

GMSL1_18 (0xC18)

BIT	7	6	5	4	3	2	1	0
Field	CC_RETR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_RETR_CNT	7:0	I^2C packet retransmit count	0xXX: Number of I^2C packets retransmitted

GMSL1_19 (0xC19)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-based control-channel CRC error counter	0xXX: Number of control-channel CRC errors

GMSL1_1A (0xC1A)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_CNT	7:0	Control channel number of generated errors	0xXX: Number of control channel generated errors

GMSL1_1B (0xC1B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LINE_CRC_ERR	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ERR	2	CRC error bit. Latched on error - cleared to 0 when read.	0b0: Video line CRC ok 0b1: Video line CRC mismatch detected

GMSL1_1C (0xC1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	EOM_EYE_WIDTH[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EYE_WIDTH	5:0	Measured eye-opening. Opening width = EOM_EYE_WIDTH/63 x 100%	0b000000: Width is 0% 0b000001: Width is 1/63 x 100% 0b000010: Width is 2/63 x 100% . . 0b11111: Width is 63/63 x 100%

GMSL1_1D (0xC1D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
Reset	–	–	–	0b0	0x0			
Access Type	–	–	–	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBOOST_DET	4	Under boost detected	0b0: Normal Operation 0x1: Underboost (at maximum AEQ gain) detected

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_BST	3:0	Adaptive equalizer boost value. Selected adaptive equalizer value; settings correspond to gain at 1.5GHz	0b0000: 0 dB manual EQ setting 0b0001: 0 dB manual EQ setting 0b0010: 1.0 dB manual EQ setting 0b0011: 2.6 dB manual EQ setting 0b0100: 4.0 dB manual EQ setting 0b0101: 5.8 dB manual EQ setting 0b0110: 7.2 dB manual EQ setting 0b0111: 8.6 dB manual EQ setting 0b1000: 10.4 dB manual EQ setting 0b1001: 11.7 dB manual EQ setting 0b1010: 13.5 dB manual EQ setting 0b1011: 14.5 dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_20 (0xC20)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_0	7:0	Bits [7:0] of CRC output for the latest line	0xXX: CRC[7:0] of latest line

GMSL1_21 (0xC21)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_1	7:0	Bits [15:8] of CRC output for the latest line	0xXX: CRC[15:8] of latest line

GMSL1_22 (0xC22)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_2	7:0	Bits [23:16] of CRC output for the latest line	0xXX: CRC[23:16] of latest line

GMSL1_23 (0xC23)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_3	7:0	Bits [31:24] of CRC output for the latest line	0xXX: CRC[31:24] of latest line

GMSL1_96 (0xC96)

BIT	7	6	5	4	3	2	1	0
Field	CONV_GMSL1_DATATYPE[4:0]					DIS_HIBW_E	CONV_GMSL1_EN	DBL_ALIGN_TO
Reset	0b00000					0b0	0b0	0b1
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONV_GMSL1_DATATYPE	7:3	Convert from GMSL1 color format mapping to GMSL2 CSI transmitter color format	0x0: RGB888 OLDI 0x1: RGB565 0x2: RGB666 0x3: YUV 422 8-bit Mux mode (use yuv_8_10_mux_mode) 0x4: YUV 422 10-bit Mux mode (use yuv_8_10_mux_mode) 0x5: RAW8 single 0x6: RAW10 single 0x7: RAW12 single 0x8: RAW14 0x9: User-defined Generic 24-bit 0xA: User-defined YUV422 12-bit 0xB: User-defined Generic 8-bit 0xC 0xD 0xE 0xF 0x10: RGB888 VESA 0x11 0x12 0x13: YUV 422 8-bit Normal mode 0x14: YUV 422 10-bit Normal mode 0x15: RAW8 double (use alt_mem_map8) 0x16: RAW10 double (use alt_mem_map10) 0x17: RAW12 double (use alt_mem_map12) 0x18 0x19 0x1A 0x1B 0x1C 0x1D 0x1E

BITFIELD	BITS	DESCRIPTION	DECODE
			0x1F
DIS_HIBW_E	2	Disable disparity error detection in HIBW	0b0: Enable disparity error detection 0b1: Disable disparity error detection
CONV_GMSL1_EN	1	Enable conversion from GMSL1 color format mapping to GMSL2 CSI transmitter	0b0: Disable conversion 0b1: Enable conversion
DBL_ALIGN_TO	0	HBM DBL mode type	0b0: DBL-Single mode with alignment 0b1: DBL-DBL mode with no alignment (d)

GMSL1_CA (0xCCA)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	PHASELOCK	WBLOCK_G1	DATAOK
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PHASELOCK	2	CDR locked	0b0: CDR not locked 0b1: CDR locked
WBLOCK_G1	1	Word boundary detected	0b0: No word boundary detected 0b1: Word boundary detected
DATAOK	0	Data activity detected on the link	0b0: No data activity detected on the link 0b1: Data activity detected on the link

GMSL1_D1 (0xCD1)

BIT	7	6	5	4	3	2	1	0
Field	CNTL_OUT_ORD[2:0]			CNTL_OUT_EN[4:0]				
Reset	0x0			0x00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CNTL_OUT_ORD	7:5	Internal CNTL_OUT order to pins CNTL4 to CNTL0	0x0: 4, 3, 2, 1, 0 0x1: 3, 2, 1, 0, 4 0x2: 2, 1, 0, 4, 3 0x3: 1, 0, 4, 3, 2 0x4: 0, 1, 2, 3, 4 0x5: 1, 2, 3, 4, 0 0x6: 2, 3, 4, 0, 1 0x7: 3, 4, 0, 1, 2
CNTL_OUT_EN	4:0	CNTL output enable for CNTL 0, 1, 2, 3, 4	0bXXXX0: Disable control output 0 0bXXXX1: Enable control output 0 0bXXX0X: Disable control output 1 0bXXX1X: Enable control output 1 0bXX0XX: Disable control output 2 0bXX1XX: Enable control output 2 0bX0XXX: Disable control output 3 0bX1XXX: Enable control output 3 0b0XXXX: Disable control output 4

BITFIELD	BITS	DESCRIPTION	DECODE
			0b1XXXX: Enable control output 4

GMSL1_EN (0xF00)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	LINK_EN_B	LINK_EN_A
Reset	–	–	–	–	–	–	0x1	0x1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_EN_B	1	Enables link B	0b0: Disable Link B 0b1: Enable Link B
LINK_EN_A	0	Enables link A	0b0: Disable Link A 0b1: Enable Link A

GMSL1_UART (0xF01)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	GMSL1_UART_ARB_TO	GMSL1_UART_ARB_EN
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL1_UART_ARB_TO	1	GMSL1 UART arbitration timeout value	0b0: 256µs 0b1: 4ms
GMSL1_UART_ARB_EN	0	UART arbitration enable on GMSL1 forward control channel links.	0b0: Disable 0b1: Enable

COMMON1 (0xF02)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	REM_ACK_ACKED_G1_B	REM_ACK_ACKED_G1_A
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ACK_ACKED_G1_B	1	Remote ACK acknowledged	0b0: Remote ACK not acknowledged 0b1: Remote ACK acknowledged
REM_ACK_ACKED_G1_A	0	Remote ACK acknowledged	0b0: Remote ACK not acknowledged 0b1: Remote ACK acknowledged

GMSL1_ERR_OEN (0xF03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	G1_B_ERR_OEN	G1_A_ERR_OEN
Reset	–	–	–	–	–	–	0b1	0b1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
G1_B_ERR_OEN	1	Enable reporting of GMSL1 Link B errors (G1_B_ERR_FLAG) at ERRB pin	0b0: Disable reporting 0b1: Enable reporting
G1_A_ERR_OEN	0	Enable reporting of GMSL1 Link A errors (G1_A_ERR_FLAG) at ERRB pin	0b0: Disable reporting 0b1: Enable reporting

GMSL1_ERR_FLAG (0xF04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	G1_B_ERR_FLAG	G1_A_ERR_FLAG
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
G1_B_ERR_FLAG	1	GMSL1 Link B error flag. When PRBS test is enabled, this flag asserted if at least one PRBS error has been detected. When PRBS test is not enabled, the flag is asserted when any of these conditions is true: 1) Number of detected decoding errors is greater than the detected error thrshold (DET_ERR > DET_THR) 2) Measured eye-opening is less than or equal to eye-opening threhold (EOM_EYE_WIDTH ≤ EOM_MIN_THR_G1) 3) Adaptive EQ has detected an under boost 4) Video Line CRC error is detected 5) Maximum retransmission count exceeded in PKTCC communication 6) CRC errors detected in PKTCC communication	0b0: Error flag not asserted 0b1: Error flag asserted
G1_A_ERR_FLAG	0	GMSL1 Link A error flag. When PRBS test is enabled, this flag is asserted if at least one PRBS error has been detected. When PRBS test is not enabled, the flag is asserted when any of these conditions is true: 1) Number of detected decoding errors is greater than the detected error thrshold (DET_ERR > DET_THR) 2) Measured eye-opening is less than or equal to eye-opening threhold (EOM_EYE_WIDTH ≤ EOM_MIN_THR_G1) 3) Adaptive EQ has detected under boost 4) Video Line CRC error is detected	0b0: Error flag not asserted 0b1: Error flag asserted

BITFIELD	BITS	DESCRIPTION	DECODE
		5) Maximum retransmission count exceeded in PKTCC communication 6) CRC errors detected in PKTCC communication	

I2C_0 (0xF05)

BIT	7	6	5	4	3	2	1	0
Field	–	–	G1_SLV_SH[1:0]		–	G1_SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
G1_SLV_SH	5:4	GMSL1 I2C-to-I2C slave setup and hold time setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I2C slave. Set this according to the I2C speed mode. Please see register groups CC_G2P* for GMSL2 registers.	0b00: Set for I2C Fast-mode Plus speed 0b01: Set for I2C Fast-mode speed 0b10: Set for I2C standard-mode speed 0b11: Reserved
G1_SLV_TO	2:0	GMSL1 I2C-to-I2C slave timeout setting Internal GMSL1 I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. Please see register groups CC_G2P* for GMSL2 registers. (Addr. 0x500 - 0x6B0)	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0xF06)

BIT	7	6	5	4	3	2	1	0
Field	EN_I2C_LOOPBACK	G1_MST_BT[2:0]			–	G1_MST_TO[2:0]		
Reset	0x0	0b101			–	0b110		
Access Type	Write, Read	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
EN_I2C_LOOPBACK	7	Enable I2C loopback between links in G1 + G2 or G1 + G1 aggregation mode. When I2C loopback is enabled, the I2C transactions generated at the leaf-end of on one link are reflected to the leaf-end of the other link	0x0: Disable loopback 0x1: Enable loopback
G1_MST_BT	6:4	GMSL1 I2C-to-I2C master bit rate setting, configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master) Set this according to the I2C speed mode. See register groups CC_G2P* for GMSL2	0b000: 9.92Kbps - Set for I2C Standard mode speed 0b001: 33.2Kbps - Set for I2C Standard mode speed 0b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 0b011: 123Kbps - Set for I2C Fast-mode speed

BITFIELD	BITS	DESCRIPTION	DECODE
		registers.	0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
G1_MST_TO	2:0	GMSL1 I²C-to-I²C master timeout setting Internal GMSL1 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. See register groups CC_G2P* for GMSL2 registers. (Addr. 0x500 - 0x6B0)	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0xF07)

BIT	7	6	5	4	3	2	1	0
Field	G1_SRC_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
G1_SRC_A	7:1	GMSL1 I²C address translator source A When I²C device address matches I²C SRC_A, internal I²C master (on remote side) replaces the device address by I²C DST_A. See register groups CC_G2P* for GMSL2 registers.	0bXXXXXXX: Value of I²C SRC_A

I2C_3 (0xF08)

BIT	7	6	5	4	3	2	1	0
Field	G1_DST_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
G1_DST_A	7:1	GMSL1 I²C address translator destination A See the description of I²C SRC_A. See register groups CC_G2P* for GMSL2 registers.	0bXXXXXXX: Value of I²C DST_A

I2C_4 (0xF09)

BIT	7	6	5	4	3	2	1	0
Field	G1_SRC_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
G1_SRC_B	7:1	GMSL1 I²C address translator source B When I²C device address matches I²C SRC_B, internal I²C master (on remote side) replaces the device address by I²C DST_B. See register groups CC_G2P* for GMSL2 registers.	0bXXXXXXX: Value of I²C SRC_B

I2C_5 (0xF0A)

BIT	7	6	5	4	3	2	1	0
Field	G1_DST_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
G1_DST_B	7:1	GMSL1 I²C address translator destination B See the description of I²C SRC_B. See register groups CC_G2P* for GMSL2 registers.	0bXXXXXXX: Value of I²C DST_B

SPI_CC_WR_ (0x1300)

Internal write location for SPI to Control Channel bytes

SPI_CC_RD_ (0x1380)

Internal read location for SPI to Control Channel bytes

RLMS3 (0x1403, 0x1503)

BIT	7	6	5	4	3	2	1	0
Field	AdaptEn	–	–	–	–	–	–	–
Reset	0x0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
AdaptEn	7	Adapt process enable	0b0: Manual adaptation process disabled 0b1: Manual adaptation process enabled

RLMS4 (0x1404, 0x1504)

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0x2		0x1	0x1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye monitor window. N is used in the equation: Observations = 6.29 x $10^{(N + 2)}$	0xX: N factor
EOM_CHK_THR	3:2	Eye-opening monitor number of error bits to allow in a measurement window	0b00: Allow no errors 0b01: Allow 1 error 0b10: Allow 2 errors 0b11: Allow 3 errors
EOM_PER_MODE	1	Eye-opening monitor periodic mode enable	0b0: Eye-opening monitor periodic mode disabled 0b1: Eye-opening monitor periodic mode enabled
EOM_EN	0	Eye-opening monitor enable	0b0: Eye-opening monitor disabled 0b1: Eye-opening monitor enabled

RLMS5 (0x1405, 0x1505)

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0x0	0x10						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye-opening monitor manual trigger. For use when periodic mode is disabled.	0b0: No action 0b1: Eye-opening monitor manual trigger request
EOM_MIN_THR	6:0	The eye-opening monitor minimum threshold as defined by the equation: % eye-opening = EOM_MIN_THR/64. If the value is zero the EOM is disabled.	0bXXXXXXX: Eye-opening monitor minimum threshold factor

RLMS6 (0x1406, 0x1506)

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	EOM_RST_THR[6:0]						
Reset	0x1	0x00						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Eye-opening is measured vertically or horizontally	0b0: Vertical opening mode 0b1: Horizonal opening mode

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_RST_THR	6:0	The eye-opening monitor refresh threshold as defined by the equation: % eye opening = EOM_MIN_THR/64. If the value is zero the eye-opening monitor is disabled.	0bXXXXXXX: Eye-opening monitor refresh threshold factor

RLMS7 (0x1407, 0x1507)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0x0	0x00						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye-opening monitor measurement done	0b0: Eye-opening monitor not complete 0b1: Eye-opening monitor complete
EOM	6:0	Last completed eye-opening monitor observation	0bXXXXXXX: Eye-monitor opening measurement result

RLMS34 (0x1434, 0x1534)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntL	7:0	Eye monitor period count (RxClk20) LSB	0xXX: Eye monitor period count (Least Significant Byte)

RLMS35 (0x1435, 0x1535)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonPerCntH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonPerCntH	7:0	Eye monitor period count (RxClk20) MSB	0xXX: Eye monitor period count (Most Significant Byte)

RLMS37 (0x1437, 0x1537)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	EyeMonDone	EyeMonCntClr	EyeMonStart	EyeMonPh	EyeMonDPol
Reset	–	–	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	–	Read Only	Write Only	Write Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonDone	4	Eye monitor period complete (read-only, reset on start)	0b0: Eye monitor data collection not complete 0b1: Eye monitor data collection complete
EyeMonCntClr	3	Eye monitor error/valid count clear (one-shot). Read-back is EyeMonClrPL from long pulse generation.	0b0: NA 0b1: Clear eye monitor data collection counters
EyeMonStart	2	Eye monitor start (one-shot). Read-back is EyeMonStClrPL from long pulse generation for both start and clear.	0b0: NA 0b1: Start eye monitor data collection
EyeMonPh	1	Eye monitor phase	0b0: Eye monitor search early phase 0b1: Eye monitor search late phase
EyeMonDPol	0	Eye monitor data polarity	0b0: Eye monitor search for 1's 0b1: Eye mnitor search for 0's

RLMS39 (0x1439, 0x1539)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonErrCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonErrCntH	7:0	Eye monitor error count (read-only)	0xXX: Eye monitor error count (Most Significant Byte)

RLMS3A (0x143A, 0x153A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntL	7:0	Eye monitor valid (hit) count (read-only)	0xXX: Eye monitor valid count (Least Significant Byte)

RLMS3B (0x143B, 0x153B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EyeMonValCntH	7:0	Eye monitor valid (hit) count (read-only)	0xXX: Eye monitor valid count (Most Significant Byte)

RLMS3D (0x143D, 0x153D)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPh[6:0]							ErrChPhTogEn
Reset	0x00							0x1
Access Type	Read Only							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPh	7:1	Error channel phase (read-only)	0bXXXXXXX: 5.6 degrees per step
ErrChPhTogEn	0	Error channel phase toggle enable	0b0: Use primary phase only 0b1: Auto toggle phase between primary and secondary

RLMS3E (0x143E, 0x153E)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTA	ErrChPhSec[6:0]						
Reset	0x1	0x33						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTA	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSec	6:0	Error channel phase secondary (odd)	0bxxxxxxx: Error channel phase secondary (odd)

RLMS3F (0x143F, 0x153F)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTA	ErrChPhPri[6:0]						
Reset	0x0	0x72						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriT	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled

BITFIELD	BITS	DESCRIPTION	DECODE
A			0b1: Timing adjust enabled
ErrChPhPri	6:0	Error channel phase primary (even)	0bxxxxxxx: Error channel phase primary (even)

RLMS58 (0x1458, 0x1558)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh1[6:0]						
Reset	–	0x18						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh1	6:0	Error channel target amplitude for ones	0bxxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS59 (0x1459, 0x1559)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh0[6:0]						
Reset	–	0x58						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChVTh0	6:0	Error channel target amplitude for zeros	0bxxxxxx: Format: {sign, Magnitude[5:0]} where sign: 1 = negative, 0 = positive Magnitude:: binary amplitude 4.7mV per count

RLMS5B (0x145B, 0x155B)

BIT	7	6	5	4	3	2	1	0
Field	–	ErrChVTh[6:0]						
Reset	–	0x00						
Access Type	–	Read Only						

BITFIELD	BITS	DESCRIPTION
ErrChVTh	6:0	Error channel threshold (read-only)

RLMS64 (0x1464, 0x1564)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCMode[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx spread spectrum mode	0b00: No spread spectrum (manual phase) 0b01: Center spread 0b10: Reserved 0b11: Reserved

RLMS70 (0x1470, 0x1570)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0x01						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx spread spectrum frequency control	0bXXXXXXX: Tx spread spectrum center frequency control

RLMS71 (0x1471, 0x1571)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0x01						0x0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx spread spectrum center spread startup control	0bXXXXXX: Tx spread spectrum center spread startup control
TxSSCEn	0	Tx spread spectrum enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472, 0x1572)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx spread spectrum frequency pre-scaler low byte	0xXX: Tx spread spectrum frequency pre-scaler low byte

RLMS73 (0x1473, 0x1573)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreScIH	2:0	Tx spread spectrum frequency pre-scaler high bits	0bXXX: Tx spread spectrum frequency pre-scaler high bits

RLMS74 (0x1474, 0x1574)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx spread spectrum interpolator phase low byte	0xXX: Tx spread spectrum frequency interpolator phase low byte

RLMS75 (0x1475, 0x1575)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0x00						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx spread spectrum interpolator phase	0bXXXXXXX: Tx spread spectrum frequency interpolator phase high bits

RLMS76 (0x1476, 0x1576)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx spread spectrum interpolator phase quadrant	0bXX: Tx spread spectrum interpolator phase quadrant

RLMS95 (0x1495, 0x1595)

BIT	7	6	5	4	3	2	1	0
Field	TxAmplManEn	–	TxAmplMan[5:0]					
Reset	0x0	–	0x29					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplManEn	7	Tx amplitude manual override	0b0: Do not manually override Tx amplitude 0b1: Manually override Tx amplitude

BITFIELD	BITS	DESCRIPTION	DECODE
TxAmplMan	5:0	Tx amplitude	0bXXXXXX: Binary amplitude 10mV per count

RLMSA4 (0x14A4, 0x15A4)

BIT	7	6	5	4	3	2	1	0
Field	AEQ_PER_MULT[1:0]		AEQ_PER[5:0]					
Reset	0x2		0x3D					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_PER_MULT	7:6	Adaptive EQ period multiplier	0b00: 1ms 0b01: 4ms 0b10: 16ms 0b11: 64ms
AEQ_PER	5:0	Adaptive EQ period. Periodic adaptation is disabled when value is 0. Adaptive EQ period is (AEQ_PER value times AEQ_PER_MULT).	0bXXXXXX: Only zeros have a special meaning. See Description

RLMSAC (0x14AC, 0x15AC)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR3G	ErrChPhSecFR3G[6:0]						
Reset	0x1	0x4D						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR3G	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR3G	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Secondary Phase, 3Gbps)	0bXXXXXXX: 7'h4D

RLMSAD (0x14AD, 0x15AD)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR3G	ErrChPhPriFR3G[6:0]						
Reset	0x0	0x0D						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR3G	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriF	6:0	A 7-bit phase command used for eye	0bXXXXXXX: 7'h0D

BITFIELD	BITS	DESCRIPTION	DECODE
R3G		monitoring and used during adaptation by the error channel. (Fast Receive, Primary Phase, 3Gbps)	

RLMSAE (0x14AE, 0x15AE)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTAFR1G5	ErrChPhSecFR1G5[6:0]						
Reset	0x1	0x4E						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTAFR1G5	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecFR1G5	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Secondary Phase, 3.5Gbps)	0bXXXXXXX: 7'h4E

RLMSAF (0x14AF, 0x15AF)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTAFR1G5	ErrChPhPriFR1G5[6:0]						
Reset	0x0	0x0F						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTAFR1G5	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriFR1G5	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Fast Receive, Primary Phase, 3.5Gbps)	0bXXXXXXX: 7'h0F

RLMSB0 (0x14B0, 0x15B0)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASR1G5	ErrChPhSecSR1G5[6:0]						
Reset	0x1	0x34						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASR1G5	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSec	6:0	A 7-bit phase command used for eye	0bxXXXXXX: 7'h34

BITFIELD	BITS	DESCRIPTION	DECODE
SR1G5		monitoring and used during adaptation by the error channel. (Slow Receive, Secondary Phase, 3.5Gbps)	

RLMSB1 (0x14B1, 0x15B1)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASR1G5	ErrChPhPriSR1G5[6:0]						
Reset	0x0	0x73						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASR1G5	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSR1G5	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Primary Phase, 3.5Gbps)	0bXXXXXXX: 7'h73

RLMSB2 (0x14B2, 0x15B2)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG75	ErrChPhSecSRG75[6:0]						
Reset	0x1	0x3E						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG75	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG75	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Secondary Phase, 750Mbps)	0bXXXXXXX: 7'h3E

RLMSB3 (0x14B3, 0x15B3)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG75	ErrChPhPriSRG75[6:0]						
Reset	0x0	0x7D						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG75	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriS	6:0	A 7-bit phase command used for eye	0bXXXXXXX: 7'h7D

BITFIELD	BITS	DESCRIPTION	DECODE
RG75		monitoring and used during adaptation by the error channel. (Slow Receive, Primary Phase, 750Mbps)	

RLMSB4 (0x14B4, 0x15B4)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG375	ErrChPhSecSRG375[6:0]						
Reset	0x1	0x3C						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG375	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhSecSRG375	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Secondary Phase, 375Mbps)	0bXXXXXXX: 7'h3C

RLMSB5 (0x14B5, 0x15B5)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG375	ErrChPhPriSRG375[6:0]						
Reset	0x0	0x7B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG375	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG375	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Primary Phase, 375Mbps)	0bXXXXXXX: 7'h7B

RLMSB6 (0x14B6, 0x15B6)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhSecTASRG1875	ErrChPhSecSRG1875[6:0]						
Reset	0x1	0x3B						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecTASRG1875	7	Error channel phase secondary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhSecSRG1875	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Secondary Phase, 187.5Mbps)	0bXXXXXXX: 7'h3B

RLMSB7 (0x14B7, 0x15B7)

BIT	7	6	5	4	3	2	1	0
Field	ErrChPhPriTASRG1875	ErrChPhPriSRG1875[6:0]						
Reset	0x0	0x7A						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
ErrChPhPriTASRG1875	7	Error channel phase primary timing adjust	0b0: Timing adjust disabled 0b1: Timing adjust enabled
ErrChPhPriSRG1875	6:0	A 7-bit phase command used for eye monitoring and used during adaptation by the error channel. (Slow Receive, Primary Phase, 187.5Mbps)	0bXXXXXXX: 7'h7A

RLMSC4 (0x14C4, 0x15C4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RevFast	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RevFast	2	GMSL1 reverse channel fast mode	0x0: Reverse channel fast mode disabled 0x1: Reverse channel fast mode enabled

DPLL_3 (0x1D03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	config_spread_bit_ratio[2:0]		
Reset	–	–	–	–	–	0x2		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
config_spread_bit_ratio	2:0	controls the magnitude of the triangle wave intput to the divider dsm as a percentage of the nominal divider value. If config registers are reset, the spread_bit_ratio value will not propagate to the triangle wave without rewriting to it. Likewise, if triangle wave module is reset, the user will need to rewrite to spread_bit_ratio to set it back to desired	000: off 001: 0.25% 010: 0.5% 011: 1% 100: 2% 101: 4% 110: 4%

BITFIELD	BITS	DESCRIPTION	DECODE
		value.	111: 4%

DPLL_3 (0x1E03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	config_spread_bit_ratio[2:0]		
Reset	–	–	–	–	–	0x2		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
config_spread_bit_ratio	2:0	controls the magnitude of the triangle wave intput to the divider dsm as a percentage of the nominal divider value. If config registers are reset, the spread_bit_ratio value will not propagate to the triangle wave without rewriting to it. Likewise, if triangle wave module is reset, the user will need to rewrite to spread_bit_ratio to set it back to desired value.	000: off 001: 0.25% 010: 0.5% 011: 1% 100: 2% 101: 4% 110: 4% 111: 4%

Ordering Information

Part Number	Temp Range	Pin-Package	Top Marking
MAX9296AGTM/V+	-40°C to +105°C	48 TQFN-EP	MAXIM
MAX9296AGTM/V+T	-40°C to +105°C	48 TQFN-EP (Tape and Reel)	MAXIM
MAX9296AGTM/VY+	-40°C to +105°C	48 TQFN-SW-EP	MAXIM
MAX9296AGTM/VY+T	-40°C to +105°C	48 TQFN-SW-EP (Tape and Reel)	MAXIM

+ Denotes a lead(Pb)-free/RoHS-compliant (test) package.

T Denotes Tape and Reel

/V Denotes an automotive qualified product

Y Denotes wettable flank

EP Denotes Exposed Pad