晶丰明源
Bright Power Semiconductor

BPMS04N003M

40V N-Channel Power MOSFET

General Description

The BPMS04N003M uses super trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

The BPMS04N003M is available in DFN5*6 package.

Application

- Synchronous Rectification for Power Supply
- DC/DC Converters
- High-frequency switching

Features

- BV_{DSS} = 40V, I_D = 110A
- $R_{DS(ON)\_TYP}$ = 2.4mΩ @ V_{GS} = 10V.
  $R_{DS(ON)\_TYP}$ = 3.3mΩ @ V_{GS} = 4.5V
- Fast switching capability.
- Robust design with better EAS performance
- EMI Improved Design
- 100% UIS Tested

Typical Application

V_{DS}	40	V
$R_{DS(ON)\ MAX}$	2.8	mΩ
I_D	110	A

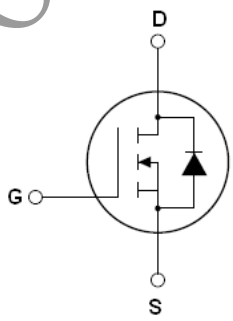
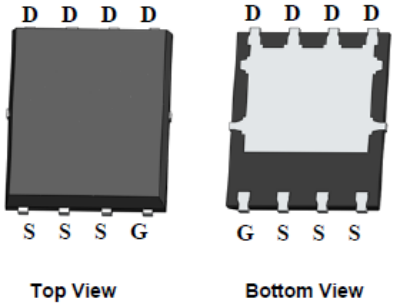


Figure 1. Schematic Diagram

Ordering Information

Part Number	Package	Operating Temperature	Packing Type	Marking
BPMS04N003M	DFN5*6	-55 ℃ to 150 ℃	Tape & Reel 5,000pcs/Reel	BPMS04N003M XXXXXAY H1AMWWY

Pin Configuration and Marking Information



BPMS04N003M
XXXXXAY
H1AMWWY

XXXXX: Lot Code
H: Fab code
AM: MOS code
WW: Week

Figure 2. Pin Configuration and Marking Information

Pin Definition

Pin No.	Name	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

Absolute Maximum Rating (note 1) (Unless otherwise specified, T_A=25℃)

Symbol	Parameters	Range	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0V)	40	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±20	V
$I_{D\,(DC)}$	Continuous Drain Current at Tc=25°C	110(note 2)	A
	Continuous Drain Current at Tc=100°C	77.8	A
$I_{DM\,(pluse)}$	Pulsed drain current (note 3)	340	A
P_D	Maximum Power Dissipation(Tc=25℃)	75	W
EAS	Single pulse avalanche energy (note 4)	500	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
R_{thJC}	Thermal Resistance, Junction-to-Case	1.67	°C /W

Note 1: *Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Under "recommended operating conditions" the device operation is assured, but some particular parameter may not be achieved. The electrical characteristics table defines the operation*

range of the device, the electrical characteristics is assured on DC and AC voltage by the test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, the accuracy is not guaranteed by spec.

Note 2: *Limited by maximum junction temperature.*

Note 3: *Repetitive Rating: Pulse width limited by maximum junction temperature.*

Note 4: *Tj=25℃,V_{DD}=50V,V_G=10V, R_G=25Ω*

Electrical Characteristics (note 5, 6)（Unless otherwise specified, T_A=25℃）

Symbol	Parameter	Condition	Min	Typ	Max	Unit
On/off states						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=40V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V, V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.2	1.7	2.2	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=55A		2.4	2.8	mΩ
		V_{GS}=4.5V, I_D=55A		3.3	3.9	
Dynamic Characteristics						
C_{lss}	Input Capacitance	V_{DS}=20V, V_{GS}=0V, F=1.0MHz		3510		pF
C_{oss}	Output Capacitance			860		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
Q_g	Total Gate Charge	V_{DS}=20V, I_D=55A, V_{GS}=0~10V		60	72	nC
Q_{gs}	Gate-Source Charge			9.9		nC
Q_{gd}	Gate-Drain Charge			9.5		nC
Switching times						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=20V, I_D=55A, R_G=1.6Ω, V_{GS}=10V		10.5		nS
t_r	Turn-on Rise Time			4		nS
$t_{d(off)}$	Turn-Off Delay Time			35		nS
t_f	Turn-Off Fall Time			5		nS
Source- Drain Diode Characteristics						
I_S	Continuous Source current	T_C=25°C			110	A
I_{SM}	Pulsed Source current				340	A
V_{SD}	Forward On Voltage	Tj=25°C, I_{SD}=55A, V_{GS}=0V			1.2	V
t_{rr}	Reverse Recovery Time	V_R=55V,Tj=25°C, I_F=55A, di/dt=100A/μs			24	nS
Q_{rr}	Reverse Recovery Charge				68	nC

Note 5: *Production testing of the chip is performed at 25°C.*

Note 6: *The maximum and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis.*

Typical Electrical and Thermal Characteristics Curves

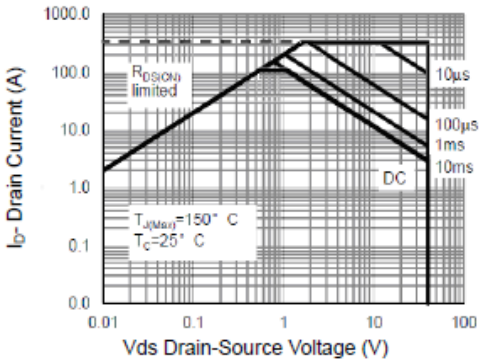


Figure 3. Safe Operating Area

I_D=f(V_{DS});T_C=25℃； V_{GS}＞7V； parameter t_p

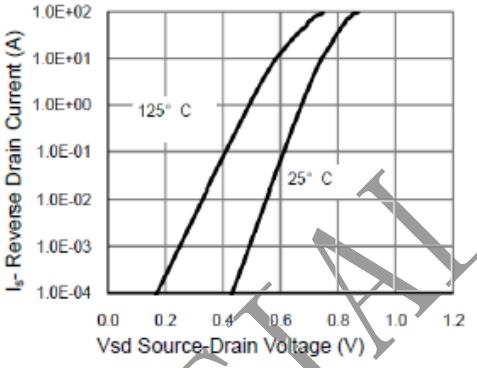


Figure 4. Source-Drain Diode Forward Voltage

I_F=f(V_{SD}); parameter T_j

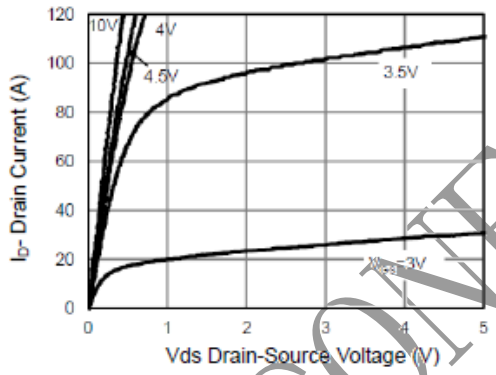


Figure 5. Output Characteristics

I_D=f(V_{DS});T_j=25℃； parameter V_{GS}

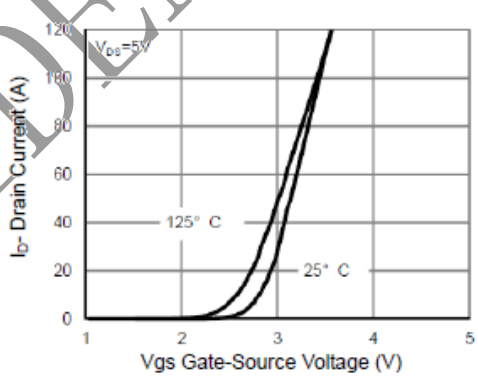


Figure 6. Transfer Characteristics

I_D=f(V_{GS}); V_{DS}=5V

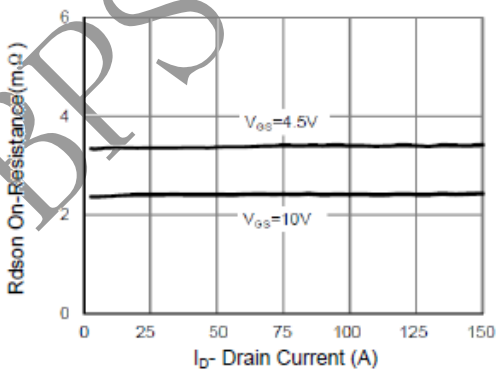


Figure 7. Static Drain-Source ON Resistance

$R_{DS(ON)}$ =f(I_D);T_j=25℃； parameter V_{GS}

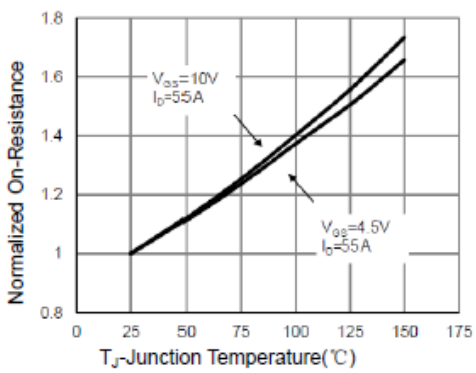


Figure 8. $R_{DS(ON)}$ vs Junction Temperature

$R_{DS(ON)}$ =f(T_j);I_D=55A； V_{GS}=10V

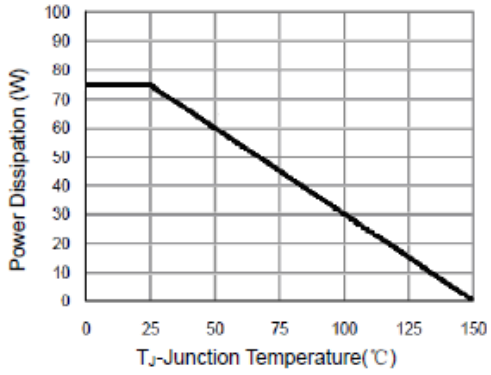


Figure 9. P_D vs Junction Temperature

P_D=f(T_j)

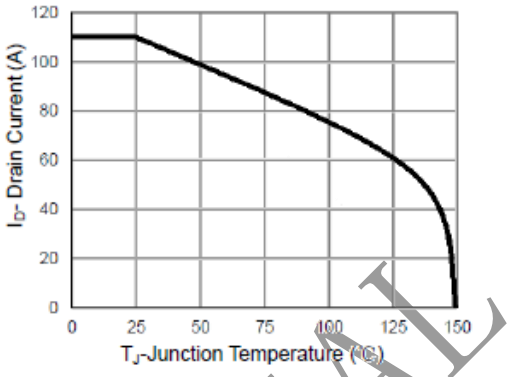


Figure 10. Maximum I_D vs Junction Temperature

I_D=f(T_j); V_{GS}>=10V

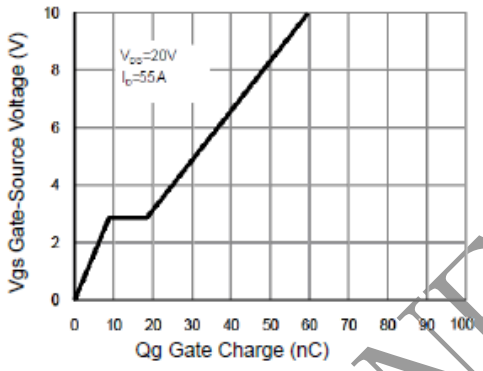


Figure 11. Gate charge waveforms

V_{GS} =f(Q_{gate});I_D=55A pulsed

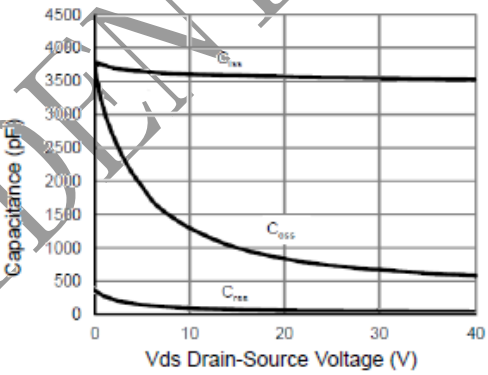


Figure 12. Capacitance

C=f(V_{DS});V_{GS}=0; f=1MHZ

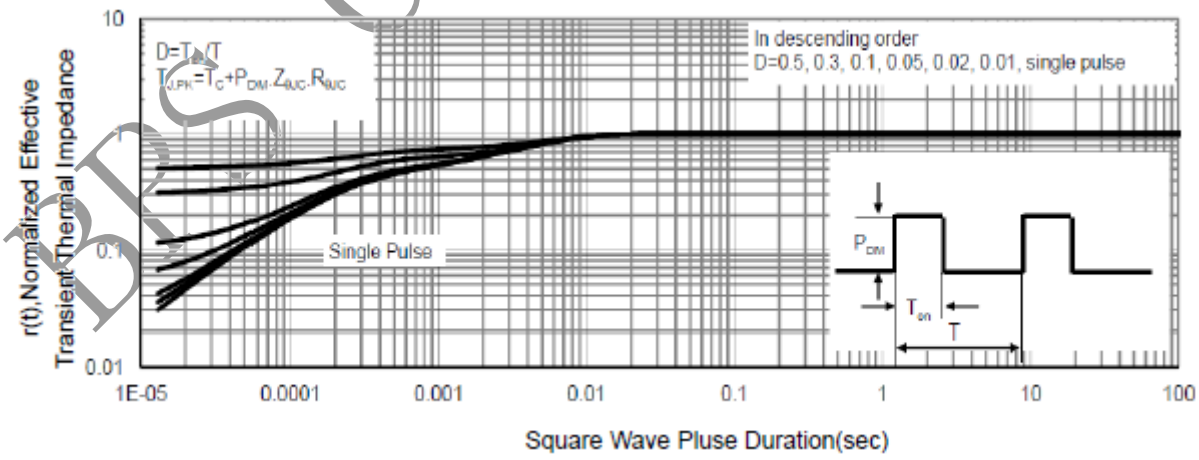
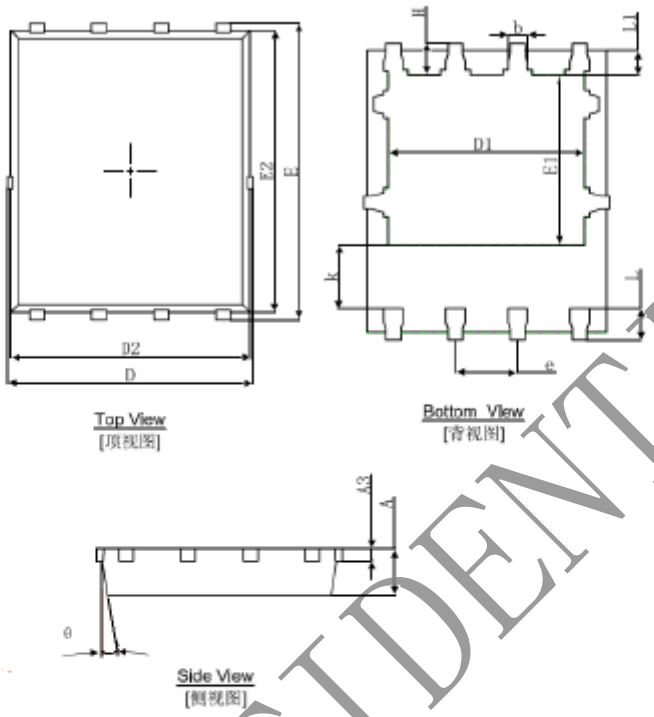


Figure 13. Transient Thermal Impedance

$Z_{(thJC)}$ =f(t_p); parameter: D=t_p/T

Package Information（DFN5*6）

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°