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# SK5129 Product Description

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This datasheet is intended for customer's evaluation and application of the SK5129 device. Under no circumstances it should be circulated outside the customer's company. This datasheet is preliminary and SunTek reserves the right to modify and to improve the data.

## PRODUCT DESCRIPTION

SK5129 is a high-gain, low-noise amplifier (LNA) designed for GPS, Galileo, Glonass and Beidou GNSS applications. Designed in a standard low-cost RF CMOS process, the LNA achieves up to 30dB gain and 1dB noise figure. SK5129 forms the optimal RF front-end for the reception of GNSS satellites. Packaged in a 6-pin μDFN package, the SK5129 sits on a small form factor PCB space. It can operate from a 1.6V to 3.6V single supply and draws only 6.5mA DC current. The shutdown leakage current is only 1uA.

## FEATURES

- Ultra-low-noise figure of 1dB
- High-power gain up to 30dB
- Integrated 50-Ohm output matching circuit
- Low-power of 6.5mA operated from a single 1.6V to 3.6V voltage
- Small footprint of 1.6mmx1.6mm
- Thin profile of 0.55mm
- Lead-free and RoHS-compliant package
- High integration with few off-chip BOM and low cost
- Temperture from –40$^{o}$ to 85$^{o}$ range

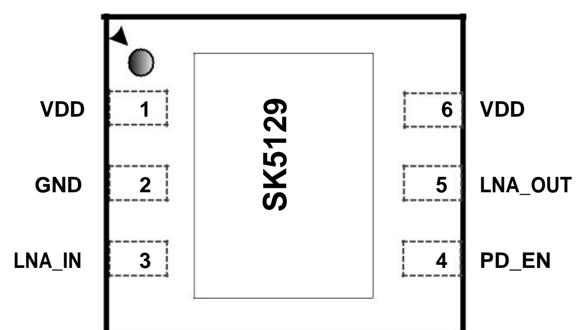
## APPLICATIONS

- PNDs (Personal Navigation Devices)
- Location-Enabled MID
- PMPs (Personal Media Players)
- Automobile Navigation Systems
- GNSS tracking systems
- GNSS industrial applications
- Software GPS
- iPad like Mobile PCs

## TECHNOLOGY

- Device in DFNWB1.6x1.6-6L package, pin compatible with the 6-pin plastic TSOP
- RoHS-compliant package
- Low noise linear regulator for power management
- Silicon CMOS 0.18um process with 1.8/3.3V operation

## PIN ASSIGNMENT

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## PIN CONNECTIONS AND INTERNAL BLOCK DIAGRAM

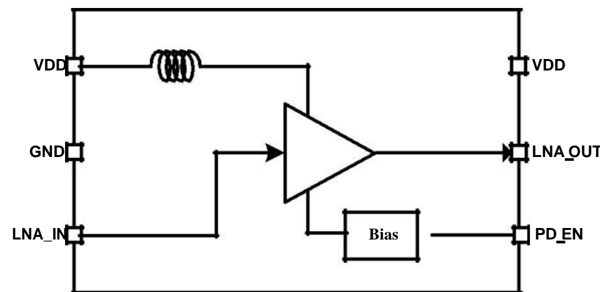


Figure 1 Block Diagram for LNA

## Pin Out Description

| Pin No. | Name | Description | Connection |
|---|---|---|---|
| 1 | VDD | power supply for LNA | Supply Voltage. |
| 2 | GND | Ground connection | Connect to PCB ground plane. |
| 3 | LNA_IN | RF Input | Requires a DC-blocking capacitor and external matching components. |
| 4 | PD_EN | Shutdown Input | A logic-low disables the device. |
| 5 | LNA_OUT | RF Output | Requires a DC-blocking capacitor and external matching components. |
| 6 | VDD | power supply for LNA | Supply Voltage. |
| **Die Pad** | GND | Ground connection | Main IC GND connection |

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## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | VDD | $T_A$=+25℃ | | 4.0 | V |
| Power Down Voltage | $V_{PD_EN}$ | $T_A$=+25℃ | | 4.0 | V |
| LNA Max RF Input Power | $P_{in}$ | | | 0 | dBm |
| ESD: HBM, 150pF/1.5KOhm | - | | 2.5 | | kV |
| Storage Temperature | $T_{STG}$ | | -40 | +150 | °C |
| Solder Reflow Temperature | $T_{SLDR}$ | | | +260 | °C |

This device should be handled with care within the above stress ratings. This IC has ESD protection circuits within but must be handled and assembled accordi g to the industry practice and at the ESD protected work platforms.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | M n. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | -40 | +25 | +85 | 0C |
| Supply Voltage | VDD | 1.6 | 2.7 | 3.6 | V |
| Power Down Turn-on Voltage | $V_{PD\ n}$ | 1.6 | - | VDD | |
| Power Down Turn-off Voltage | $V_{PD\ ff}$ | 0 | - | 0.4 | V |

## ELECTRICAL CHARACTERISTICS

**($T_A$ = +25℃,VDD= $V_{PD\ EN}$ = 2.7V, $f_{in}$ = 1 575.42MHz, unless otherwise specified)**

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| circuit current | $I_{cc}$ | No Signal | 5.0 | 6.5 | 8.0 | mA |
| Power Gain (Note1) | $G_p$ | Pin=-35dBm | 28 | 30 | 32 | dB |
| Noise Figure | NF | | - | 0.85 | 1.2 | dB |
| Input Return Loss | $RL_{in}$ | | - | 10 | - | dB |
| Output Return Loss | $RL_{out}$ | | 12 | 15 | - | dB |

Note1: If low gain is needed modify output inductor value.

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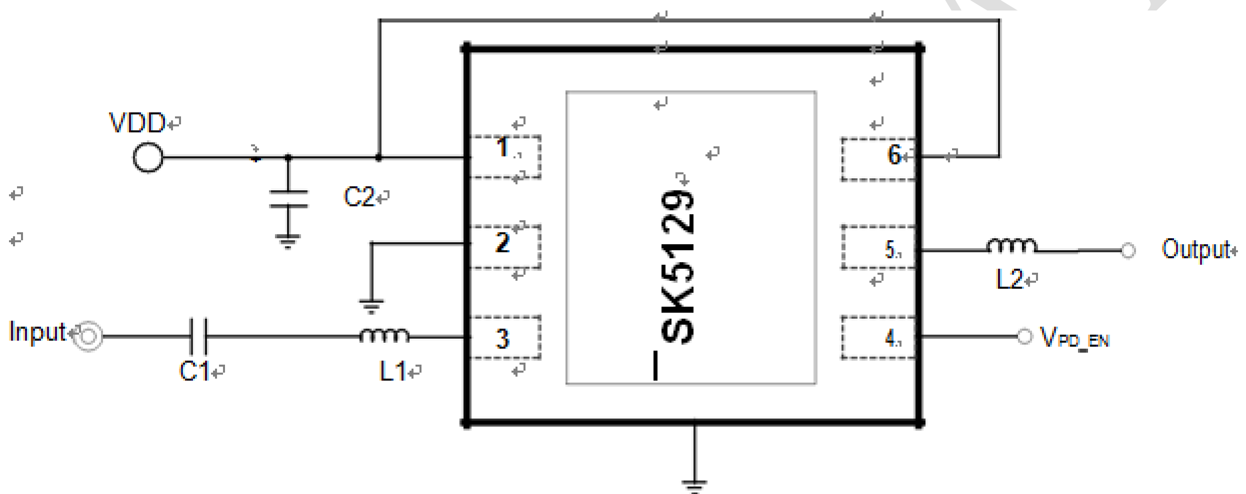
## STANDARD CHARACTERISTICS FOR REFERENCE

**($T_A$ = +25℃, VDD= $V_{PD\ EN}$ = 2.7V, $f_{in}$ = 1 575.42MHz, unless otherwise specified)**

| P r meter | Symbol | Test Conditions | Reference | Unit |
|---|---|---|---|---|
| Isolation | ISL | | 45 | dB |
| Input 3rd Order Distortion Intercept Point | $IIP_3$ | fin1 = 1 575 MHz<br>fin2 = 1 574 MHz | -15 | dBm |
| Gain 1 dB Compression Input Power | $P_{in(1dB)}$ | | -25 | dBm |

## Typical Application Diagram




## BOM LIST

| BOM Descriptions | Symbol | Size | Value | Unit |
|---|---|---|---|---|
| Chip Capacitor | C1 | 0402 | 100 | pF |
| Chip inductor | L1 | 0402 | 8.2 | nH |
| Chip Capacitor | L2 | 0402 | 10 | nH |
| Chip Capacitor | 2 | 0402 | 10 | nF |

These component values are for reference only and are subject to change with customer specific PCB layout design.

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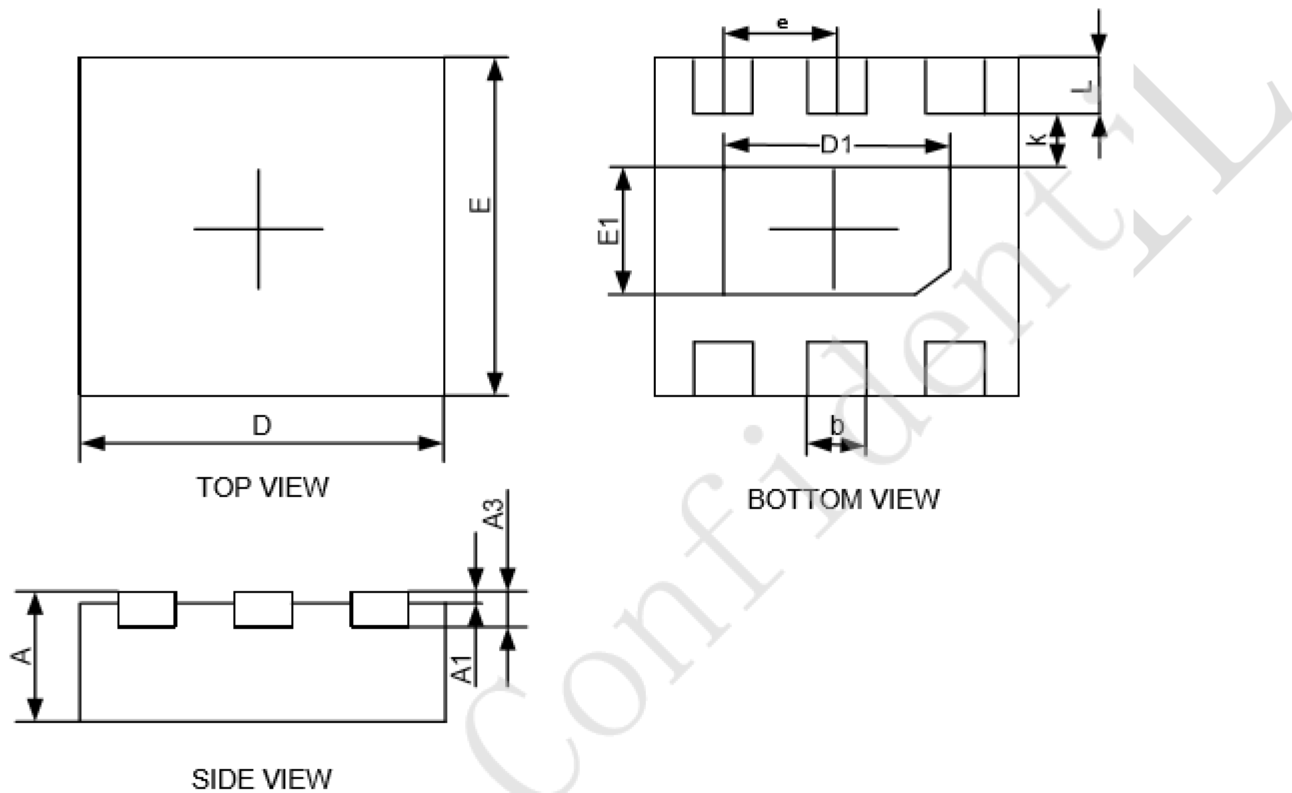
## PACKAGE DIMENSIONS

***Pin compatible with 6-pin plastic TSON**




| symbol | Dim nsions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.450 / 0.550 | 0.550 / 0.650 | 0.018 / 0.022 | 0.022 / 0.026 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.152REF. | | 0.006REF. | |
| D | 1.550 | 1.650 | 0.061 | 0.065 |
| E | 1.550 | 1.650 | 0.061 | 0.065 |
| E1 | 0.550 | 0.650 | 0.022 | 0.026 |
| D1 | 0.950 | 1.050 | 0.037 | 0.041 |
| k | 0.200MIN. | | 0.008REF. | |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| e | 0.500BSC. | | 0.020BSC. | |
| L | 0.164 | 0.316 | 0.006 | 0.012 |

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## RECOMMANDED REFLOW PROFILE

Table2 Reflow Test Condition

| Profile Feature | Pb-Free Assembly |
|---|---|
| **Preheat & Soak**<br>Temperature min (Tsmin)<br>Temperature max (Tsmax)<br>Time (Tsmin to Tsmax)(ts) | <br>150℃<br>200℃<br>60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3℃/second max. |
| Liquidous temperature (TL)<br>Time at liquidous (tL) | 217℃<br>60-150 seconds |
| Peak package body temperature (Tp) * | See classification temp in Table 3 |
| Time (tp)** within 5℃ of the specified<br>clsssification temperature (Tc) | 30**seconds |
| Average ramp-down rate (Tp to Tsmax) | 6℃/second max. |
| Time 25℃ to peak temperature | 8 minutes max. |

Remark: All temperatures refer to the package b dy surface temperature. The highest temperature of reflow profile can not exceed 265℃.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2℃ of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latt r. To accurately measure actual peak package body temperatures refer to JEP140 for recomm nd d thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in T ble2. For example, if Tc is 260℃ and time tp is 30 seconds, this means the following for the supplier and the user. For a supplier: The peak temperature must be at least 260℃ .The time

bove 255℃ must be at least 30 seconds. For a user: The peak temperature must not exceed 260℃. The time above 255℃ must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

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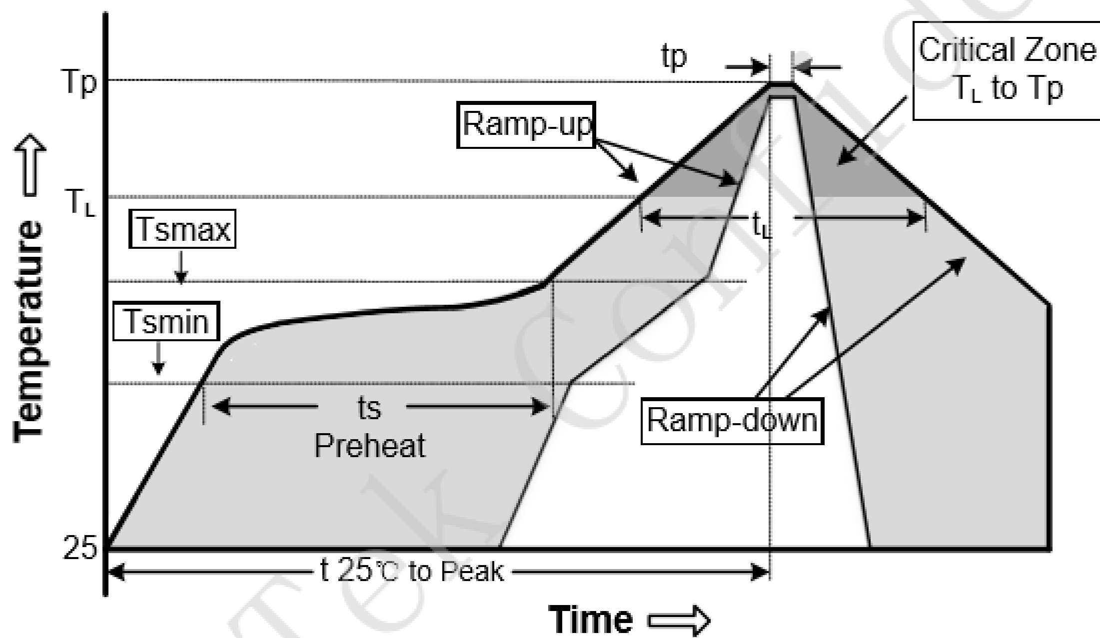
Table 3 Pb-Free Process – Classification Temperatures (Tc)

| Package Thickness | Volume mm3 < 350 | Volume mm3 350 - 2000 | Volume mm3 > 2000 |
|---|---|---|---|
| < 1.6 mm | 260℃ | 260℃ | 260℃ |
| 1.6 mm - 2.5 mm | 260℃ | 250℃ | 245℃ |
| > 2.5 mm | 250℃ | 245℃ | 245℃ |

**Reflow Profile**




The reflow profile shown above should not be exceeded, since excessive temperatures or transport times duri g reflow can damage the chip.

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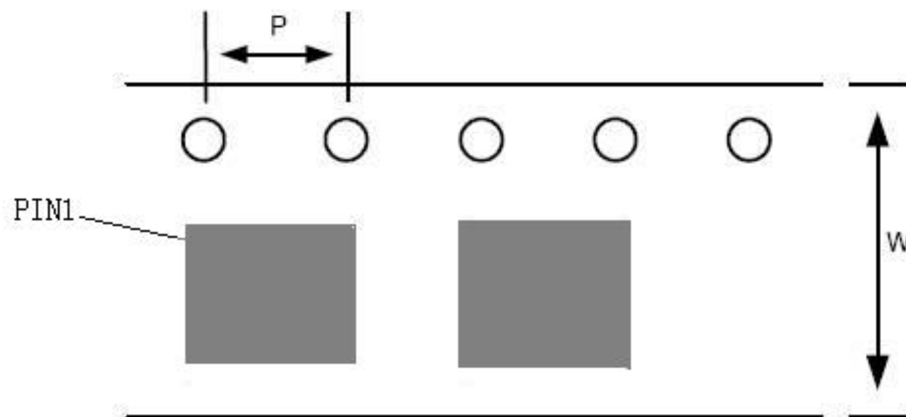
## PACKING SPEC

| PKG | TAPE | REEL | BOX | PCS/REEL | REEL/BOX | PCS/BOX | BOX/CARTON | PCS/CARTON |
|---|---|---|---|---|---|---|---|---|
| DFN1.6x1.6 | IC-ZD-78-1 | 7" IC-JP-05 | TR-1-01 | 3000 | 10 | 30000 | 4 | 120000 |

## ■ Tape & Reel Dimension

P = 4 mm

W = 8 mm

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