Leadtrend

Preliminary Datasheet

LD7839

05/06/2020

High Performance Primary Side LED Controller With dimming function and Thermal Fold back

REV: P03

The values contained in this preliminary datasheet are for reference only and not for approval. Users should verify for a current and complete document before placing orders.

General Description

The LD7839 is a controller with active power factor correction. It supports high power factor across a wide range input of line voltages, and it drives the converter in the Quasi-Resonant (QR) mode to achieve the higher efficiency. By using Primary Side Regulation (PSR), the LD7839 controls the output current accurately without a shunt regulator and an opto-coupler at secondary side, reducing the external component count, the cost, and volume of the driver board. Designed to support flyback or buck boost topologies in voltage mode technical.

The LD7839 is compatible with analog dimming. The output current can be modulated by PWM duty ratio or average level of DIM pin.

The LD7839 housed in the standard SOIC10, The device is highly integrated with a minimum number of external components. A robust suite of safety protections is built in to simplify the design as LED open circuit , LED short circuit , VCC under voltage lockout (UVLO), VCC over voltage (VCC_OVP), over load, input under/ over voltage , external / internal over temperature , cycles by cycles current limitation…. ect. To ensure reliable operation at elevated temperatures, a user configurable current fold-back circuit is also provided.

Feature

- Wide Input Voltage Range: 85~277Vac
- Fast Start up Controller by ST pin (< 0.5Sec)
- Primary Side Feedback Controller
- Line Feed forward for Enhanced Accuracy
- Tight Constant Current Regulation (+/-2%,typ.)
- Power Factor Correction (> 0.9,typ)
- Optimization Total Harmonic (< 10%,typ)
- Dimming function by DIM pin
  - DC dimming input range : 0.5V~2.5V
  - PWM dimming input range : 800Hz~2KHz
- Robust Protection Features
  - Brown−In/Out Detections by VS pin
  - AC input Over Voltage Protection by VS pin
  - Over Voltage Protection on VCC pin
  - Programmable Open LED (OVP) Protection on ZCD or SD pin
  - Cycle−by−cycle Peak Current Limit
  - 2rd Current Limited Protection (CSP)
  - Current Sense Short Circuit Protection (CSCP)
  - Output Short Circuit Protection
  - Thermal Fold-back on SD pin by External NTC
  - Internal Over Temperature Protection

Applications

- AC-DC LED Lighting Driver

Typical Application

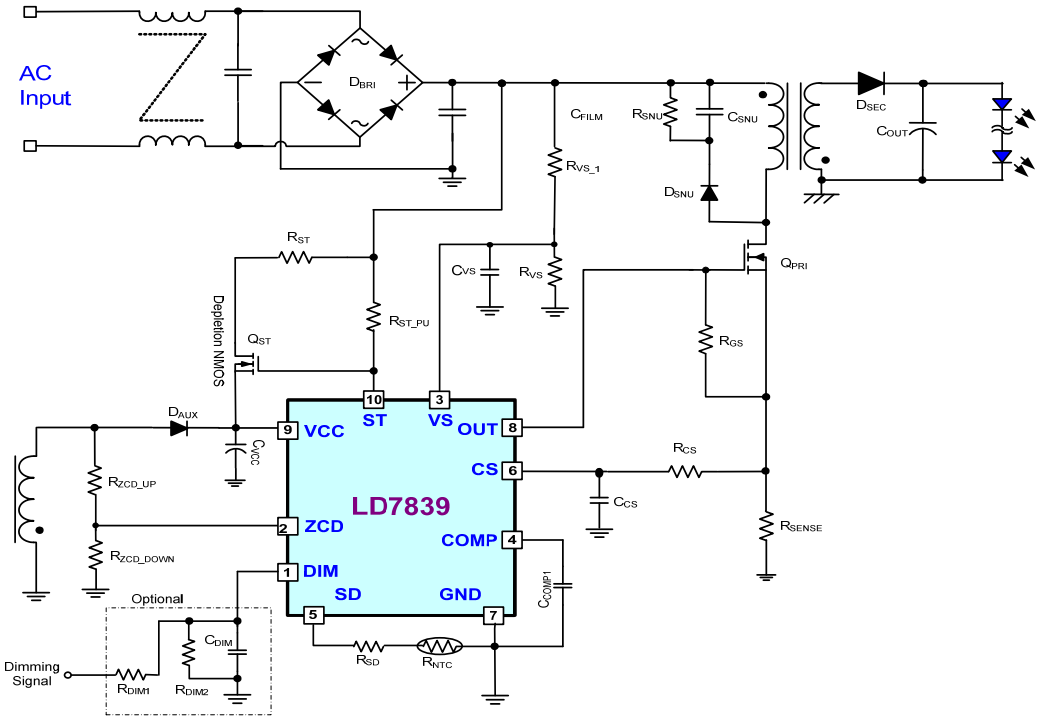


Figure.1 Reference Circuit Design for Flyback Topology

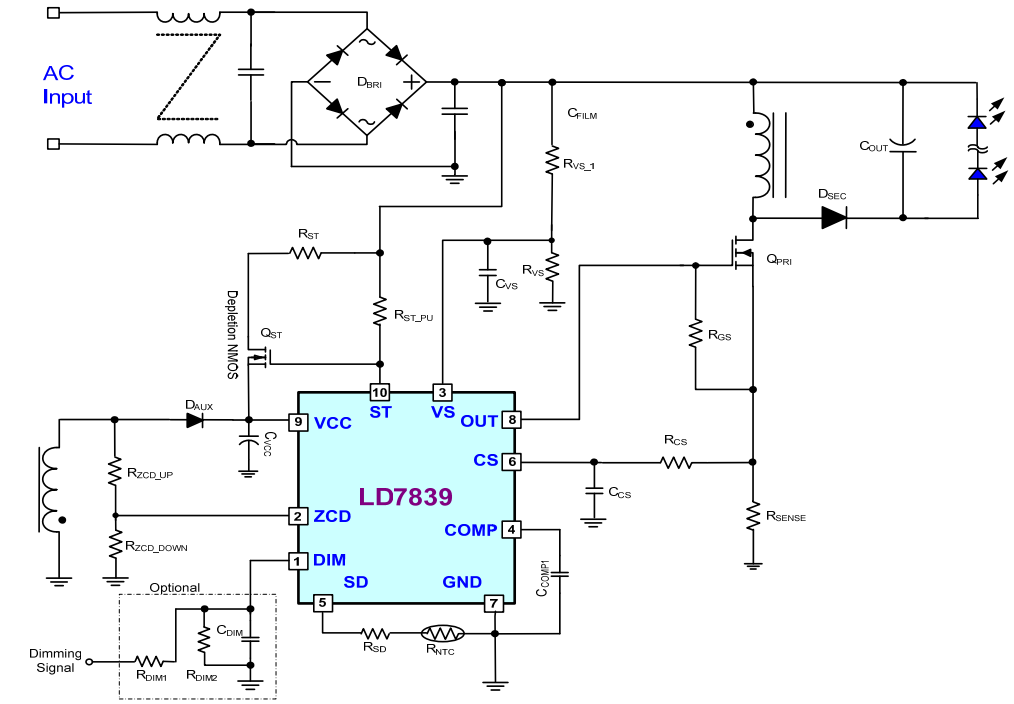
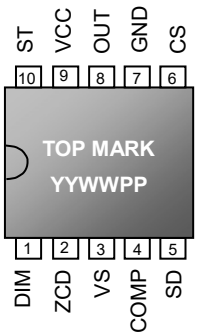


Figure.2 Reference Circuit Design for Buck Boost Topology

Pin Configuration

SOP-10 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7839GJ	SOP-10	LD7839GJ	2500 /tape & reel

The LD7839 GJ is ROHS compliant/ green packaged.

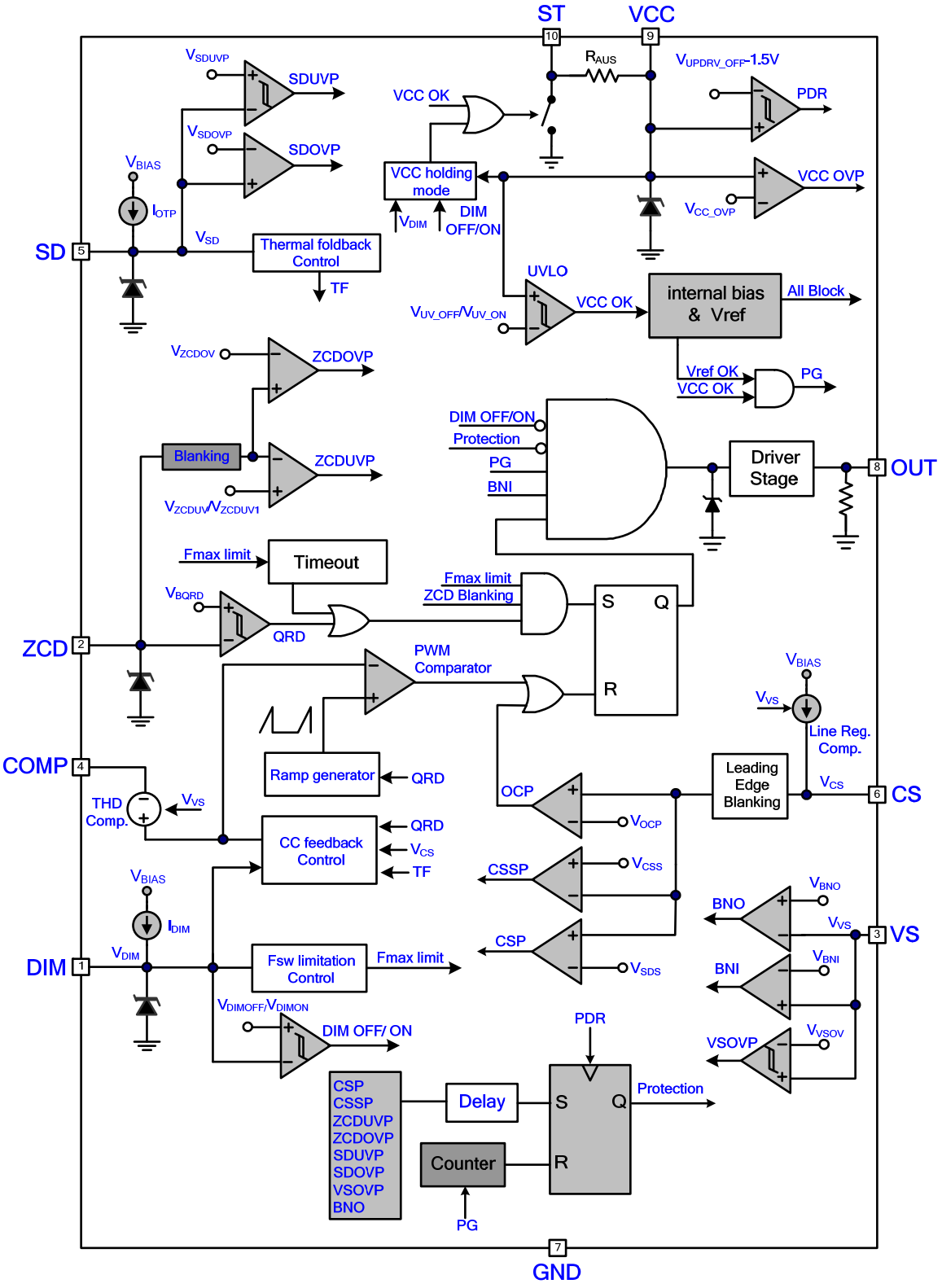
Protection Mode

Item	VCC_OVP ZCD_OVP	SD_UVP	SD_OVP	CSP	CSSP	ZCD_UVP	VS_OVP
LD7839GJ	Auto 1 hiccup	Auto 2 hiccup	Auto 4 hiccup	Auto 7 hiccup	Auto 7 hiccup	Auto 7 hiccup	Auto 1 hiccup

Pin Descriptions

Pin Number	NAME	FUNCTION
1	DIM	This pin is used for dimming control. A dimming signal is varied between 0.5V and 2.5V to adjust the LED current. When this V_{DIM} is lower than 0.5V, IC's gate is no switching.
2	ZCD	Quasi resonance and output voltage condition detector.
3	VS	Input voltage detector for brown in/out, high/low line condition, input over voltage protection and line regulation compensation.
4	COMP	This pin is connected to a loop compensation circuit. Recommend capacitance is from 0.47μF to 2.0μF.
5	SD	This pin programs thermal fold-back function by connecting a NTC to GND. Add an external Zener diode to AUX-winding for LED open protection or over voltage protection.
6	CS	This pin monitors primary side current for output constant current and over peak current protection.
7	GND	Ground. Power return.
8	OUT	Driving to the external MOSFET.
9	VCC	This pin is the positive supply of the IC. The operating range is recommended on 10V to 25V.
10	ST	Active start-up and bleeder control. Driving JFET (Depletion NMOS) or BJT and diode circuit to improvement start up time.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3 ~32V
ST	-0.3 ~ 30V
OUT	-0.3 ~ 20V
COMP, VS, DIM, CS, ZCD	-0.3 ~6V
CS (Bandwidth ≦ 300ns)	-0.8 ~6V
ZCD (Bandwidth ≦ 300ns)	-0.5 ~6V
ZCD source current	2mA
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-10, θ_{JA})	160°C/W
Power Dissipation (SOP-10, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
VCC operation voltage range Note1	12	25	V
Capacitance of VCC pin	10	47	μF
Operating junction temperature Note3	-40	125	°C
Capacitance of COMP pin	0.47	2.0	μF
Capacitance of ZCD pin filter	3	22	pF
Capacitance of CS pin filter	47	470	pF
Resistance of CS pin filter	0.1	2.0	kΩ
Capacitance of SD pin filter	10	47	nF
Capacitance of DIM pin filter	0.1	1	μF
Capacitance of VS pin filter	0.1	1	nF
Resistance of ST pin for HV start-up	1	3	MΩ

Note：

1) It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2) Exceeding these ratings may damage the device.
3) This product guarantees robust performance from -20°C to 105°C ambit temperature. The specification of junction temperature range is assured by design, characterization and correlation with statistical process controls.
4) When operation at harsh environment condition, as temperature and humidity or climate change …etc. Please pay attention to impedance variation between pin to pin or ground to avoid ripple remover closing loop and being failure.

Electrical Characteristics

(VCC=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Line Detection (VS Pin)						
Brown−In Threshold Voltage	After VCC > V_{UV_ON}	V_{BNI}	0.92	1.0	1.08	V
Brown−In De-bounce Time	*	T_{BNI}		1	25	ms
Brown−Out Threshold voltage	Before VCC > V_{UV_OFF}	V_{BNO}	0.82	0.9	0.98	V
Brown−Out De-bounce Time	*	T_{BNO}		20		ms
VS OVP Threshold Voltage	Gate off and COMP pull low	V_{VSOV}	3.8	4.0	4.2	V
VS OVP Hysteresis Voltage	*	V_{HVSOV}		-0.1		V
VS OVP Enable De-bounce Time	*	T_{VS_OV}		385		μs
Threshold for High− Line Range (HL) Detection	$T_{ON\_MAX\_H}$= 0.425 * $T_{ON\_MAX\_L}$	V_{HL}	1.95	2.10	2.20	V
Hysteresis for V_{HL} to V_{LL}	*	V_{H_HLLL}		-0.15		V
V_{VS} to I_{CS} Conversion Ratio	Source current from CS pin when V_{VS}=1.5V & 3.5V	K_{LINE}	18	20	22	μA/V
Supply Voltage (VCC Pin)						
Startup Current	VCC ≦ V_{UV_ON}	I_{ST}		50	100	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP} = 0V, V_{ZCD} = 0V	I_{OP_LO}		1.1		mA
	V_{COMP} ≧ 3V, V_{ZCD} = 2V	I_{OP_HI}		1.5		mA
	*; During Protection	I_{OP_PROT}		0.4		mA
De-Latch Voltage	*	V_{PDR}	V_{UV_OFF}-1.5V			V
UVLO_OFF Threshold Voltage		V_{UV_OFF}	7.5	9.0	10.5	V
UVLO_ON Threshold Voltage		V_{UV_ON}	17.0	18.5	20.0	V
VCC Holding Clamp High Level	When V_{DIMOFF} < V_{DIM} ≦ V_{DIMHO}	V_{VCCUV1_H}	12.1	13.0	13.9	V
VCC Holding Clamp Low Level	When V_{DIMOFF} < V_{DIM} ≦ V_{DIMHO}	V_{VCCUV1_L}	10.8	11.5	12.2	V
VCC_OVP Threshold Voltage		V_{CC_OVP}	25.8	27.5	29.2	V
VCC_OVP De-bounce Time	*	T_{DEB_OVP}		250		μs
Protection De-Latch Counter	*;VCC_OVP, ZCD_OVP, VS_OVP	Hiccup1		1		Number
	*;SD_UVP	Hiccup2		2		Number
	*;SD_OVP	Hiccup3		4		Number
	*;SDSP,CSSP, ZCD_UVP	Hiccup4		7		Number
Start-up Section (ST pin)						
Resistance of VCC to ST Pin.	*;When VCC ≧ UVLO_ON ,ST pull low immediately.	R_{AUS}	0.8	1.2	1.5	MΩ

(VCC=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
CC Integrator (COMP Pin)						
COMP Open Voltage	*	V_{COMP_HCL}	4.4	4.7	5.0	V
Burst Mode In Level (Zero on time)	On time is Zero(gate off)	$V_{COMPL1L}$	0.55	0.65	0.75	V
Burst Mode Out Level		$V_{COMPL1H}$	0.9	1.0	1.1	V
Current Sensing (CS Pin)						
Current Limit Threshold Voltage		V_{OCP}	0.9	1.0	1.1	V
Current Limit-2 Threshold Voltage	Duration T_{LEB} region. If it's enable, OUT pin is pull low immediately.	V_{SDS}	0.52	0.60	0.68	V
De-bounce Cycle of Current Limit-2 Protection	*; continuously	T_{SDSP}		7		Cycles
Soft Start Time	*; V_{CS} is from 0.2V to 1.0V	T_{SS}			30	ms
CS Short Protection Threshold Voltage	OUT is from high to low.	V_{CSS}	85	125	165	mV
CS short Protection De-bounce Time	*; including soft start time and V_{COMP} > 2V.	T_{CSSP}		90		ms
LEB time and Programming Delay Time	*; include gate off delay time (100ns,typ) on chip	T_{LEB}		250		ns
KCC Tolerance		KCC_T		±2		%
Maximum OFF-Time						
Timeout after Switching Period	*; Always	T_{O1}	4.5	6.5	8.5	μs
Minimum ON -Time						
Minimum Turn On Time	*; when V_{VS} > 2.1V	T_{ON_MIN}		450		ns
Maximum ON -Time						
Maximum Turn On Time	When R_{ZCD} setting is 20kΩ	T_{ON_MAX1}	15.2	18.5	21.8	μs
	When R_{ZCD} setting is 10kΩ	T_{ON_MAX2}	11.2	13.5	15.8	
Minimum (ON+OFF)-Time						
Minimum ON+OFF-Time	F_{S_MAX} ≒ 90kHz	T_{S_MIN}	9.5	11.5	13.5	μs
	F_{S_MIN} ≒ 20kHz	T_{S_MAX}	40	50	60	μs
	*; F_{S_SS}≒ 30kHz	T_{S_SS}		33		μs
Gate Drive Output (OUT Pin)						
Output Low Level	I_{SINK}=20mA	V_{G_LO}	0		0.8	V
Output High Level	I_{SOURCE}=20mA	V_{G_HI}	10		13	V
Output High Clamp Level	*	V_{G_CLAMP}		13		V
Rising Time*	*; C_{OUT}=1000pF	T_{G_RISE}		140		ns

(VCC=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)						
Falling Time*	*; C_{OUT}=1000pF	T_{G_FALL}		30		ns
Zero Current Detector (ZCD Pin)						
Upper Clamp Voltage	When I_{ZCD} = 200μA	V_{ZH}	4.4	4.7	5.0	V
Lower Clamp Voltage	When I_{ZCD} = - 2mA	V_{ZL}	0		-0.3	V
QRD Threshold Voltage		V_{BQRD}		0.3		V
Hysteresis of QRD	Leading edge	VH_{ZCD}		+0.1		V
Blanking Time	*; when $V_{DIM} > V_{DIM50}$	T_{BNK_ZCDL}	2.0	2.4	2.8	μs
	*; when $V_{DIM} \leqq V_{DIM50}$	T_{BNK_ZCDH}	1.2	1.6	2.0	μs
ZCDUVP Threshold Voltage	$V_{DIM} \geqq 1.1V$	V_{ZCDUV}	0.9	1.0	1.1	V
	$V_{DIM} < 1.1V$	V_{ZCDUV1}	0.7	0.8	0.9	
ZCDUVP Delay Time	*; including soft start time.	T_{UVP}		180		ms
ZCDOVP Threshold Voltage	Detection point on gate off after Blanking Time	V_{ZCDOV}	3.90	4.05	4.20	V
ZCDOVP De-bounce Time	*	T_{DEB_CV}		250		μs
Dimming Function (DIM pin)						
DIM Clamp Voltage	DIM pin open	V_{DIM_CLH}	2.65	2.70		V
Source Current of DIM Pin	Source current	I_{DIM}	9.0	10.0	11.0	μA
DIM100 Threshold Voltage		V_{DIM100}	2.37	2.50	2.63	V
DIM50 Threshold Voltage	*	V_{DIM50}	1.35	1.45	1.55	V
DIM0 Threshold Voltage	*; V_{DIM} from high to low.	V_{DIM0}	0.45	0.48	0.51	V
VCC Holding Mode start Threshold Voltage	$V_{DIMOFF} < V_{DIM} < V_{DIMHO}$ still $V_{DIM} < V_{DIMOFF}$ before 20mS,max	V_{DIMHO}	-	1.1	-	V
DIMOFF Threshold Voltage	Gate is not turn on if $V_{DIM} \leqq V_{DIMOFF}$	V_{DIMOFF}	0.45	0.50	0.55	V
DIMON Threshold Voltage	V_{DIM} from V_{DIMOFF} to gate on	V_{DIMON}	0.50	0.55	0.60	V
Frequency Limitation Start Threshold Voltage		V_{DIM_FS}	1.26	1.36	1.46	V
Frequency Limitation End Threshold Voltage		V_{DIM_FE}	0.68	0.78	0.88	V
Thermal Foldback Function (SD pin)						
SD Clamp Voltage	SD pin open	V_{SD_CLA}	1.55	1.75		V
Clamped Resistance	*	R_{SD_CLA}		2.0		kΩ
SDOVP Threshold Voltage		V_{SDOVP}	2.9	3.0	3.1	V
SDOVP De-bounce Time	*; $V_{SD} \geqq V_{SDOV}$	T_{SDOV}		250		μs
SDUVP Threshold Voltage		V_{SDUVP}	0.45	0.5	0.55	V
Hysteresis of SDUVP	*; When IC start up first	V_{H_SDUVP}		+0.1		V

(VCC=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Thermal Foldback Function (SD pin)						
SDUVP De-bounce Time	*; V_{SD}<V_{SDUV}	T_{SDUV}		600		μs
Source Current of SD Pin		I_{OTP}		82		μA
Thermal Foldback Start Threshold Voltage		V_{TF_START}	1.0	1.1	1.2	V
Thermal Foldback End Threshold Voltage	Reduce current to 50%,typ.	V_{TF_STOP}	0.55	0.65	0.75	V
Internal OTP (Over Temp. Protection)						
OTP Junction Trip Level*	Gate off then Hiccup	OTP		140		°C

*: Guaranteed by design.

Application Information

Operation Overview

The LD7839 is an excellent single-stage flyback PFC controller with dimmable constant current and primary side regulation (PSR) control algorithm for LED lighting applications. It drives converter operating in quasi-resonant mode to achieve high efficiency. By PSR, The LD7839 is feedback accurately with primary side current without the shunt regulator and opto-coupler at secondary side. LD7839 is a QR/DCM mode and voltage-mode PFC controller. The turn-on time of the switch is fixed while the turn-off time is varied in steady state. Therefore, the switching frequency varies in accordance with the input voltage or output power variation. The maximum switching frequency is limited about 90kHz and minimum switching frequency is limited about 20kHz. The LD7839 can support analog dimming by adjusting the voltage of DIM pin. LD7839 provides robust protections as over load protection, over voltage protection, over current protection, under voltage lockout and LEB of the current sensing. Specially, LD7839 also provide thermal foldback function by programmable NTC. Its major features are described as below.

External High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance.

To achieve optimized topology, as shown in Fig. 3, LD7839 drive a high-voltage startup circuit to enhance it. When input voltage is applied, ST pin is pulled high by resistor (R_{ST_PU}) and high voltage switch (Q_{ST}, It is BJT + Diode or Depletion NMOS) is turned on. VCC capacitor (C_{VCC}) is charged by R_{ST} and Q_{ST}. The voltage of ST pin (V_{ST}) increased with VCC pin. Once the VCC voltage reaches start-up threshold (V_{UVLO_ON}), LD7839 is activated and ST pin is pulled low, Q_{ST} is turned off at the same time and finished the start-up sequence. As shown in Fig. 4. In using such configuration, the turn-on delay time will be almost no difference either in low-line or high-line conditions. Once the VCC voltage rises higher than V_{UVLO_ON} to power on the LD7839 and further to deliver the gate drive signal, Q_{ST} will be turn off and the supply current is provided from the auxiliary winding of the transformer. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

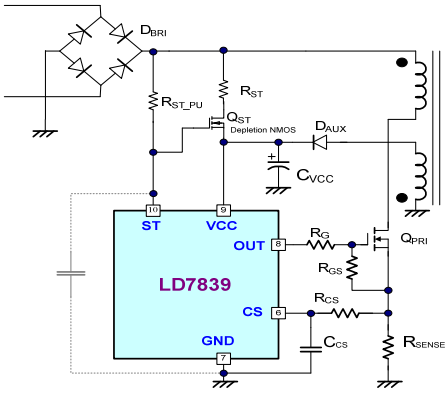


Fig. 3 Start up circuit

An UVLO comparator is embedded to detect the voltage on the VCC pin to ensure the supply voltage enough to power on the LD7839 PWM controller and in addition to drive the power MOSFET.

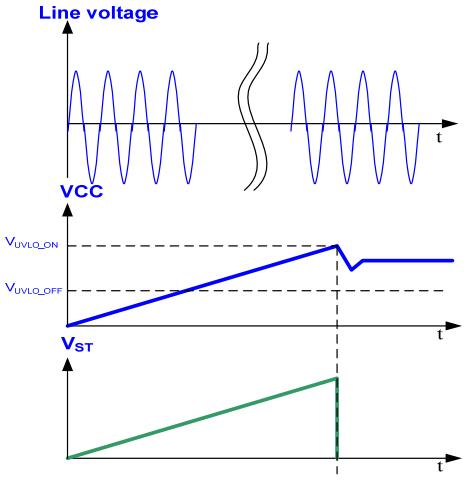


Fig. 4 Start up Sequence

Brown-In/Out and AC Input Over Voltage Protection (VS_OVP)

The LD7839 features brown-in/out function on VS pin. As the built-in comparator detects the condition of V_{VS} which is input voltage divided by R_{VS}, it will shut off the controller to prevent from any damage. Fig. 5 shows the operation. When V_{VS}<V_{BNO} (0.9V, typically), the gate output will remain off even when the VCC already reaches V_{UVLO_ON}. It therefore forces the VCC hiccup between V_{UVLO_ON} and V_{UVLO_OFF}. Unless the input voltage rises over V_{BNI} (1.0V, typically), the gate will not start switching even as the next V_{UVLO_ON} is tripped. A hysteresis is implemented to prevent the false-triggering during turn-on and turn off.

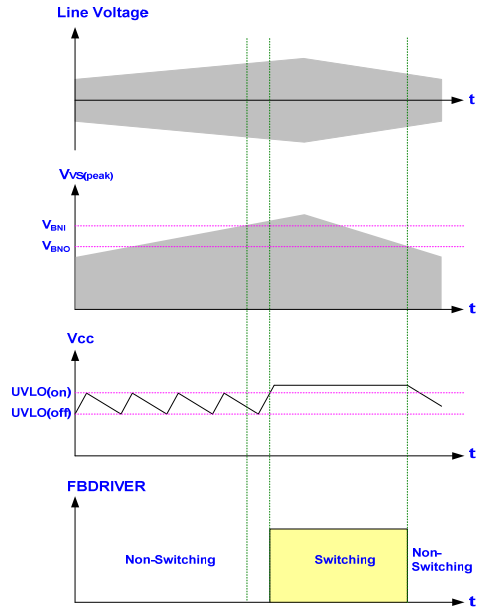


Fig. 5 BNI/BNO function

As shown in Fig. 6 and 7. When V_{VS} is higher than V_{VSOV} (4.0V, typically) for 385μs delay, VS_OVP is trigger. V_{COMP} is pulling low and LD7839 will enforce the gate off until the 1st cycle of VCC hiccup is tripped and V_{VS} is lower than V_{VSOV} – 0.1V.

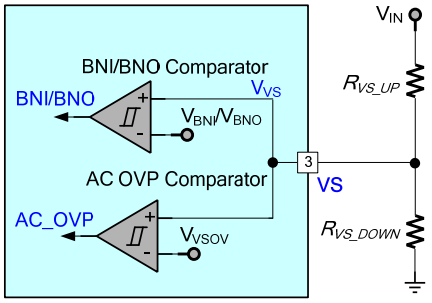


Fig. 6 AC_OVP circuit

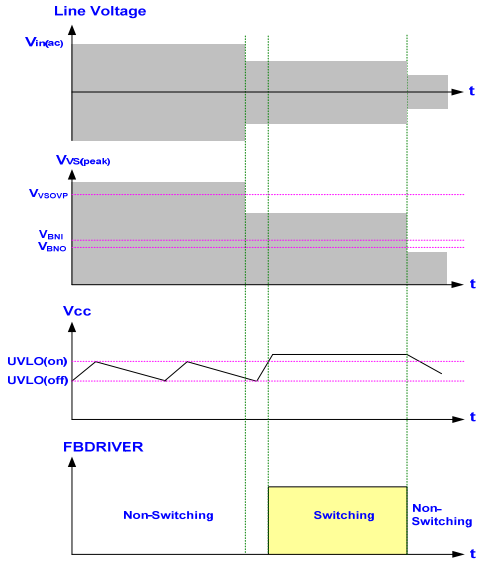


Fig. 7 AC_OVP Protection

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 8 shows typical ramp generator block and ZCD block. The COMP pin voltage (V_{COMP}) and the output of the ramp generator block are compared to determine the MOSFET on-time, as shown in Fig. 9.

A greater comp voltage produces more on-time. Using an external resistor connected to ZCD pin to set the desired slope of the internal ramp, the user may program the maximum on-time. Alternatively, the on-time will also achieve its maximum when V_{COMP} trip to V_{COMP_HCL} (4.7V, typically).

The maximum on-time (T_{ON_MAX}) should be set according to the condition of the transformer, lowest AC

line voltage, and maximum output power. A choice of optimum resistor value would result in best performance.

It shuts down the drive output if V_{COMP} falls below zero on-time threshold voltage. This optimizes the efficiency in power saving in most conditions.

The zero current detection block will detect auxiliary winding signal to drive MOSFET as ZCD pin voltage (V_{ZCD}) drops to 0.3V. As V_{ZCD} drop to 0.3V, the current through the transformer is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if V_{ZCD} remains at above 0.4V. Once it drops below 0.3V, the zero current detector will act to turn on the MOSFET.

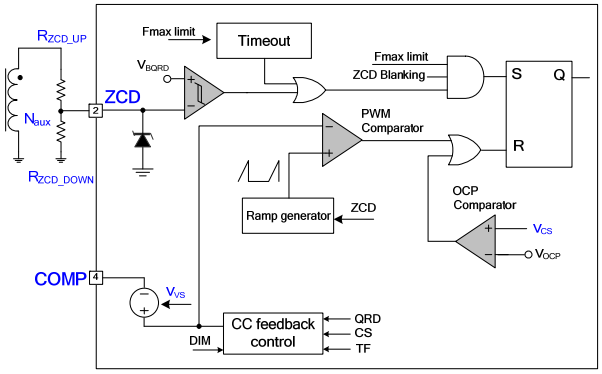


Fig. 8 ZCD function block

Fig. 9 shows typical ZCD-related waveforms. Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from R_{ZCD_UP}. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

Programming Maximum On-Time

LD7839 provides adjustable maximum on-time to limit power output in abnormal operation. The selection of maximum on-time is subject to ZCD resistance as shown in Fig. 10. ZCD resistance can be obtained from below, but order to avoid ZCD pin over rating, I_{ZCD} must be set lower than 2mA.

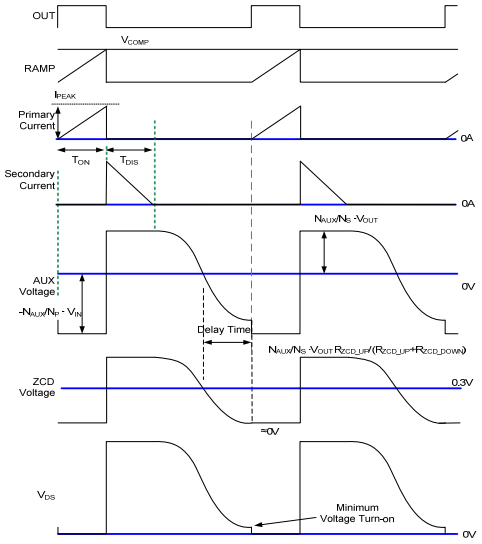


Fig. 9 ZCD detection

The following table is a suggestion for maximum on-time setting.

R_{ZCD} (Ω)	T_{ON,MAX_LL}	T_{ON,MAX_HL}	R_{ZCD_DOWN} Suggestion
R_{ZCD} > 20kΩ	18.5μs	~8μs	25kΩ
R_{ZCD} <10kΩ	13.5μs	~6μs	7.5kΩ

Table. 1

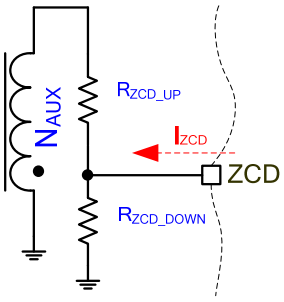


Fig. 10 ZCD Setting

Where:

$$R_{ZCD}=\frac{R_{ZCD\_UP}\times R_{ZCD\_DOWN}}{R_{ZCD\_UP}+R_{ZCD\_DOWN}}$$

$$I_{ZCD}=\frac{V_{IN,PEAK}}{R_{ZCD\_UP}}\times\frac{N_{AUX}}{N_P}$$

Principle of Constant Current Operation

Primary side control is applied to eliminate secondary feedback circuit or opto-coupler to reduce the circuit cost. The switching waveforms are shown in Fig.11.The output current I_{OUT} as follows:

$$I_{OUT}=\frac{1}{2}\times\frac{I_{S,PK}\times T_{DIS}}{T_S}$$
$$=\frac{1}{2}\times\frac{N_P}{N_S}\times I_{P,PK}\times\frac{T_{DIS}}{T_S}$$
$$=\frac{1}{2}\times\frac{N_P}{N_S}\times\frac{V_{CS}}{R_{SENSE}}\times\frac{T_{DIS}}{T_S}$$

The primary peak current ($I_{P,PK}$), inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC. The ratio of V_{CS} x T_{DIS}/T_S will be modulated as a constant. Maximum output mean current $I_{OUT,MAX}$ can be induced finally as follows:

$$I_{OUT,MAX}=\frac{1}{2}\times\frac{N_P}{N_S}\times\frac{V_{CS}}{R_{SENSE}}\times\frac{T_{DIS}}{T_S}$$
$$\sim\frac{1}{2}\times\frac{N_P}{N_S}\times\frac{0.5V}{R_{SENSE}}\times(1-K)\times\eta_{TR}$$
$$\sim\frac{1}{2}\times\frac{N_P}{N_S}\times\frac{0.5V}{R_{SENSE}}\times(1/K_{CC})\times\eta_{TR}$$

Where K = (T_{ON}/T_S) = (1- T_{DIS}/T_S) and $K_{CC}\fallingdotseq 3.5$, which are measured at V_{CS} =0.5V and $V_{ZCD}\geqq 2V$. η_{TR} is coupling coefficient of transformer that is about 0.90~0.99. So, $I_{OUT,MAX}$ can be programed by N_P/N_S and R_{SENSE} easily.

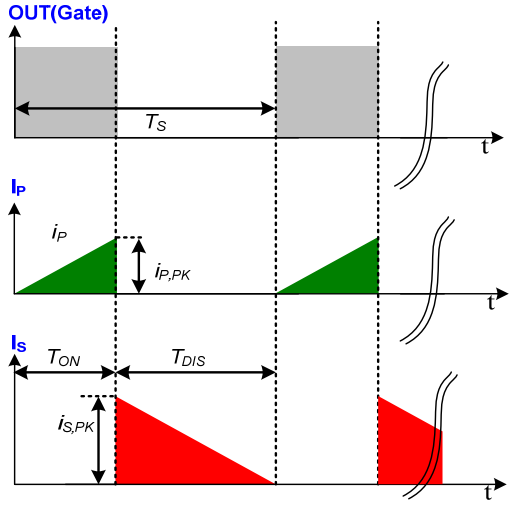


Fig. 11 Switching current

Dimming Performance and Frequency Limitation

Apply DC voltage on DIM pin to achieve analog dimming of LED current. LED current could be controlled by V_{DIM} as follow:

If $V_{DIM}\leq V_{DIM0}$, I_{OUT}=0A

If $V_{DIM}\geq V_{DIM100}$, $I_{OUT}=I_{OUT,MAX}$

If $V_{DIM0}<V_{DIM}<V_{DIM100}$,

$$I_{OUT}=\left(\frac{V_{DIM}-V_{DIM0}}{V_{DIM100}-V_{DIM0}}\right)\times I_{OUT,MAX}$$

Where, V_{DIM0} and V_{DIM100} respectively are 0.5V and 2.5V typically.

Once $V_{DIM}\leqq V_{DIMOFF}$, LD7839 will gate off immediately. But if this condition is continuously and last more than 20ms, V_{COMP} is pulled low until V_{DIM} > V_{DIMON} again. If $V_{DIM}\leqq V_{DIMOFF}$ but less than 20ms, when $V_{DIM}\geqq V_{DIMON}$, LD7839 will gate on immediately.

DIM pin also control switching frequency limitation, When V_{DIM} lower than V_{DIM_FS} (1.36V, typically), maximum switching frequency limitation is reducing proportional to V_{DIM} until V_{DIM} is equal to V_{DIM_FE} (0.78V, typically). The minimum switching frequency is ~20kHz, maximum switching frequency is 90kHz, typically, as shown in Fig. 12.

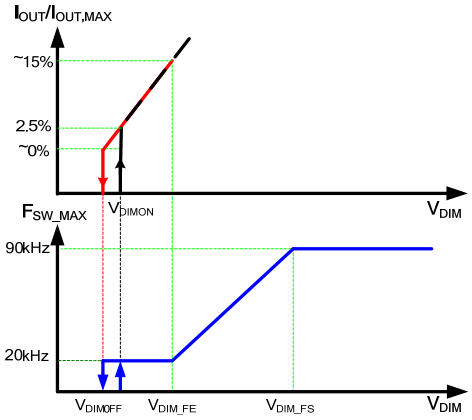


Fig. 12 Dimming Performance

Thermal Fold Back by SD Pin

LD7839 provides the thermal fold-back function by SD pin as follow:

If $V_{SDUVP} \le V_{SD} \le V_{TF\_STOP}$, $I_{OUT}=50\%\times I_{OUT,NOM}$

If $V_{SD} \ge V_{TF\_START}$, $I_{OUT}=100\%\times I_{OUT,NOM}$

If $V_{TF\_STOP} < V_{SD} < V_{TF\_START}$

$$I_{OUT}=\left(\frac{V_{TF\_START}-V_{TF\_STOP}}{2\times V_{TF\_START}-V_{TF\_STOP}-V_{SD}}\right)\times I_{OUT,NOM}$$

$$V_{SD}=I_{SD}\times R_{NTC}$$

Where, V_{TF_START}, V_{TF_STOP} and V_{SDUVP} respectively, are 1.1V, 0.65V, 0.5V typically. $I_{OUT,NOM}$ is the output current which is controlled by DIM pin. Connect a NTC between SD and GND pin, as shown in Fig. 13.

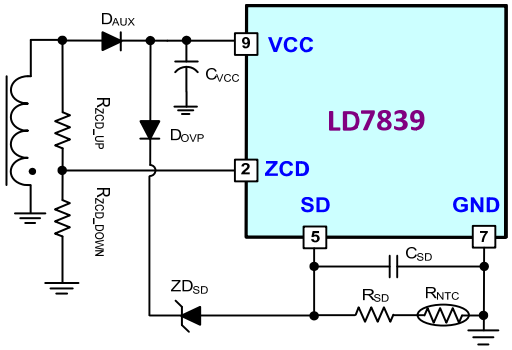


Fig.13 SDOVP and external OTP

The SD pin is clamped at V_{SD_CLA} (1.75V typically), Once V_{SD} is higher than V_{SDOVP} (3.0V typically), SDOVP is triggered, LD7839 will enforce the gate off until the 4th cycle of VCC hiccup is tripped. Add an external Zener diode (ZD_{SD}) can adjust the LED open protection or output over voltage protection. The maximum output voltage as follows:

$$V_{OUT,MAX} \approx [(V_{ZD_{SD}}+V_{D_{OVP}})+3.0V]\times\frac{N_S}{N_{AUX}}$$

VCC Holding Mode

VCC may not enough at lower output voltage and dimming low condition, LD7839 provide the VCC holding mode to enhance the wide operation range. Once the V_{DIM} is lower than V_{DIMHO} (1.1V, typically) and VCC is lower than V_{VCCUV1_L}, ST pin will pull high by R_{ST_PU}, C_{VCC} charge by R_{ST}. VCC voltage will be clamped between V_{VCCUV1_H} and V_{VCCUV1_L}, as shown in Fig. 14. If V_{DIM} is lower than V_{DIMOFF} about 20ms, the VCC holding mode is disabled.

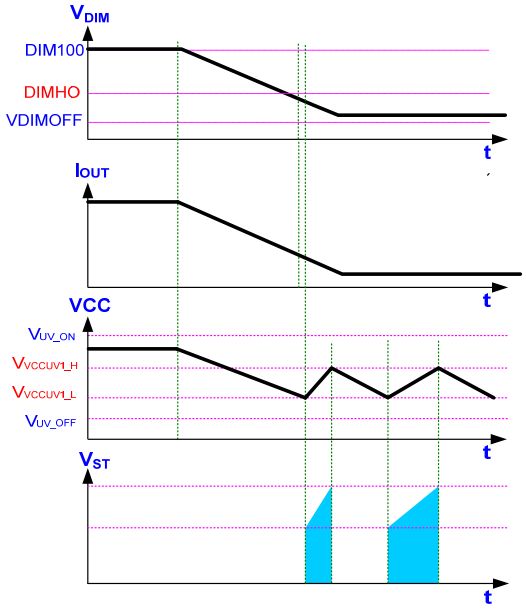


Fig.14 VCC holding mode

Output Drive Stage

With typical 250mA/-500mA peak driving capability, an output stage of a CMOS buffer is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Leading-Edge Blanking and Cycle by Cycle Limit

A 250ns leading-edge blanking time (T_{LEB}) is included in the input of CS pin to prevent the false-trigger from the current spike. In the different rated power application, if the total pulse width of the turn-on spikes is lower than and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller

R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

LD7839 detect the primary side peak current from the CS pin, which is not only for constant current regulation but also for cycle by cycle peak current limit. The maximum voltage threshold of the CS pin set at V_{OCP} (1.0V, typically), once V_{CS} is higher than V_{OCP}, gate off immediately.

Once V_{CS} exceeds V_{SDS} (0.6V, typically) during T_{LEB} -100ns after gate on, LD7839 will gate off immediately, if 7 switching cycles continuously with this situation, LD7839 will enforce the gate off until the 7th cycle of VCC hiccup is tripped.

Line Regulation Compensation

The line regulation could be compensation by fine tuning R_{CS}. To compensate this, an offset voltage is added to the CS signal by an internal current source (I_{CS}) when gate on duration through an external resistor (R_{CS}) in series between the sense resistor (R_{SENSE}) and CS pin, as shown in Fig. 15.

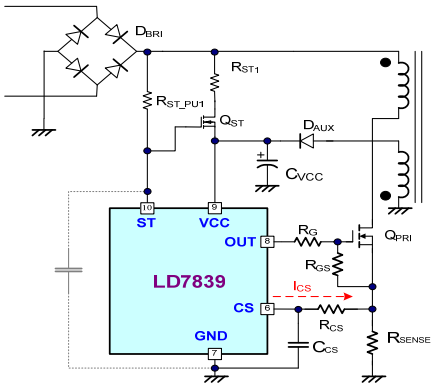


Fig. 15 Line Regulation Compensation

And I_{CS} is defined by V_{VS} as below.

$$I_{CS} = V_{VS} \times K_{LINE} = V_{VS} \times 20\mu A/V$$

By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted.

Output OVP on ZCD Pin-1 Hiccup

When the LED string open circuit occurs, the reflected output voltage of AUX-winding will cause ZCD voltage up. If the ZCD voltage is higher than V_{ZCDOV} (4.05V, typically) and de-bounce about 250μs, LD7839 will enforce the gate off until the 1st cycle of VCC hiccup is tripped, the selection of output over voltage (V_{OVP}) trigger level is subject to ZCD divide resistance as the below equation:

$$V_{OVP} \times \frac{N_{VCC}}{N_S} \times \frac{R_{ZCD\_DOWN}}{R_{ZCD\_UP}+R_{ZCD\_DOWN}} = 4.05V$$

UVP (OSCP) on ZCD Pin-7 Hiccup

When the LED string short circuit occurs, the reflected output voltage of aux winding will cause ZCD voltage down. If V_{VS} is lower than V_{HL} (2.1V, typically) and the ZCD voltage fall to V_{ZCDUV} (1V, typically) or V_{VS} is higher than V_{HL} and the ZCD voltage fall to V_{ZCDUV1} (0.8V, typically), de-bounce about 180ms, LD7839 will enforce the gate off until the 7th cycle of VCC hiccup is tripped.

VCC Over Voltage Protection – 1 Hiccup

The maximum rating of the VCC pin is limited below 30V. To prevent VCC from the fault condition, the LD7839 is implemented with OVP function on VCC pin. As soon as the VCC pin voltage is higher than V_{CC_OVP} (27.5V, typically) and de-bounce about 250μs, Ics will enforce the gate off until the 1st cycle of VCC hiccup is tripped.

Output OVP on SD Pin- 4 Hiccup

When the V_{SD} is higher than V_{SDOVP} (3V, typically) and de-bounce about 250μs, LD7839 will enforce the gate off until the 4th cycle of VCC hiccup is tripped.

UVP (External OTP) on SD Pin- 2 Hiccup

When over temperature condition occurs, the resistance of NTC is decreased with temperature. Once V_{SD} is lower than V_{SD_UVP} (0.5V, typically) and still about 600μs, LD7839 will enforce the gate off until the 2nd cycle of VCC hiccup is tripped. Once the SDUVP is active,

LD7839 recovery until the V_{SD} is higher V_{SD_ON} (0.6V, typically) again. As shown in Fig. 16.

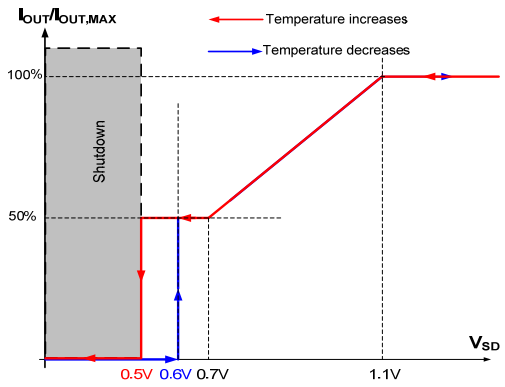


Fig. 16 Thermal Fold-back

Short Circuit Protection on CS Pin-7 Hiccup

To protect the circuit from damage due to CS pin short condition, a smart and robust function is implemented in the LD7839 for it. This function is an auto recovery type protection. Under such fault condition, Once V_{CS} is lower than V_{CSS} (0.125V, typically) and V_{COMP} is higher than 2V(typically), after de-bounce about 90ms, LD7839 will enforce the gate off until the 7th cycle of VCC hiccup is tripped. As shown in Fig. 17.

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply:

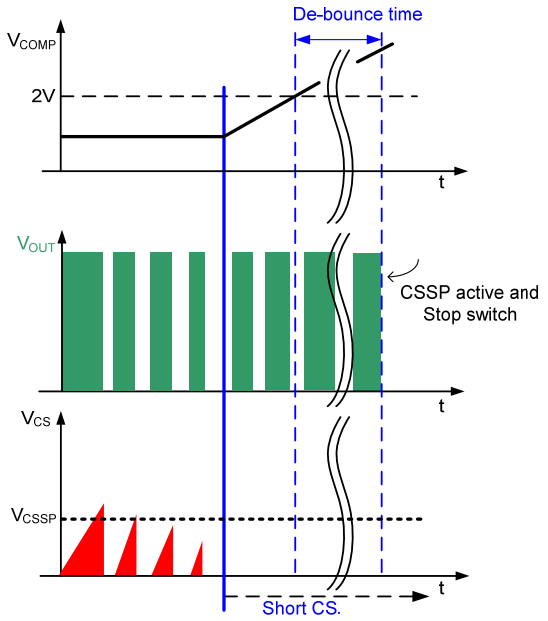


Fig. 17 Current Sense Short Circuit Protection

The current path(1) from the input capacitor, transformer, MOSFET, RCS returning to input capacitor is a high frequency current loop. The path(2) from GATE pin, MOSFET, RCS returning to the ground of the IC is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(3) between MOSFET ground(b) and IC ground(d) is recommended to be as short as possible, too.

The path(4) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.

The path(5) from the input capacitor to VDD pin is a high voltage loop. Keep a space from path(5) to other low voltage traces.

It is good for reducing noise, output ripple and EMI issue to separate ground traces of the input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together at the input capacitor ground(a). The areas of these ground traces should be kept large.

To reduce the parasitic trace inductance and EMI, the area of the loop connecting to the secondary winding, the output diode, and the output filter capacitor must be minimized. In addition, the sufficient copper area at the anode and cathode terminal of the output diode can help for heat-sinking. It is recommended to apply the larger area at the quiescent cathode terminal. The large anode area will induce high-frequency radiated EMI.

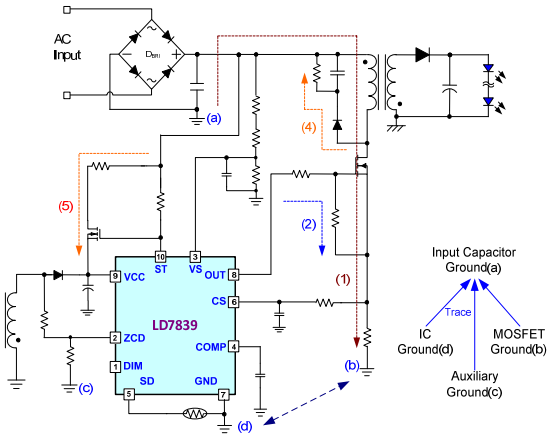
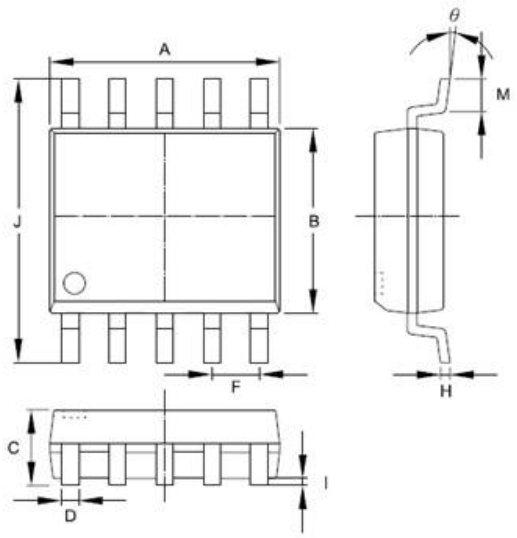


Fig. 18 PCB layout Consideration

Package Information

SOP-10



LEADTREND / SOP-10				
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	4.800	5.000	0.189	0.197
B	3.800	4.000	0.150	0.157
C	1.300	1.750	0.051	0.069
D	0.300	0.500	0.012	0.020
F	1.0 TYP.		0.039 TYP.	
H	0.170	0.250	0.007	0.010
I	0.100	0.250	0.004	0.010
J	5.800	6.200	0.228	0.244
M	0.400	1.27	0.016	0.05
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
P00	10/01/2019	Original Specification
P01	12/25/2019	1. Modify the SDSP to CSP at protection mode table. 2. Modify block diagram. 3. Modify value and symbol of electrical characteristics table. 4. Modify maximum on time setting table.
P02	03/23/2020	1. Modify the minimum ON+OFF-Time (T_{S_MIN} &T_{S_MAX}) to maximum and minimum frequency (F_{S_MAX} & F_{S_MIN}). 2. Correct the SDUVP hysteresis voltage (+0.1V). 3. Modify Fig. 14 (VCC holding mode). 4. Add Fig.17 (Current Sense Short Circuit Protection). 5. Internal OTP function haven't hysteresis (few value).
P03	05/06/2020	1. Correct V_{SDOVP} (3V), page 15. 2. Add the description of DIM ($V_{DIM} \leqq V_{DIMOFF}$), page 13. 3. Modify description of VSOVP, page11. 4. Modify EC table V_{VCCUV1_H}, page6. 5. Modify EC table V_{VCCUV1_L}, page6. 6. Modify EC table T_{ON_MIN}, page7. 7. Modify EC table T_{LEB}, page7. 8. Modify EC table T_{BNK_ZCDL}, page8. 9. Modify EC table T_{BNK_ZCDH}, page8. 10. Modify Pin description (DIM), page3. 11. Modify feature (dimming), page1. 12. Add R_{AUS} at block diagram, page 4. 13. Modify operation current unit of EC table, page 6.