SENSYLINK Microelectronics

(CT7112)

Digital Temperature Sensor

CT7112 is a Digital Temperature Sensor with ±0.5°C Accuracy Compatible with SMBus, I^2C and 2-wire Interface.
It is ideally used in HVAC, Thermal management and Portable Devices etc.

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±0.5°C Digital Temperature Sensor with Digital Interface

Description

CT7112 is a digital temperature sensor with ±0.5°C accuracy. Temperature data can be read out directly via digital interface (compatible with SMBus, I²C or 2-wire) by MCU, Bluetooth Chip or SoC chip.

CT7112 supports I²C communication with speed up to400 kHz.

Each chip is specially calibrated for ±0.5°C(Max.) accuracy over 0°C to 50°C range in factory before shipment to customers. There is no need for re-calibration anymore for ±0.5°C accuracy.

It includes a high precision band-gap circuit, a 12-bit analog to digital converter that can offer 0.0625°C resolution, a calibration unit with non-volatile memory, and a digital interface block.

It has ALERT logic output pin with open drain structure, which is selectable for active low or high by programming. ALERT response is compatible with SMBus ALERT Response Address (ARA).CT7112 can also be used as standalone thermostat.

Available Package: DFN1.6x1.6-6 package

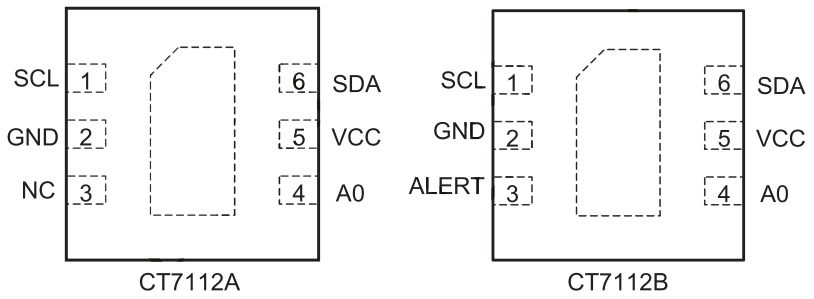
Features

- Operation Voltage: 1.7V to 5.5V
- Average Quiescent Current: 3uA(Typ.) 1Cov/s
- Standby Current: 1.5uA (typ.)
- Temperature Accuracy without calibration:
  Maximum:±0.5°C from 0°C to 50°C
  Maximum:±1.0°C from -40°C to 125°C
- 12 bit ADC for 0.0625°C resolution
- Compatible with SMBus, 2-wire and I²C interface
- Programmable Over/Under Temperature
- Programmable Active Low or High for ALERT pin
- Support SMBus ALERT Response Address(ARA)
- Generate 4 different slave address by setup A0 pin
- Temperature Range: -40°C to 125°C

Applications

- Smart HVAC System
- Thermal Management
- Portable Devices

PIN Configurations (Top View)



DFN1.6x1.6-6 (Package Code DN)

Typical Application

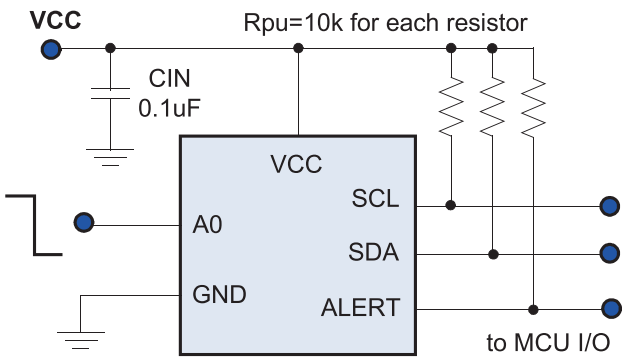


Figure 1. Typical Application of CT7112

Pin Description

PIN No.		PIN Name	Description
CT7112A	CT7112B		
1	1	SCL	Digital interface clock input pin, need a pull-up resistor to VCC.
2	2	GND	Ground pin.
3		NC	No Connection.
	3	ALERT	To Indicate ALERT of over or under Temperature programmed by setting T_{HIGH}/T_{LOW} register, it is open drain output with programmable active low or high. Need a pull-up resistor to VCC in application.
4	4	A0	Address selection pin, the chip can be defined total 4 different slave address by connecting this pin to GND, VCC, SCL or SDA pin respectively. Do not leave this pin open. See 1.5.1 **Slave Address** for detail.
5	5	VCC	Power supply input pin, using 0.1uF low ESR ceramic capacitor to ground
6	6	SDA	Digital interface data input or output pin, need a pull-up resistor to VCC.
		Exposed Thermal PAD (bottom side)	Exposed thermal pad (bottom side) is short to GND pin inside the chip.

Function Block

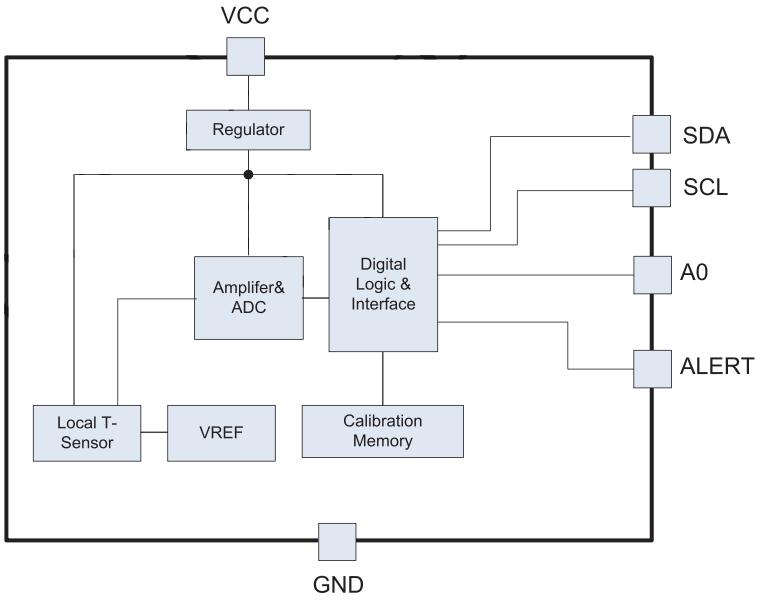
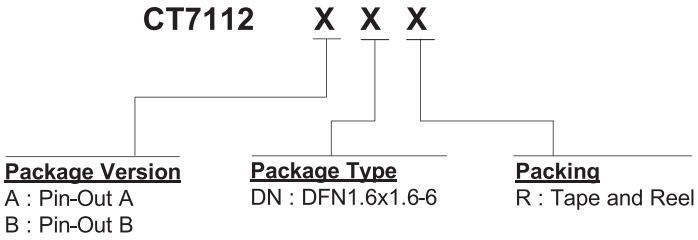


Figure 2. CT7112 function block

Ordering Information



Order PN	Accuracy	Green[1]	Package	Marking ID[2]	Packing	MPQ	Operation Temperature
CT7112ADNR	±0.5°C	Halogen free	DFN1.6x1.6-6	AG TWWA	Tape & Reel	3000	-40°C~+125°C
CT7112BDNR	±0.5°C	Halogen free	DFN1.6x1.6-6	AH YWWA	Tape & Reel	3000	-40°C~+125°C

Notes

1. Based on ROHS Y2012 spec, Halogen free covers lead free. So most package types Sensylink offers only states halogen free, instead of lead free.

2. Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.

1) Generally, date code is represented by 3 numbers. The number stands for year and work week information. e.g. 501stands for the first work week of year 2015;621 stands for the 21st work week of year 2016.

2) Right after the date code information, the next 2-3 numbers or letters are specified to stands for supplier or production location information.

3) For very small outline package, there's 4 digits to stands for product information and date code, first 2 digits represent product code, and the other 2 digits stands for work week

Absolute Maximum Ratings (Note3)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} to GND	-0.3 to 5.5	V
SDA, SCL, A0 Voltage	$V_{SDA}/V_{SCL}/V_{A0}$to GND	-0.3 to 5.5	V
ALERT Voltage	V_{ALERT} to GND	-0.3 to 5.5	V
Operation junction temperature	T_J	-50 to 125	ºC
Storage temperature Range	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260	ºC
ESD MM	ESD_{MM}	400	V
ESD HBM	ESD_{HBM}	4000	V
ESD CDM	ESD_{CDM}	1000	V

Note3

1. *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.*
2. *Using 2oz dual layer (Top, Bottom) FR4 PCB with 4x4 mm^2 cooper as thermal PAD*

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	1.7~ 5.5	V
Ambient Operation Temperature Range	T_A	-40~+125	°C

Electrical Characteristics (Note4)

Test Conditions: C_{IN} = 0.1uF, V_{CC} = 3.3V, T_A=-40 to 125°Cunless otherwise specified. All limits are 100% tested at T_A=25°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		1.7		5.5	V
Temperature Accuracy	T_{AC}	T_A = 0 to 50°C, VCC=3.3V	-0.5		0.5	°C
		T_A = -20 to 85°C, VCC=1.7-5.0V	-1.5		1.5	°C
		T_A = -40 to 125°C, VCC=3.3V	-1		1	°C
		T_A = -40 to 125°C, VCC=1.7-5.0V	-2.5		2.5	°C
Temperature Resolution				0.0625		°C
Average Operating Current	I_{AOC}	1.0 con/s		3.0	4.5	uA
Shutdown Current	$I_{SHUTDOWN}$	Enable STB bit, force SDA/SCL to VCC or GND		1.5	3.0	uA
Open Drain Output Voltage	V_{OL}	ALERT pin, sink 5mA			0.5	V
Open Drain Leakage	I_{ODL}	ALERT pin	-1.0		1.0	uA
Conversion time	t_{CON}	From active to finish completely		30		ms
Digital Interface						
Logic Input Capacitance	C_{IL}	SDA, SCL pin		3.0		pF
Logic Input High Voltage	V_{IH}	SDA, SCL pin	0.7*VCC		VCC+0.3	V
Logic Input Low Voltage	V_{IL}	SDA, SCL pin	-0.3		0.3*VCC	V
Logic Input Current	I_{INL}	SDA, SCL pin	-1.0		1.0	uA
Logic Output Sink Current	I_{OLS}	SDA, ALERT pin, forced 0.2V		5.0		mA
SCL frequency	f_{CLK}	Fast Mode	1		400	kHz
		High Speed Mode	0.001		3	MHz
Timeout of detecting clock low period time	t_{TOUT}	SMBus Communication		30		ms
Clock low period time	t_{LOW}	Fast Mode	1300			ns
		High Speed Mode	210			ns
Clock high period time	t_{HIGH}	Fast Mode	600			ns
		High Speed Mode	60			ns
Bus free time	t_{BUF}	Between Stop and Start condition	1200			ns
Hold time after Start condition	$t_{HD:STA}$	Fast Mode	600			ns
		High Speed Mode	160			ns
Repeated Start condition setup time	$t_{SU:STA}$	Fast Mode	600			ns
		High Speed Mode	160			ns
Stop condition setup time	$t_{SU:STO}$	Fast Mode	600			ns
		High Speed Mode	160			ns
Data Hold time	$t_{HD:DAT}$	Fast Mode	100			ns
		High Speed Mode	25			ns
Data Setup time	$t_{SU:DAT}$	Fast Mode	100			ns
		High Speed Mode	25			ns
Clock/Data fall time	t_F	Fast Mode			300	ns
		High Speed Mode			40	ns
Clock/Data rise time	t_R	Fast Mode			300	ns
		High Speed Mode			40	ns

Note 4:

1. *All devices are 100% production tested at TA = +25°C; All specifications over full temperature range is guaranteed by design, not production tested.*
2. *The chip can work at VCC = 1.6V, under this condition, the temperature accuracy deteriorates to ±2.5°C from ±1.0°C (at VCC = 3.3V) over full temperature, -40°C to 125°C.*

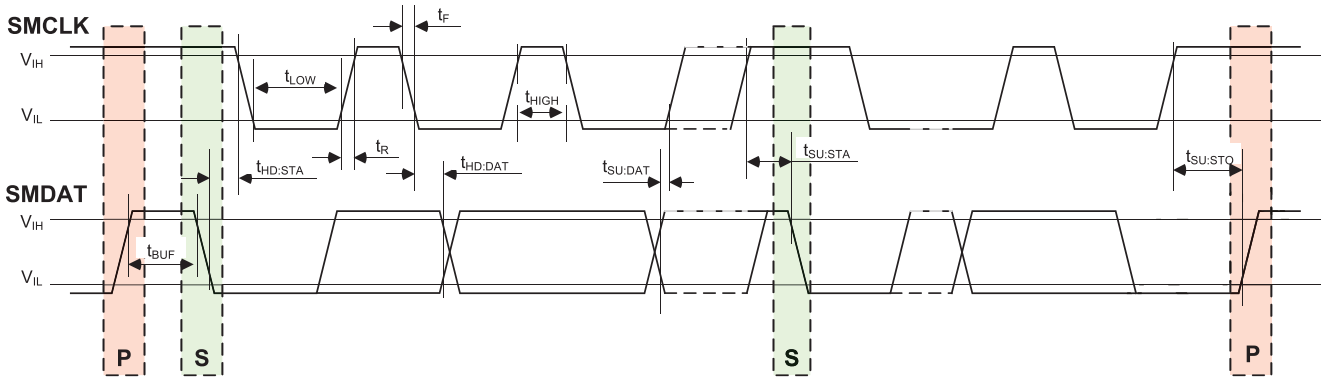


Figure 3. SMBus/I^{2}C Timing Diagram

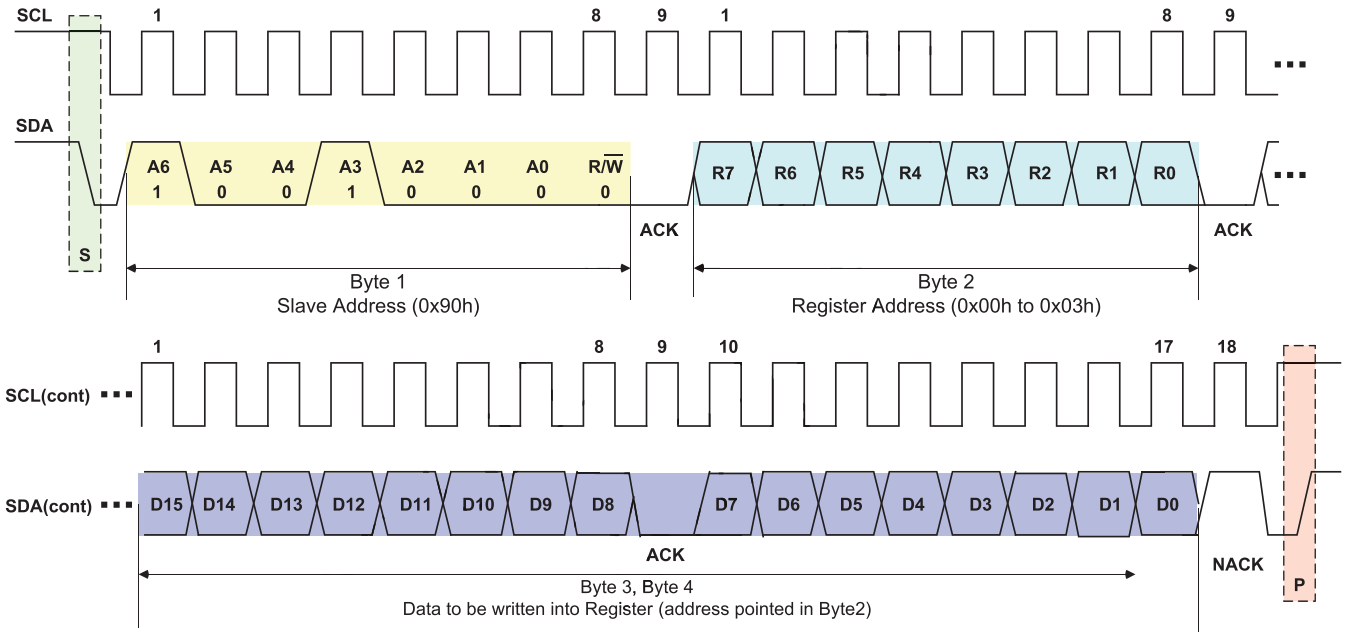


Figure 4. SMBus/I^{2}C Write Word (2-Bytes) Timing Diagram

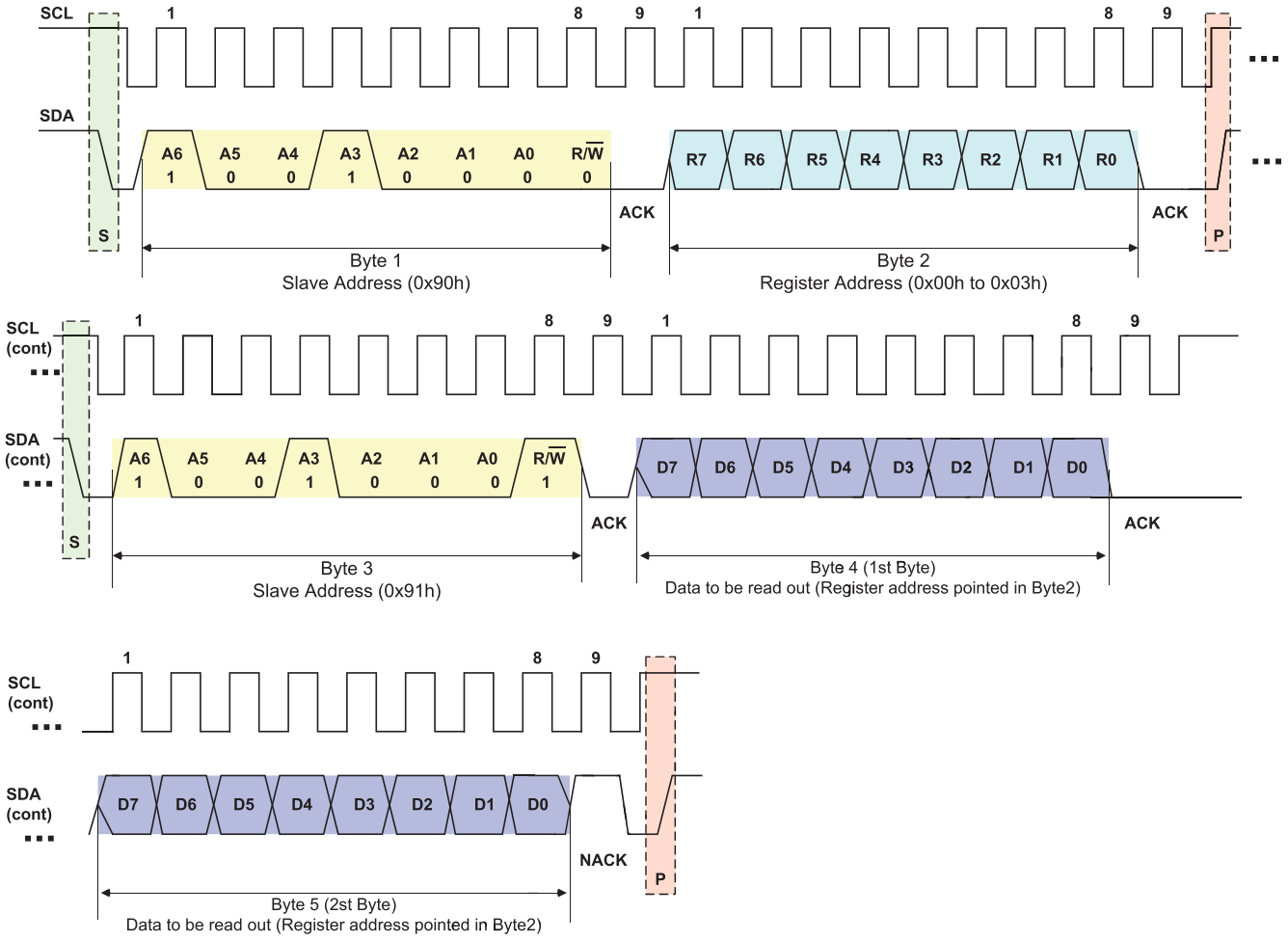


Figure 5. SMBus/I^{2}C Read Word (2-Bytes) Timing Diagram

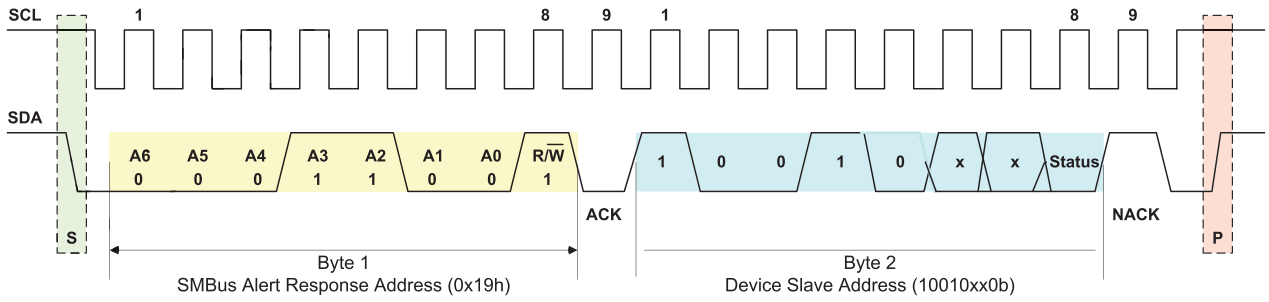


Figure 6. SMBus ALERT Response Diagram

Characteristics (VCC=3.3V/5.0V)

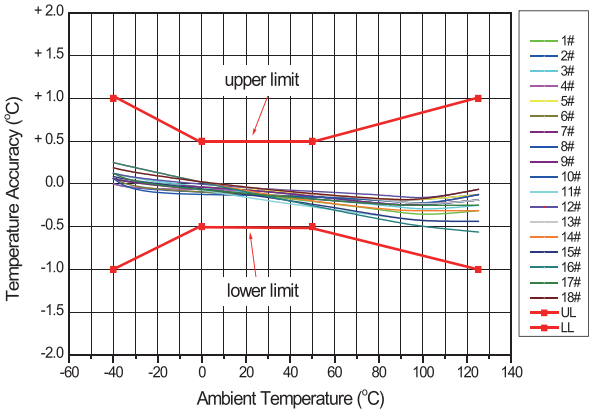


Figure 7. Temperature Accuracy vs. Temperature

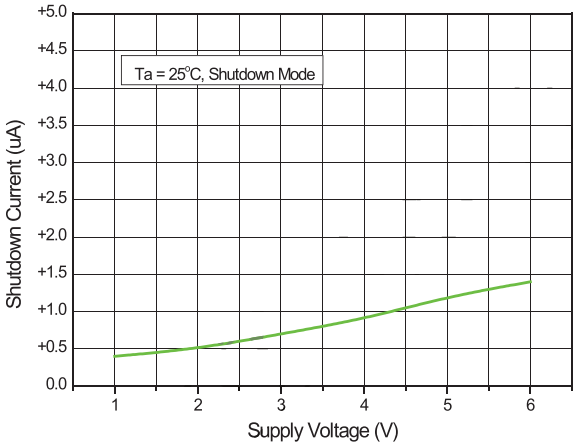


Figure 9. Shutdown Current vs. Supply Voltage

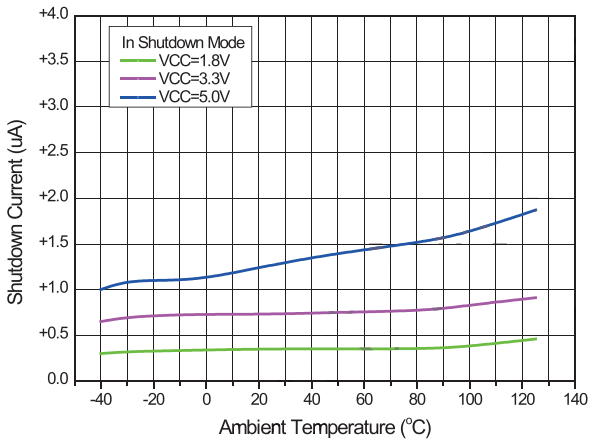


Figure 8. Shutdown Current vs. Temperature

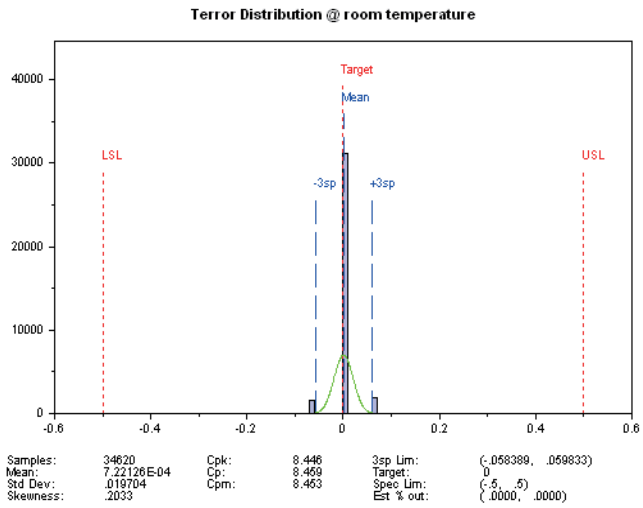


Figure 10. Temperature Error Distribution

1 Function Descriptions

The chip can sense temperature and convert it into digital data by a 12-bit ADC. Also the chip supports programmable high-/low-limit temperature settings. If the measured temperature meets or exceeds the high-limit temperature, ALERT pin will be asserted (be set low or high, depending on POL bit of configuration register).Once the measured temperature goes below the low-limit temperature (programmable by user), ALERT pin will be released.

1.1 Digital Output of Temperature Data

The temperature measurement data is stored in Read Only temperature register. The temperature register is in 12-bit binary format (set EM bit as 0) or 13-bit binary format (set EM bit as 1) with 2-Bytes. This 2-Bytes Temperature data must be read at the same time in each reading cycle, 1st-Byte is MSB followed by 2nd-Byte, the LSB. The relationship between Temperature data in Celsius degree and binary data is shown as below tables.

Table 1. 12-bit Temperature Data (EM bit = 0)

Temperature (°C)	12-bit Digital Output (HEX)	12-bit Digital Output (BIN)
+128	0x7FF0	0 1 1 1, 1 1 1 1, 1 1 1 1 (0 0 0 0)
+127.9375	0x7FF0	0 1 1 1, 1 1 1 1, 1 1 1 1 (0 0 0 0)
+100	0x6400	0 1 1 0, 0 1 0 0, 0 0 0 0 (0 0 0 0)
+25	0x1900	0 0 0 1, 1 0 0 1, 0 0 0 0 (0 0 0 0)
+0.25	0x0040	0 0 0 0, 0 0 0 0, 0 1 0 0 (0 0 0 0)
0	0x0000	0 0 0 0, 0 0 0 0, 0 0 0 0 (0 0 0 0)
-0.0625	0xFFF0	1 1 1 1, 1 1 1 1, 1 1 1 1 (0 0 0 0)
-0.25	0xFFC0	1 1 1 1, 1 1 1 1, 1 1 0 0 (0 0 0 0)
-25	0xE700	1 1 1 0, 0 1 1 1, 0 0 0 0 (0 0 0 0)

Table 2. 13-bit Temperature Data (EM bit = 1)

Temperature (°C)	13-bit Digital Output (HEX)	8-bit Digital Output (BIN) (MSB) 1st Byte	5-bit Digital Output (BIN) (LSB) 2nd Byte
+150	0x4B01	0 1 0 0, 1 0 1 1	0 0 0 0, 0 (0 0 1)
+128	0x4001	0 1 0 0, 0 0 0 0	0 0 0 0, 0 (0 0 1)
+127.9375	0x3FF9	0 0 1 1, 1 1 1 1	1 1 1 1, 1 (0 0 1)
+100	0x3201	0 0 1 1, 0 0 1 0	0 0 0 0, 0 (0 0 1)
+25	0x0C81	0 0 0 0, 1 1 0 0	1 0 0 0, 0 (0 0 1)
+0.25	0x0021	0 0 0 0, 0 0 0 0	0 0 1 0, 0 (0 0 1)
0	0x0001	0 0 0 0, 0 0 0 0	0 0 0 0, 0 (0 0 1)
-0.0625	0xFFF9	1 1 1 1, 1 1 1 1	1 1 1 1, 1 (0 0 1)
-0.25	0xFFE1	1 1 1 1, 1 1 1 1	1 1 1 0, 0 (0 0 1)
-25	0xF381	1 1 1 1, 0 0 1 1	1 0 0 0, 0 (0 0 1)

1.2 Temperature Higher than 128°C

When temperature is higher than 128°C, it can be expressed in binary register data by setting EM bit as 1, shown as above Table 2.In extended format, the resolution of AD converter does not change, but sign bit is added. For example, 12-bit format for 100°C is 0x6400, in which 0x64 is from 1st Byte, and 0x00 is from 2nd Byte. 13-bit format for 100°C is 0x3201, in which 0x32 is from 1st Byte, and 0x01 is from 2nd Byte. The default for EM bit is 0 after Power-on reset.

1.3 Register Map

The chip has 4 registers, and there are 2 bytes (1st Byte and 2nd Byte) for each resister, total 16 bits for each register, shown as below table.

Table 3. Register Map

Register Address	Register Name	Attribution	Default Data	BIT							
				7	6	5	4	3	2	1	0
0x00	Temp_MSB (1st Byte)	R/O	N/A	Temp_Data[11:4]							
	Temp_LSB (2nd Byte)	R/O	N/A	Temp_Data[3:0]							
0x01	Config_MSB (1st Byte)	R/W	0x60	OS	1	1	F1	F0	POL	ALTM	SD
	Config_LSB (2nd Byte)	R/W	0xA0	CR1	CR0	AL	EM	0	0	0	0
0x02	Low_Temp_Set_MSB (1st Byte)	R/W	0x4B	Low_Temp_Setup_Data[11:4]							
	Low_Temp_Set_LSB (2nd Byte)	R/W	0x00	Low_Temp_Setup_Data[3:0]							
0x03	High_Temp_Set_MSB (1st Byte)	R/W	0x50	High_Temp_Setup_Data[11:4]							
	High_Temp_Set_LSB (2nd Byte)	R/W	0x00	High_Temp_Setup_Data[3:0]							

1.4 Register Description

1.4.1 Temp_Data, Temperature Data

Register Address: 0x00

Register Attribution: Read only

Default Data: N/A

BIT (1st Byte)	7	6	5	4	3	2	1	0
Name: Temp_MSB (1st Byte)	Temp_Data[11:4]							
Temperature Data (°C) [12-bit]	SIGN	64	32	16	8	4	2	1
12-bit format	T11	T10	T9	T8	T7	T6	T5	T4
Temperature Data (°C) [13-bit]	(SIGN)	(128)	(64)	(32)	(16)	(8)	(4)	(2)
13-bit format	(T12)	(T11)	(T10)	(T9)	(T8)	(T7)	(T6)	(T5)

BIT (2nd Byte)	7	6	5	4	3	2	1	0
Name: Temp_LSB (2ndByte)	Temp_Data[3:0]							
Temperature Data (°C) [12-bit]	0.5	0.25	0.125	0.0625	0	0	0	0
12-bit format	T3	T2	T1	T0	0	0	0	0
Temperature Data (°C) [13-bit]	(1)	(0.5)	(0.25)	(0.125)	(0.0625)	0	0	(1)
13-bit format	(T4)	(T3)	(T2)	(T1)	(T0)	(0)	(0)	(1)

1.4.2 Config, Configuration Setup register

Register Address: 0x01

Register Attribution: Read/Write

Default Data: 0x60 (1st Byte) 0xA0(2nd Byte) after POR. If user used only 1-Byte, it is ok to read/write 1-Byte command via digital interface; the 1st Byte (MSB) will be accessed.

BIT	7	6	5	4	3	2	1	0
1st Byte	OS	Reserved		F1	F0	POL	ALTM	SD
	0	1	1	0	0	0	0	0
2nd Byte	CR1	CR0	AL	EM	Reserved			
	1	0	1	0	0	0	0	0

OS, One shot Conversion bit

When the device is in shutdown mode, setting this bit as '1'will trigger a single temperature conversion. During the conversion, the OS bit reads as '0'. The device returns to shutdown mode once it completes the single conversion. This feature is used for reducing power consumption when continuous temperature monitoring is not necessary.

CR1, CR0, Conversion Rate Selection bits

These 2 bits allow user to setup different conversion rate for temperature. The default is 10 after POR, meaning the conversion rate is 4Hz, i.e. 4 times conversion every second.

CR1	CR0	Conversion Rate / Conversion Time
0	0	0.25Hz / 4.0s
0	1	1.0Hz / 1.0s
1	0	4.0Hz /0.25s (default)
1	1	8Hz / 0.125s

F1, F0, Fault Queue bits

These 2 bits are used to setup the number of fault conditions to trigger alert. The default is 00 after POR, which means one time fault. This feature is used to prevent a false alert, which is immune to certain noise in application.

F1	F0	Fault Queue Number
0	0	1 (default)
0	1	2
1	0	4
1	1	6

POL, Alert Output Polarity bit

This bit allows user to setup the polarity of ALERT pin for output. The default is 0 after POR, meaning ALERT pin is active low. When POL bit is setup '1', the ALERT pin becomes active high and the state of ALERT pin is inverted.

ALTM, Alert Operation Mode bit

This bit allows user to select ALERT pin operation mode: Comparator Mode or Interrupt Mode. The default is 0 to select Comparator Mode. For detail information, see ALERT output section.

SD, Shutdown bit

This bit allows user to shutdown the chip and to make the chip enter into standby mode once writing'1'. The default value is '0', which sets the chip to be in Normal working mode. During shutdown mode, the temperature data is kept as those of last time, no anymore update, and all function blocks are turned-off except interface. Set this bit as '0' can allow the chip be out of shutdown mode. In shutdown mode, the operation current is about1.5uA in typical.

EM, Extended Mode bit

This bit allows user to select 12-bit (EM = 0) or 13-bit (EM = 1) temperature data. When EM bit is set as '1', the temperature resolution is still 0.0625°C resolution. However the expression range is extended from -255°C to +255°C.

AL, Alert Status bit

The AL bit indicates the Alert status with read-only attribution. In addition, this bit is always read as the inversion of POL bit. When the POL bit equals 0, the AL bit reads as 1 until the measured temperature equals or exceeds Temperature (HIGH) for the programmed number of consecutive faults, causing the AL bit to read as 0. The AL bit continues to read as 0 until the temperature falls below Temperature (LOW) for the programmed number of consecutive faults, when it again reads as 1. Vice versa, when the POL bit is '1', the AL bit reads as 0 until the temperature equals or exceeds Temperature (HIGH). And the AL bit is set as 0 again once the temperature falls below Temperature (LOW). The status of the TM bit does not affect the status of the AL bit.

1.4.3 Low_Temp_Set, Setup Low Temperature Limitation register

Register Address: 0x02

Register Attribution: Read/Write

Default Data: 0x4B (1st Byte) 0x00 (2nd Byte) after POR.

BIT	BIT	7	6	5	4	3	2	1	0
1st Byte	12-bit	L11	L10	L9	L8	L7	L6	L5	L4
	13-bit	(L12)	(L11)	(L10)	(L9)	(L8)	(L7)	(L6)	(L5)
	Default	0	1	0	0	1	0	1	1
2nd Byte	12-bit	L3	L2	L1	L0	0	0	0	0
	13-bit	(L4)	(L3)	(L2)	(L1)	(L0)	(0)	(0)	(0)
	Default	0	0	0	0	0	0	0	0

The high-/low- limit temperatures are determined by High_Temp_Set register [0x03] and Low_Temp_Set register [0x02] with same format as Temp_Data register [0x00], which could be in 12-bit or 13-bit binary format. The chip compares Temp_Data [0x00] register and High_Temp_Set register [0x03]/Low_Temp_Set register [0x02] in each conversion cycle, which will affect ALT pin output. The default value is 0x4B00 with 12-bit binary format, which means 75°C. For other low-limit temperature data chip, please contact our sales.

1.4.4 High_Temp_Set, Setup High Temperature Limitation register

Register Address: 0x03

Register Attribution: Read/Write

Default Data: 0x50 (1st Byte) 0x00 (2nd Byte) after POR.

BIT	BIT	7	6	5	4	3	2	1	0
1st Byte	12-bit	H11	H10	H9	H8	H7	H6	H5	H4
	13-bit	(H12)	(H11)	(H10)	(H9)	(H8)	(H7)	(H6)	(H5)
	Default	0	1	0	0	0	0	0	0
2nd Byte	12-bit	H3	H2	H1	H0	0	0	0	0
	13-bit	(H4)	(H3)	(H2)	(H1)	(H0)	(0)	(0)	(0)
	Default	0	0	0	0	0	0	0	0

The high-/low- limit temperature is determined by High_Temp_Set register [0x03] and Low_Temp_Set register [0x02] with same format as Temp_Data register [0x00], which could be in 12-bit or 13-bit binary format. The chip compares Temp_Data [0x00] register and High_Temp_Set register [0x03]/Low_Temp_Set register [0x02] in each conversion cycle, which will affect ALT pin output. The default value is 0x5000 with 12-bit binary format, which means 80°C. For other low-limit temperature data chip, please contact our sales.

1.5 SMBus Digital Interface

1.5.1 Slave Address

The SMBus or I²C slave address of this device can be configured 4 different add ressesby setting [A0] pin. See below table for detail. Which permit connecting total 4 devices in one SMBus.

No.	A0	R/W	Slave Address in Hex [R/W]
1	GND	1/0	0x91/0x90
2	VCC	1/0	0x93/0x92
3	SDA	1/0	0x95/0x94
4	SCL	1/0	0x97/0x96

1.5.2 Timeout

The chip supports SMBus timeout. If the data (SDA PIN)or clock (SCL PIN) is held low for longer than 30ms (Typ.), the chip will reset its SMBus protocol and be ready for a new transmission.

1.5.3 SMBus Protocol

The chip supports four standard SMBus protocols Send Byte, Read Byte, Write Byte and Receive Byte, shown as below tables.

Write Byte

S	Slave Add	R/W	ACK	Reg Add	ACK	Reg Data	ACK	P
		0	0	0x00 to 0x03	0	XXh	0	

Read Byte

S	Slave Add	R/W	ACK	Reg Add	ACK	S	Slave Add	R/W	ACK	Reg Data	NACK	P
		0	0	0x00 to 0x03	0			1	0	XXh[1]	1	

Send Byte

S	Slave Add	R/W	ACK	Reg Add	ACK	P
		0	0	XXh	0	

Receive Byte

S	Slave Add	R/W	ACK	Reg Add	NACK	P
		1	0	XXh	1	

Here S means SMBus Start to communication with master, P, means communication STOP.

Slave Add, means the chip's slave address.

Reg Add, means pointed Register Address.

Reg Data, means data to be written into register or read from register.

For this chip, each register includes 2 Bytes, so generally reading or writing operation is based on 1 Word (2-Bytes).Also it is permitted to read 1 byte for read/write, then the 1st byte will be accessed in first.

1.5.4 Compatible with I²C

The chip is compatible with both SMBus and I²C. And the major difference between SMBus and I²C are shown as below. For more information, refer to SMBus specification v2.0 and I²C specification v2.1.

1). This chip supports I²C fast mode (400kHz) and standard mode (100kHz), which can cover SMBus maximum frequency 100kHz.

2). For SMBus protocol, the minimum frequency is 10kHz. There is no such limitation for I²C.

3).ARA (Alert Response Address) general call is only valid interrupt in SMBus, not valid in I²C.

1.5.5 General Call

The CT7112 device responds to a two-wire general-call address (0000 000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000 0110, the CT7112 internal registers are reset to power-up values.

1.5.6 High-Speed (Hs) Mode

If I^2C/SMBus needs to run at frequencies above 400 kHz, the master device must issue an Hs-mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. After the Hs-mode master code has been issued, the master transmits a slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the CT7112 device will return back to fast-mode operation.

1.6 ALERT Output

ALERT pin is output with open drain which can be set active low or active high by setting POL bit. And it is triggered when the measured temperature equals or exceeds the limitation temperature setup in the registers of High_Temp_Set / Low_Temp_Set. There are two types of ALERT output mode: comparator mode and interrupt mode.

1.6.1 Comparator mode (ALTM=0)

Below Figure shows the mechanism of the ALERT output in comparator mode. In this mode, the ALERT pin will becomes active if the monitored temperature equals or exceeds the value setup in High_Temp_Set [0x03] register for a consecutive number of faults according to setup by F1 and F0 bits. The ALERT pin keeps active until the temperature falls below the value setup in Low_Temp_Set [0x02] register.

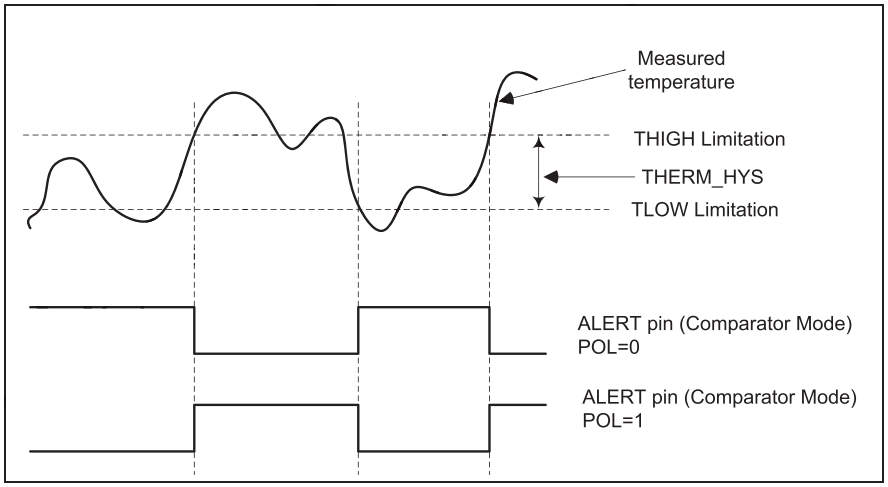


Figure 11 ALERT pin output in comparator mode

1.6.2 Interrupt mode (ALTM=1)

Below Figure shows the mechanism of the ALERT pin output interrupt mode. In this mode, the ALERT pin becomes active when the temperature equals or exceeds the value setup in High_Temp_Set [0x03] register for a consecutive number of faults according to setup by F1 and F0 bits. The ALERT pin keeps active until a read operation of any register happens or the chip responds to SMBus Alert Response Address (ARA) successfully. When ALERT pin is cleared, it will become active again only when the temperature falls below the value setup in Low_Temp_Set [0x02] register, and keeps active until being cleared by reading register or responding to SMBus ARA.ALERT pin is also cleared by setting the chip in shutdown mode.

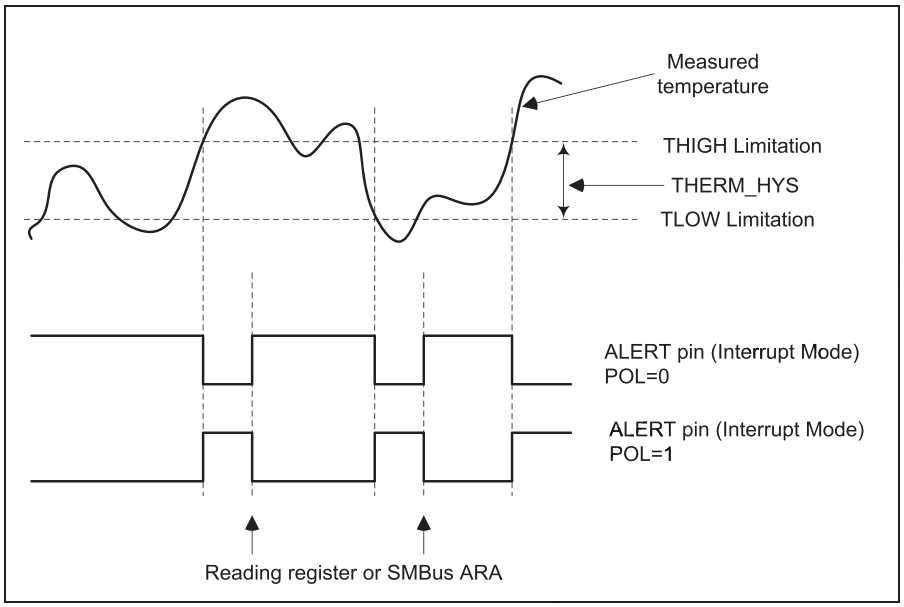


Figure 12 ALERT pin output in interrupt mode

1.6.3 SMBus Alert Response Address (ARA)

The chip supports the SMBus alert function feature. When the chip operates in interrupt mode (ALTM=1), it can be connected as SMBus alert signal, used as a processer interrupt or as SMBus ALERT. When the master detects that the ALERT pin is asserted, it will send Alert Response Address (ARA) to general address (0001, 1001b). All devices with active interrupts will respond with client address. If the alert pin is active, the device acknowledges the SMBus command by returning the slave address from SDA line. If more devices than one on the bus respond SMBus ARA, arbitration during the slave address portion of SMBus ARA determines which device clears the alert trigger. The device with the highest priority (lowest address) wins the arbitration. If the chip wins the arbitration, ALERT pin is released after completion of SMBus ARA command. If the chip loses the arbitration, it will keep ALERT pin active. See System Management Bus (SMBus) Specification for more detail.

Below Figure shows the mechanism of the ALERT output SMBus Alert mode.

S	Slave Add	R/W	ACK	Reg Add	ACK	P
	0001,100	1	0	1001, 0xxS	1	

Here Reg Add presented the chip real actual address setup by user. S bit means trigger ALTER or not. if S bit is 0, means no ALERT trigger, or means ALERT is trigged.

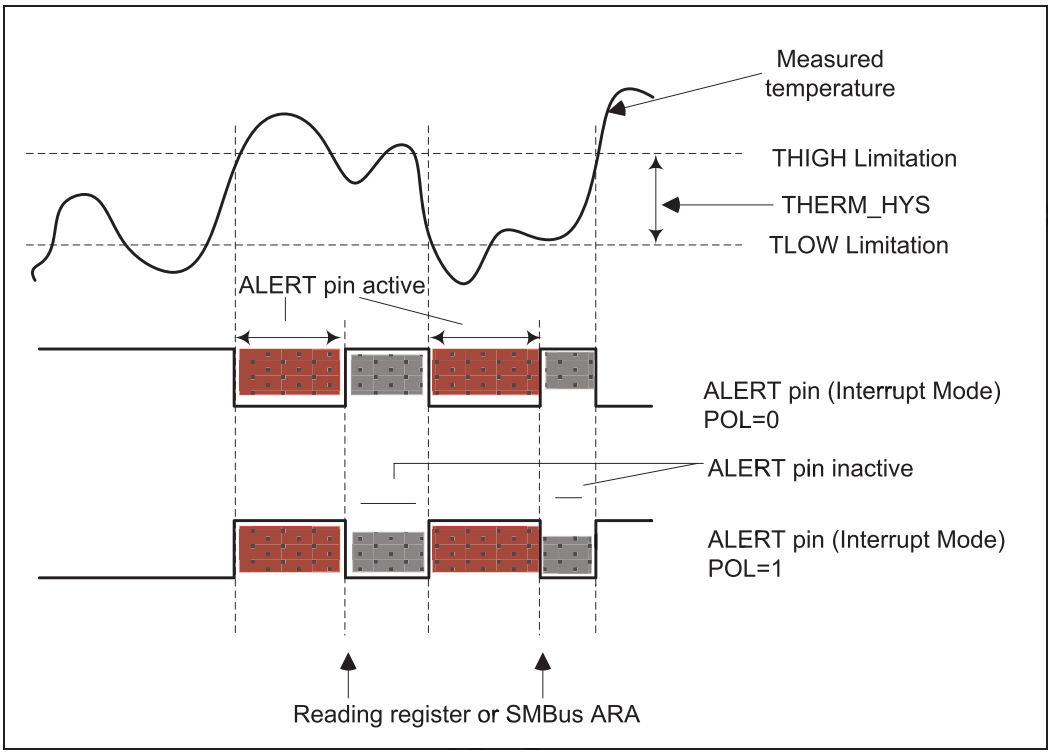


Figure 13 ALERT pin in SMBus Alert Response(ARA)

2 Application Information

2.1 How to Improve Temperature Accuracy

The temperature measurement of the chip is based on semiconductor physics principle --Forward voltage of diode is a function of temperature. The formula is shown as below.

$$V_F = \frac{kT}{q} \ln\left(\frac{I_F}{I_S}\right)$$

Here,

V_F -- forward voltage

I_F -- forward current

I_S -- reverse saturation current

k -- Boltzmann constant

T -- Temperature in K

q -- Electric charge constant

To cover wide temperature range, i.e. -40°C to 125°C, a very small voltage variation is corresponding to every degree C temperature change. Sensylink has applied many ways to improve measurement accuracy in chip circuits design, such as compensation, trimming etc. In real system design, however, some factors that can increase measurement error need to be considered. Most issues that usually occur are high-lighted as below.

2.2 Noise between VCC and GND

It is very necessary to place a low ESR ceramic cap (C_{IN}) between VCC and GND pin to filter digital noise, although suppression noise circuit has been built inside the chip. This filter cap should be placed as close as possible to the chip. The recommended capacitance is 0.1uF.

2.3 PCB Layout

Cautions below are important to improve temperature measurement accuracy in PCB layout design.

2.3.1 Device placement

It is better to place the chip away from any thermal source (e.g. power device in board), high speed digital bus (e.g. memory bus), coil device (e.g. inductors) and wireless antenna (e.g. Bluetooth, WiFi, RF). It is recommended to place the chip close to the remote diode.

2.3.2 Cin, Pull-up resistor

It is better to place Cin as close as possible to VCC and GND pins of the chip. The recommended Cin value is 0.1uF with low ESR ceramic cap although using multi caps, such as 1.0uF plus 0.1uF or 0.01uF, is ok, which can suppress digital noise with different frequency range.

User has to put a pull-up resistor with 4.7k to 10k for SDA and SCL pins respectively. It is ok to use smaller resistors such as 2k-3k in real application, if multi SMBus/I2C devices are used in the same bus.

2.4 Standalone Thermostat

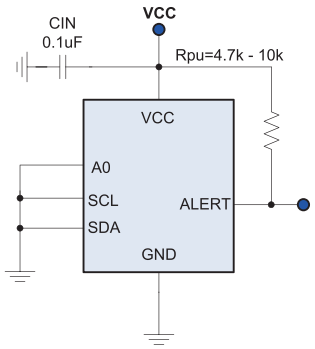
CT7112 can also be used as standalone thermostat shown as below. It does not need external MCU to setup High/Low limitation temperature via SMBus/I2C communication. The trigger temperature and hysteresis temperature can be setup in factory before shipping to customer. For example,

Trigger temperate is 55°C, and

Hysteresis temperature is 5°C.

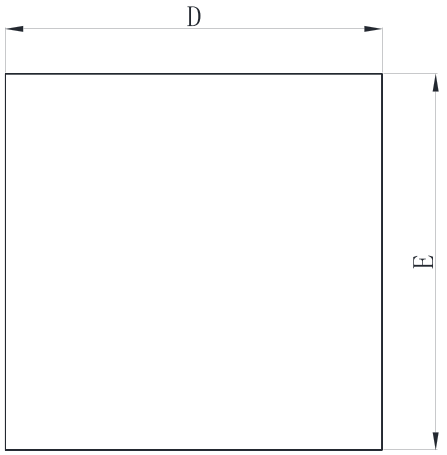
Which means once the chip temperature equals or exceeds 55°C, the ALERT pin will be set low. And once the temperature of the chip drops below 50°C (55 - 5), the ALERT pin will be released, back to high.

Please contact Sensylink sales for specific Trigger, Hysteresis temperature you want.

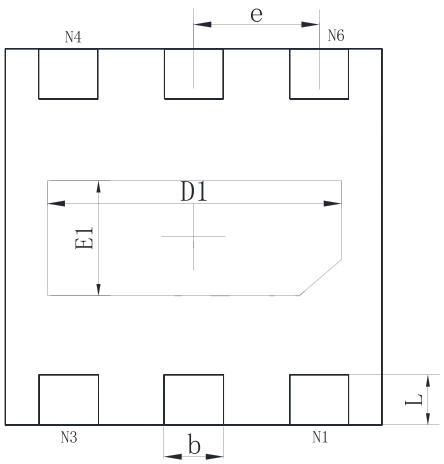


Package Outline Dimensions

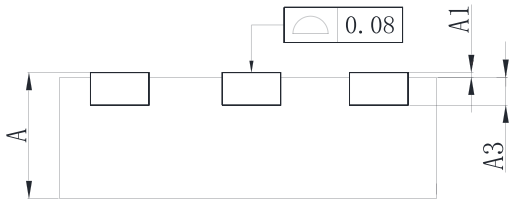
DFN1.6x1.6-6 **Unit (mm)**



Top View



Bottom View

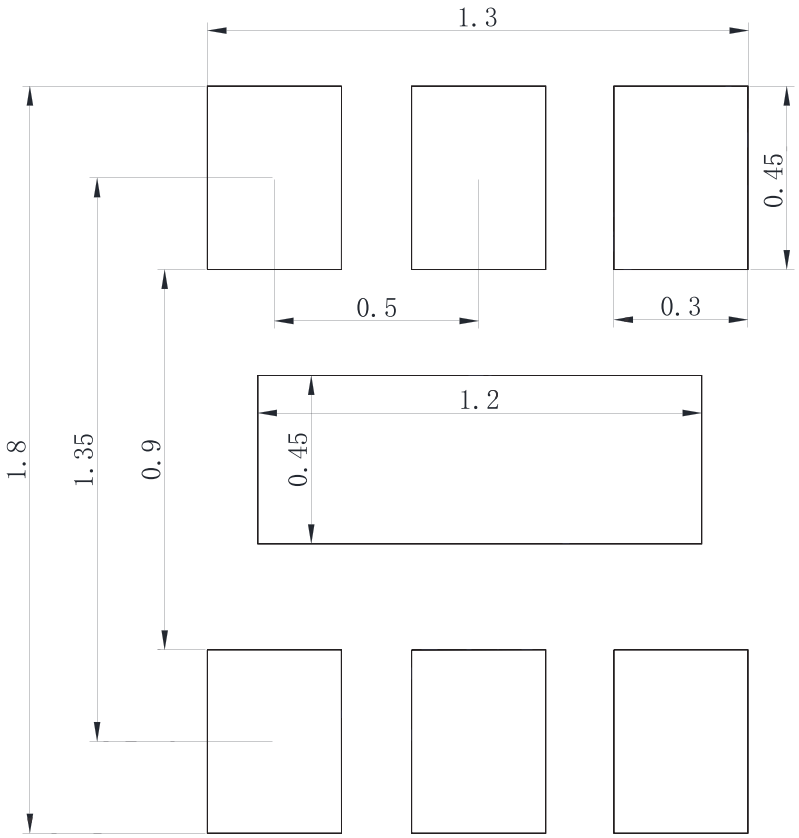


Side View

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF	
D	1.500	1.700	0.059	0.067
E	1.500	1.700	0.059	0.067
D1	1.150	1.250	0.045	0.049
E1	0.400	0.500	0.016	0.020
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP	
L	0.200	0.300	0.008	0.012

Recommend Land Pattern Layout

DFN1.6x1.6-6 **Unit (mm)**



Note:

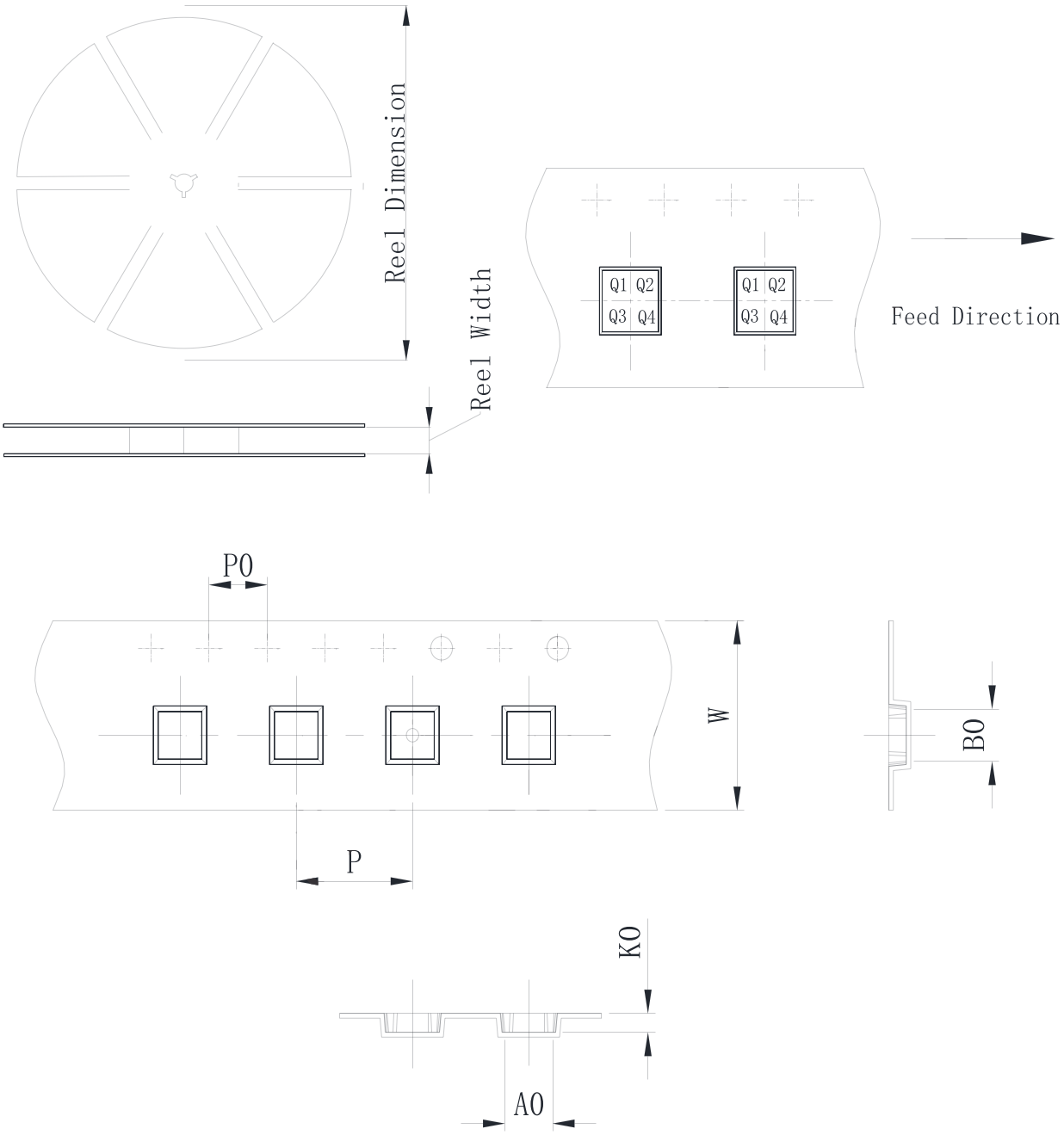
1 All dimensions are in millimeter

2 Recommend tolerance is within ±0.1mm

3 If the thermal pad is not necessary, designer can leave the land pattern area blank

4 Change without notice

Packing information



Package type	Reel size	Reel dimension	Reel width(mm)	A0(mm)	B0(mm)	K0(mm)	P(mm)	P0(mm)	W(mm)	Pin1
DFN1.6x1.6-6	7'	180±3.0	12.8±1.0	1.85±0.1	1.85±0.1	1.0±0.1	4.0±0.1	4.0±0.1	12±0.3	Q2

Revision History

Version	Date	Change Content
Ver1.0	2018/07	Initial the datasheet
Ver1.1	2019/03	Update Electrical Characteristics
Ver1.2	2019/05	Update Characteristics Plots
Ver1.3	2019/07	Add CT7112B part No.
Ver1.4	2019/08	Revised CT7112B pin out.
Ver1.5	2019/11	Update Sensylink Logo
Ver1.6	2020/08	1. Add Packing Information 2. Add EPAD in Pin Description

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