

#### **Description**

The AP85N08BP/T uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

 $V_{DS} = 80V I_{D} = 85A$ 

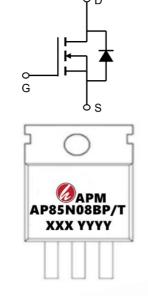
 $R_{DS(ON)} < 8.5 m\Omega \ V_{GS} = 10 V \quad (\ Type: \ 6.5 m\Omega)$ 

#### **Application**

**Battery protection** 

Load switch

Uninterruptible power supply





#### Package Marking and Ordering Information

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Product ID	Pack	Marking	Qty(PCS)	
AP85N08BP	TO-220-3L	AP85N08BP XXX YYYY	1000	
AP85N08BT	TO-263-3L	AP85N08BT XXX YYYY	800	

Absolute Maximum Ratings (T<sub>c</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	80	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID@TC=25°C	Continuous Drain Current, VGS @ 10V	85	А
ID@TC=100°C	Continuous Drain Current, VGS @ 10V	55	А
IDM	Drain Current-Continuous@ Current-Pulsed	300	А
PD@TC=25°C	Maximum Power Dissipation(Tc=25°C)	160	W
EAS	Single pulse avalanche energy	550	mJ
TSTG	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 To 175	°C
RθJA	Thermal Resistance Junction-Ambient	0.94	°C/W
RθJC	Thermal Resistance Junction-Case	63	°C/W



#### **80V N-Channel Enhancement Mode MOSFET**

#### Electrical Characteristics (T₁=25 °C, unless otherwise noted)

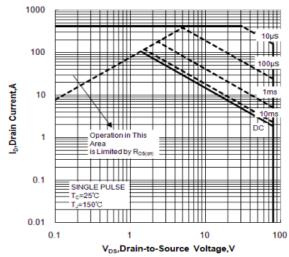
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V(BR)DSS	Drain-source breakdown voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	80	85		V
VGS(th)	Gate threshold voltage	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250uA T <sub>j</sub> =25°C	2.0	3.0	4.0	V
IDSS	Zero gate voltage drain current	V <sub>DS</sub> =80V,V <sub>GS</sub> =0V T <sub>j</sub> =25°C	-		1	μA
IDSS	Zero gate voltage drain current	V <sub>DS</sub> =80V,V <sub>GS</sub> =0V T <sub>j</sub> =125°C		- 5		μΑ
IGSS	Gate-source leakage current	V <sub>GS</sub> =20V,V <sub>DS</sub> =0V	-	-	100	nA
RDS(on)	Drain-source on-state resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =50A,T <sub>j</sub> =25°C	-	6.5	8.5	mΩ
gfs	Transconductance	V <sub>DS</sub> =5V,I <sub>D</sub> =50A	-	80	-	S
Ciss	Input Capacitance		-	2948	-	pF
Coss	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =40V, f=1MHz	-	354	-	pF
Crss	Reverse Transfer Capacitance		-	198	-	pF
Q <sub>G</sub>	Gate Total Charge		-	61	-	nC
Qgs	Gate-Source charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =40V,I <sub>D</sub> =50A	-	13	-	nC
Qgd	Gate-Drain charge		-	24	-	nC
td(on)	Turn-on delay time		-	24	-	ns
t <sub>r</sub>	Rise time	T <sub>j</sub> =25°C, V <sub>GS</sub> =10V, V <sub>DS</sub> =40V,	-	15	-	ns
td(off)	Turn-off delay time	R <sub>L</sub> =3Ω	-	52	-	ns
t <sub>f</sub>	Fall time		-	17	-	ns
Rg	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	-	1.2	-	Ω
VSD	Body Diode Forward Voltage	V <sub>GS</sub> =0V,I <sub>SD</sub> =50A	-	0.9	1.2	V
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	-	40	-	ns
Qrr	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	-	61	-	nC

#### Note:

- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2. The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3. The test cond  $\leq$  300us duty cycle  $\leq$  2%, duty cycle ition is V<sub>DD</sub>=64V<sub>GS</sub>=10V,L=0.1mH,I<sub>AS</sub>=41A
- 4. The power dissipation is limited by 175℃ junction temperature
- 5. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.



### **Typical Characteristics**



160
140
120
120
100
60
40
20
0
25 50 75 100 125 150
Tc,Case Temperature, ©

Figure 1. Maximum Safe Operating Area

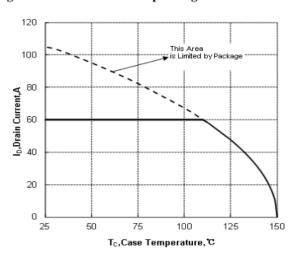


Figure 2. Maximum Power Dissipation vs Case Temperature

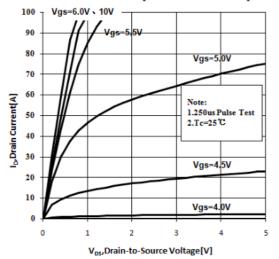


Figure 3. Maximum Continuous Drain Current vs

Figure 4. Typical output Characteristics

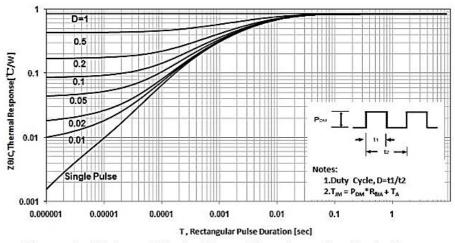


Figure 5 Maximum Effective Thermal Impedance, Junction to Case





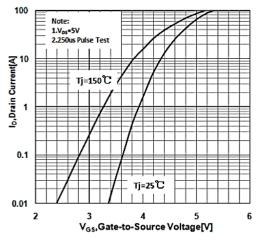


Figure 6 Typical Transfer Characteristics

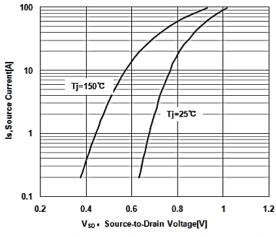


Figure 7 Typical Body Diode Transfer Characteristics

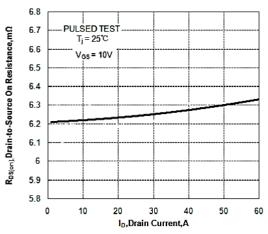


Figure 8. Drain-to-Source On Resistance vs Drain Current

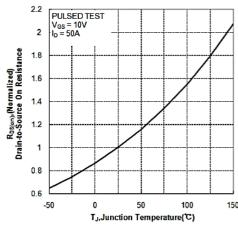


Figure 9. Normalized On Resistance vs Junction Temperature

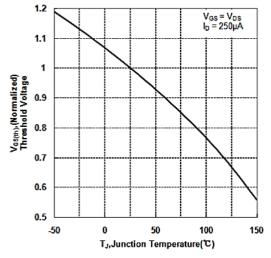


Figure 10. Normalized Threshold Voltage vs Junction Temperature

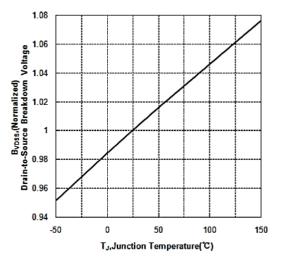
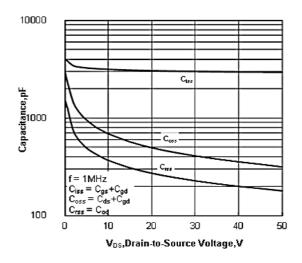


Figure 11. Normalized Breakdown Voltage vs Junction Temperature



## **80V N-Channel Enhancement Mode MOSFET**



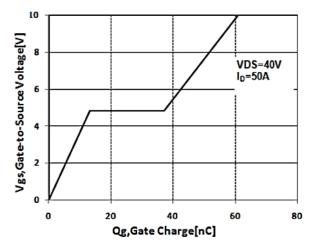
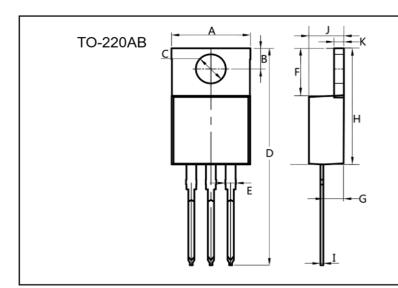


Figure 12. Capacitance Characteristics

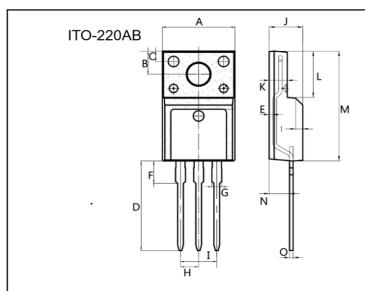
Figure 13 . Typical Gate Charge vs Gate to Source Voltage



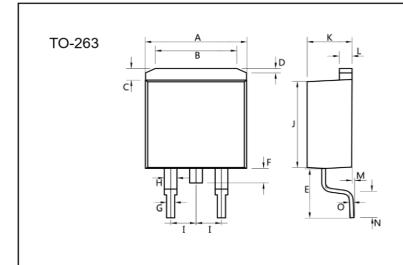




Dim.	Min.	Max.
Α	10.0	10.4
В	2.5	3.0
С	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
Н	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
All Dimensions in millimeter		



Dim.	Min.	Max.	
Α	9.9	10.3	
В	2.9	3.5	
С	1.15	1.45	
D	12.75	13.25	
Е	0.55	0.75	
F	3.1	3.5	
G	1.25	1.45	
Н	Typ 2.54		
I	Typ 5.08		
J	4.55	4.75	
K	2.4	2. 7	
L	6.35	6.75	
М	15.0	16.0	
N	2.75	3.15	
0	0.45	0.60	
All Dimensions in millimeter			



Dim.	Min.	Max.	
Α	10.0	10. 5	
В	7.25	7.75	
С	1.3	1.5	
D	0.55	0.75	
E	5.0	6.0	
F	1.4	1.6	
G	0.75	0.95	
Н	1.15	1.35	
1	Typ 2.54		
1	ТУР	2.01	
J	8.4	8.6	
J	8.4	8.6	
J K	8.4 4.4	8.6 4.6	
J K L	8.4 4.4 1.25	8.6 4.6 1.45	
J K L	8.4 4.4 1.25 0.02	8.6 4.6 1.45 0.1	
J K L M N	8.4 4.4 1.25 0.02 2.4	8.6 4.6 1.45 0.1 2.8 0.45	



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## **80V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2020/10/31	Initial release

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