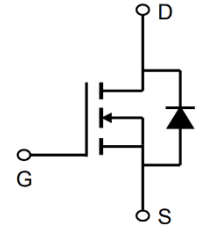


200V N-Channel Enhancement Mode MOSFET

Description

The AP40N20MP is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

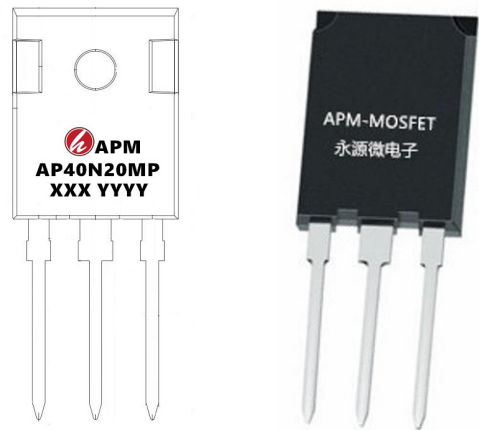
$V_{DS} = 200V, I_D = 40A$

$R_{DS(ON)} < 80m\Omega @ V_{GS} = 10V$

Application

Power amplifier

motor drive



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40N20MP	TO-247-3 Plus	AP40N20MP XXX YYYY	600

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage	200	V
ID	Drain Current -continuous	40	A
IDM	Drain Current -pulse	120	A
VGSS	Gate-Source Voltage	± 30	V
EAS	Single Pulsed Avalanche Energy	588	mJ
IAR	Avalanche Current	40	A
EAR	Repetitive Avalanche Current	15.8	mJ
dv/dt	Peak Diode Recovery dv/dt	5.5	V/ns
PD $T_C = 25^\circ C$	Power Dissipation	158	W
TJ, TSTG	Operating and Storage Temperature Range	$-55 \sim +150$	$^\circ C$
TL	Maximum Lead Temperature for Soldering Purposes	300	$^\circ C$
Rth(j-c)	Thermal Resistance, Junction to Case	0.79	$^\circ C/W$
Rth(j-A)	Thermal Resistance, Junction to Ambient	62.5	$^\circ C/W$

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Electrical Characteristics Diagrams

Symbol	Parameter	Tests conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Voltage	$I_D=250\mu A, V_{GS}=0V$	200	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D=250\mu A$, referenced to 25°C	-	0.19	-	V/°C
$IDSS$	Zero Gate Voltage Drain Current	$V_{DS}=200V, V_{GS}=0V, T_C=25^\circ C$	-	-	1	μA
$IGSSF$	Gate-body leakage current, forward	$V_{DS}=0V, V_{GS}=30V$	-	-	100	nA
$IGSSR$	Gate-body leakage current, reverse	$V_{DS}=0V, V_{GS}=-30V$	-	-	-100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D=250\mu A$	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D=14.0A$	-	60	80	m Ω
g_{fs}	Forward Transconductance	$V_{DS} = 40V, I_D=14.0A$	-	24	-	S
C_{iss}	Input capacitance	$V_{DS}=25V, V_{GS} = 0V, f=1.0MHz$	-	2879	3742	pF
C_{oss}	Output capacitance		-	362	470	pF
C_{rss}	Reverse transfer capacitance		-	81	105	pF
$t_{d(on)}$	Turn-On delay time	$V_{DD}=100V, I_D=28A, R_G=25\Omega, V_{GS}=10V$ (note 4, 5)	-	28	69	ns
t_r	Turn-On rise time		-	251	494	ns
$t_{d(off)}$	Turn-Off delay time		-	309	617	ns
t_f	Turn-Off Fall time		-	220	412	ns
Q_{gi}	Total Gate Charge	$V_{DS} = 160V, I_D=28A$ $V_{GS} = 10V$ (note 4, 5)	-	103	136	nC
Q_{gs}	Gate-Source charge		-	16	-	nC
Q_{gd}	Gate-Drain charge		-	53	-	nC
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	28	A
ISM	Maximum Pulsed Drain-Source Diode Forward Current		-	-	112	A
V_{SD}	Maximum Continuous Drain-Source Diode Forward Current	$V_{GS}=0V, I_S=28A$	-		1.4	V
t_{rr}	Reverse recovery time	$V_{GS}=0V, I_S=28A, di_F/dt=100A/\mu s$ (note 4)		218		ns
Q_{rr}	Reverse recovery charge			1.91		μC

Notes:

- 1: Pulse width limited by maximum junction temperature
- 2: $L=1.5mH, I_{AS}=28A, V_{DD}=50V, R_G=25\Omega$, Starting $T_J=25^\circ C$
- 3: $I_{SD} \leq 28A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ C$
- 4: Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
- 5: Essentially independent of operating temperature

200V N-Channel Enhancement Mode MOSFET

Electrical Characteristics Diagrams

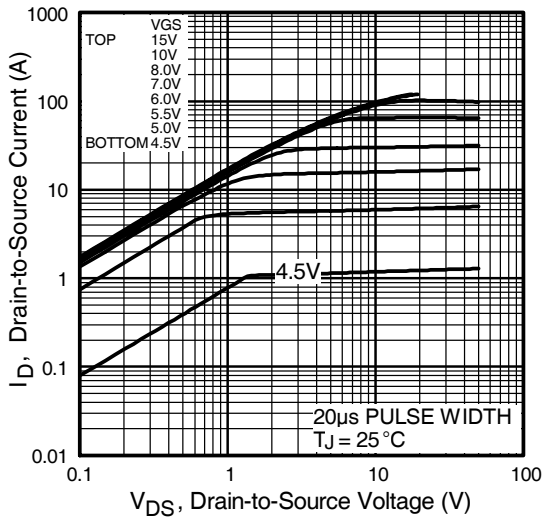


Fig 1. Typical Output Characteristics

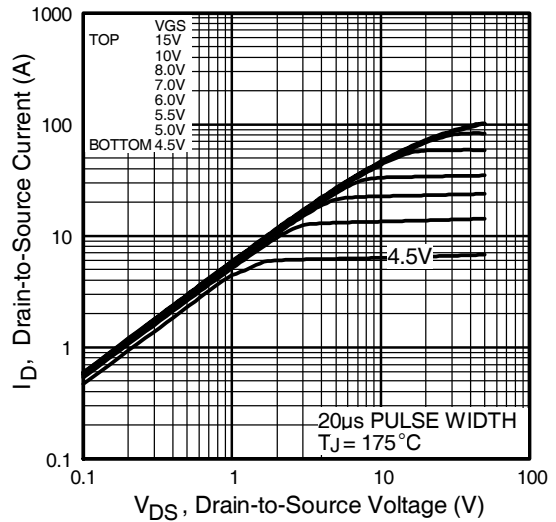


Fig 2. Typical Output Characteristics

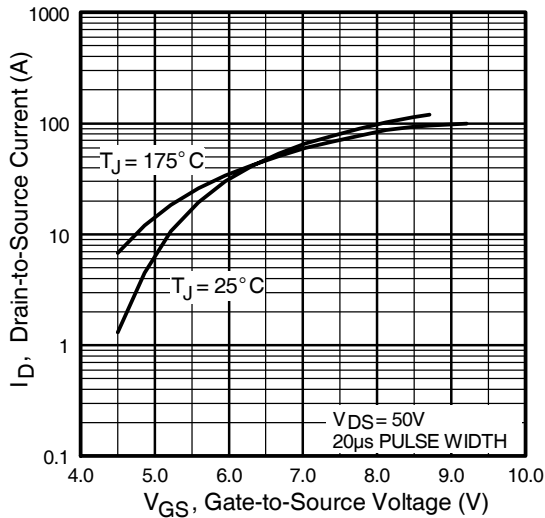


Fig 3. Typical Transfer Characteristics

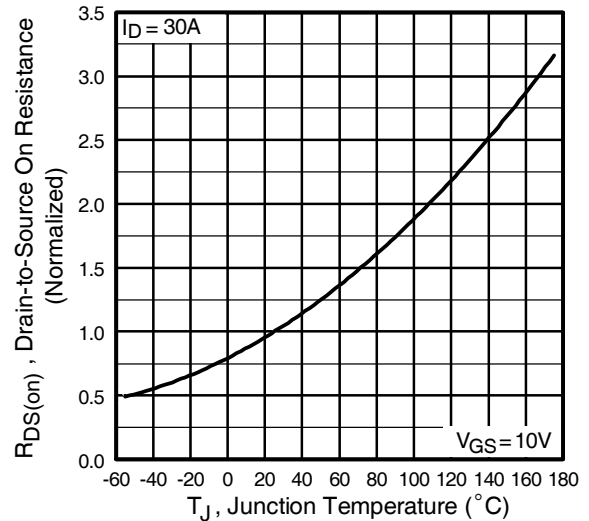


Fig 4. Normalized On-Resistance Vs. Temperature

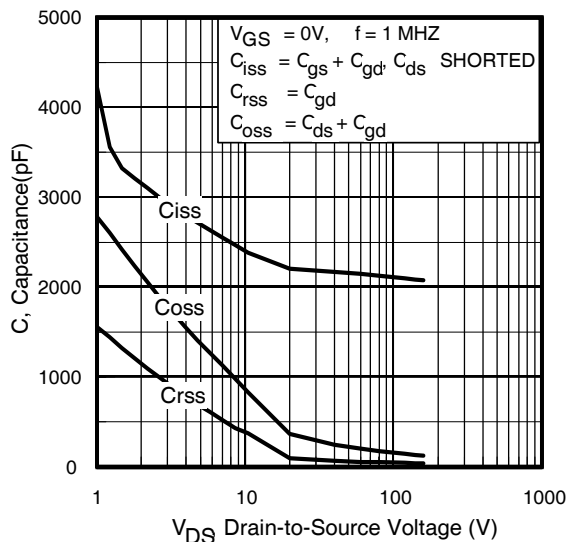


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

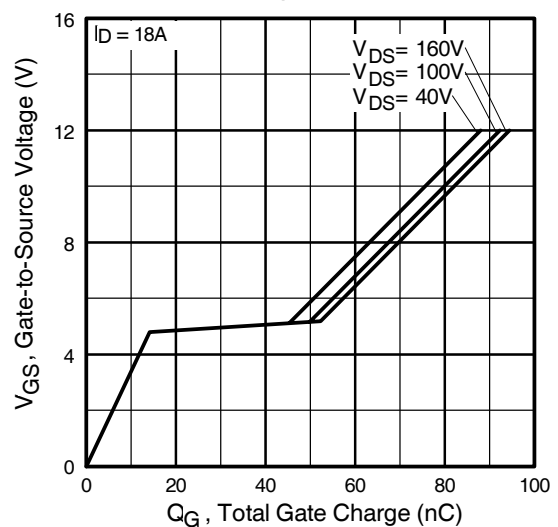


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

200V N-Channel Enhancement Mode MOSFET

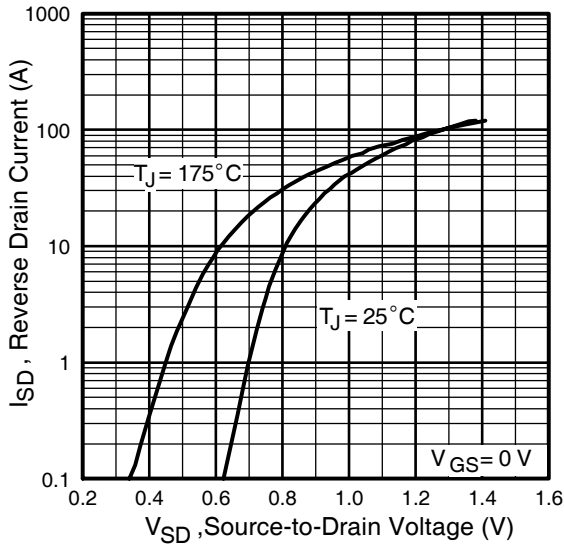


Fig 7. Typical Source-Drain Diode Forward Voltage

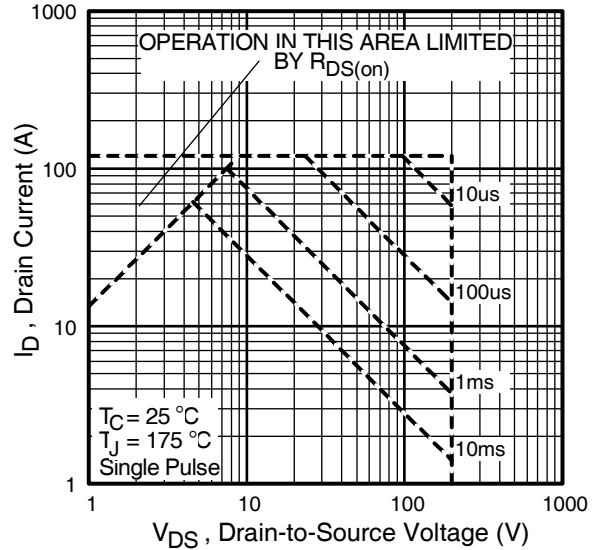


Fig 8. Maximum Safe Operating Area

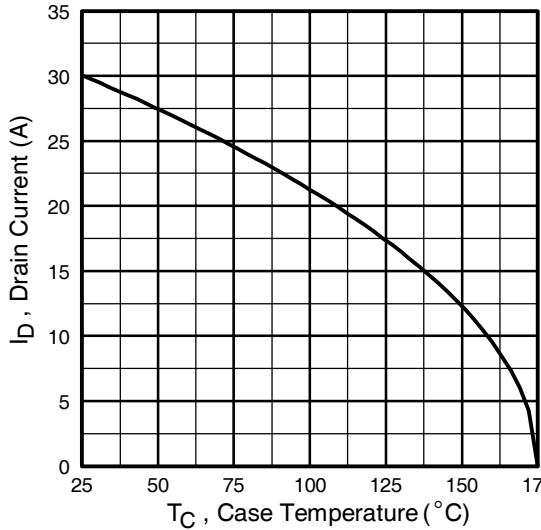


Fig 9. Maximum Drain Current Vs. Case Temperature

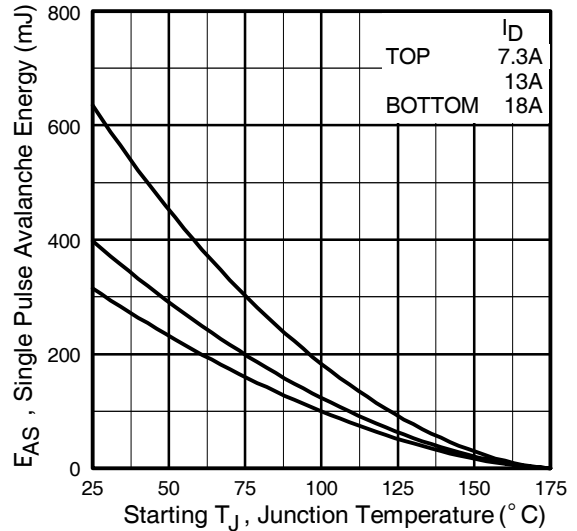


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

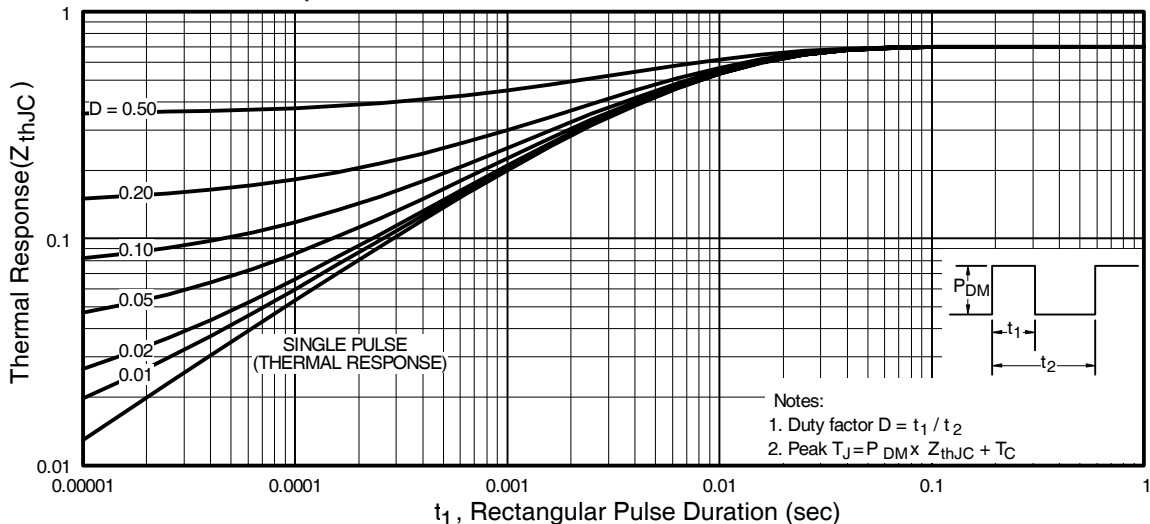
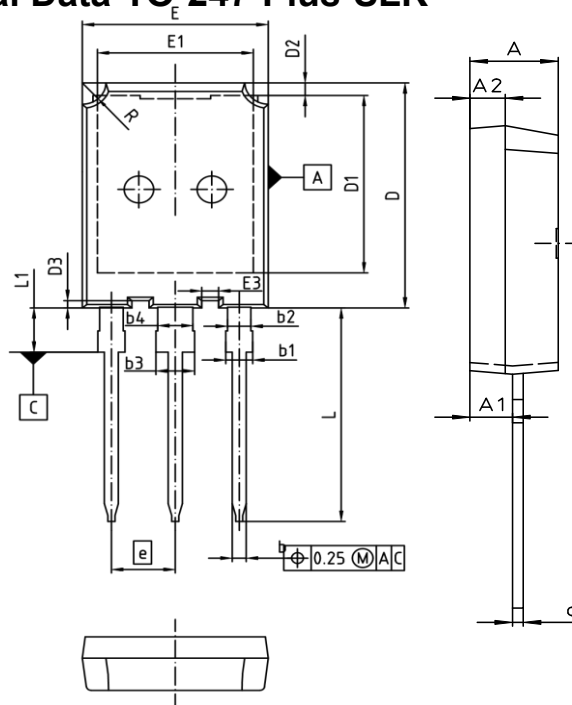


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-TO-247-Plus-SLK



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.201
A1	2.31	2.51	0.091	0.099
A2	1.90	2.10	0.075	0.083
b	1.16	1.26	0.046	0.050
b1	1.96	2.25	0.077	0.089
b2	1.96	2.06	0.077	0.081
c	0.59	0.66	0.023	0.026
D	20.90	21.10	0.823	0.831
D1	16.25	16.85	0.640	0.663
D2	1.05	1.35	0.041	0.053
D3	0.58	0.78	0.023	0.031
E	15.70	15.90	0.618	0.626
E1	13.10	13.50	0.516	0.531
E3	1.35	1.55	0.053	0.061
e	5.44 (BSC)		0.214 (BSC)	
N	3		3	
L	19.80	20.10	0.780	0.791
L1	-	4.30	-	0.169
R	1.90	2.10	0.075	0.083

200V N-Channel Enhancement Mode MOSFET**Attention**

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