GigaDevice Semiconductor Inc.

GD32EPRTxx
Arm® Cortex®-M33 32-bit MCU

Datasheet

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1. General description

The GD32EPRTxx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32EPRTxx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at up to 180 MHz frequency with Flash accesses 0~4 waiting time to obtain maximum efficiency. It provides 384 KB embedded Flash memory, 96 KB SRAM memory and 4 MB PSRAM. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer three 12-bit ADCs, two DACs, three general 16-bit timers, a general 32-bit timer, two basic timers, two PWM advanced timers, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs, six USARTs, two I2Ss, an USBD and an ENET. Additional peripherals as EXMC interface, Serial/Quad Parallel Interface (SQPI) are included.

The device operates from a 1.62 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32EPRTxx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike, optical module and so on.

2. Device overview

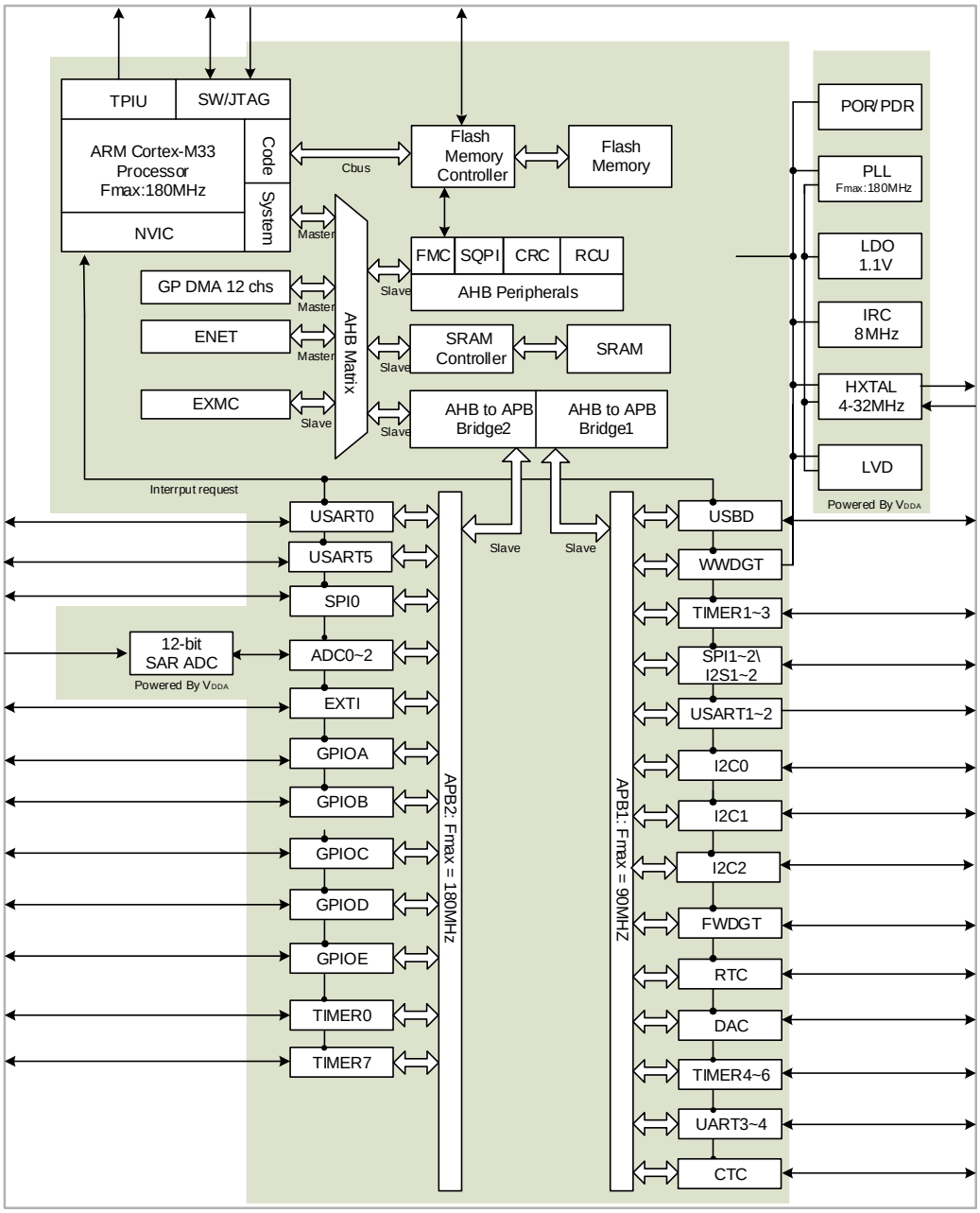
2.1. Device information

Table 2-1. GD32EPRTxx devices features and peripheral list

Part Number		GD32EPRTxx	
		RDT6	VDT6
FLASH (KB)		384	384
SRAM (KB)/PSRAM (MB)		96 / 4	96 / 4
Timers	General timer(16-bit)	3 (2-4)	3 (2-4)
	General timer(32-bit)	1 (1)	1 (1)
	Advanced timer(16-bit)	2 (0,7)	2 (0,7)
	SysTick	1	1
	Basic timer(16-bit)	2 (5-6)	2 (5-6)
	SHRTIMER	0	0
	Watchdog	2	2
	RTC	1	1
Connectivity	USART	4 (0-2,5)	4 (0-2,5)
	UART	2 (3-4)	2 (3-4)
	I2C	3 (0-2)	3 (0-2)
	SPI/I2S	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)
	Ethernet	1	1
	CAN	0	0
	USBD	1	1
GPIO		51	80
EXMC		1	1
DAC		2	2
CMP		0	0
TMU		0	0
ADC	Units	3	3
	Channels	16	16
Package		LQFP64	LQFP100

2.2. Block diagram

Figure 2-1. GD32EPRTxx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32EPRTVDT6 LQFP100 pinouts

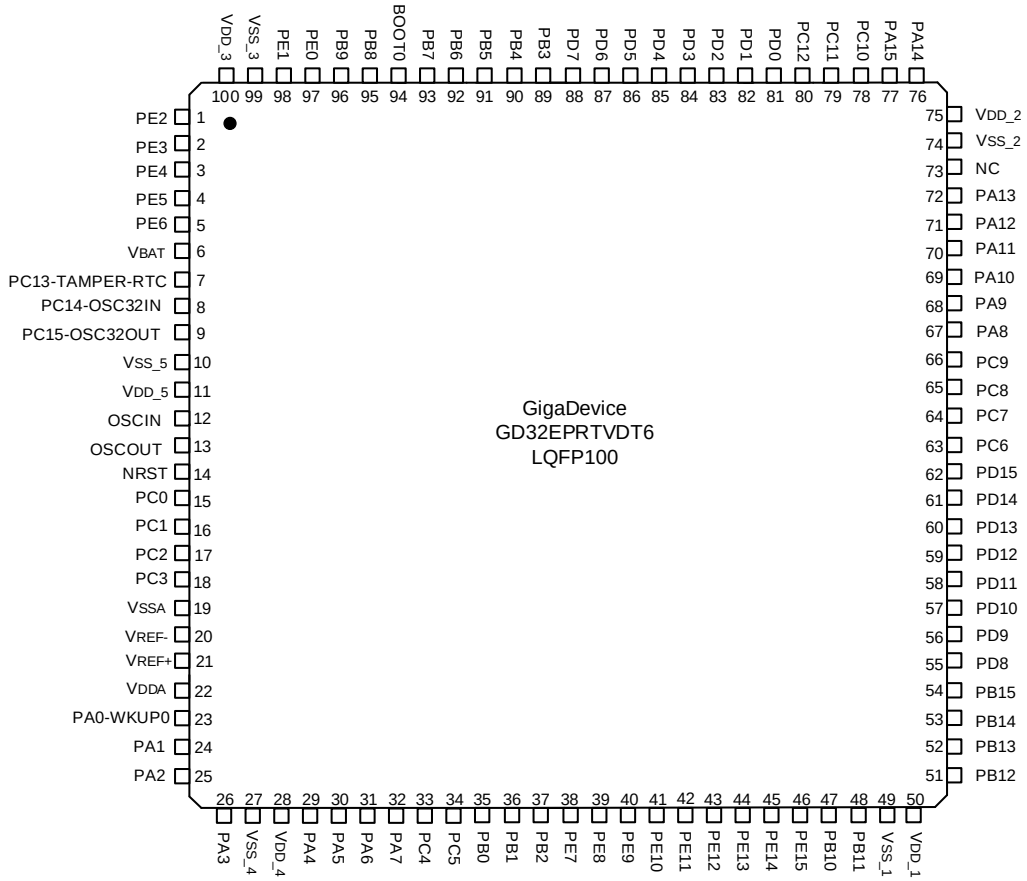
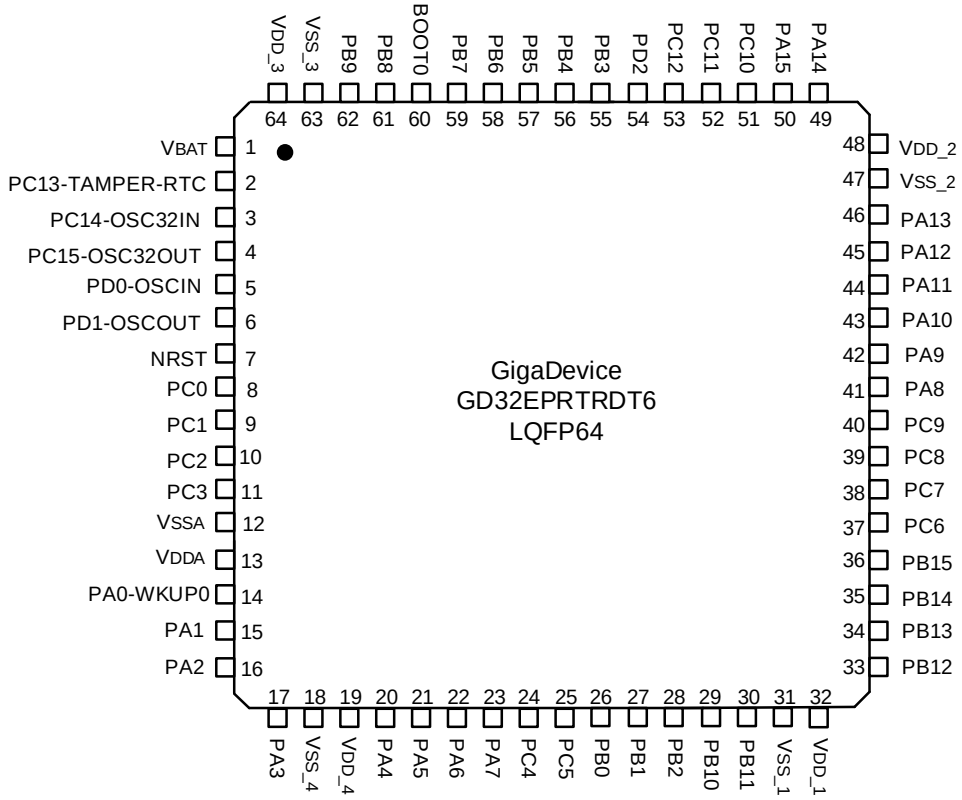


Figure 2-3. GD32EPRTRDT6 LQFP64 pinouts



2.4. Memory map

Table 2-2. GD32EPRTxx memory map

Pre-defined Regions	Bus	Address	Peripherals
External device	AHB3	0xC000 0000 - 0xDFFF FFFF	Reserved
		0xB000 0000 - 0xBFFF FFFF	SQPI_PSRAM(MEM)
		0xA000 1400 - 0xAFFF FFFF	Reserved
		0xA000 1000 - 0xA000 13FF	SQPI_PSRAM(REG)
		0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	EXMC - PC CARD
		0x7000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB1	0x5000 0000 - 0x5003 FFFF	Reserved
		0x4008 0400 - 0x4FFF FFFF	Reserved
		0x4008 0000 - 0x4008 03FF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	ENET
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	Reserved
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	Reserved
		0x4002 0400 - 0x4002 07FF	DMA1

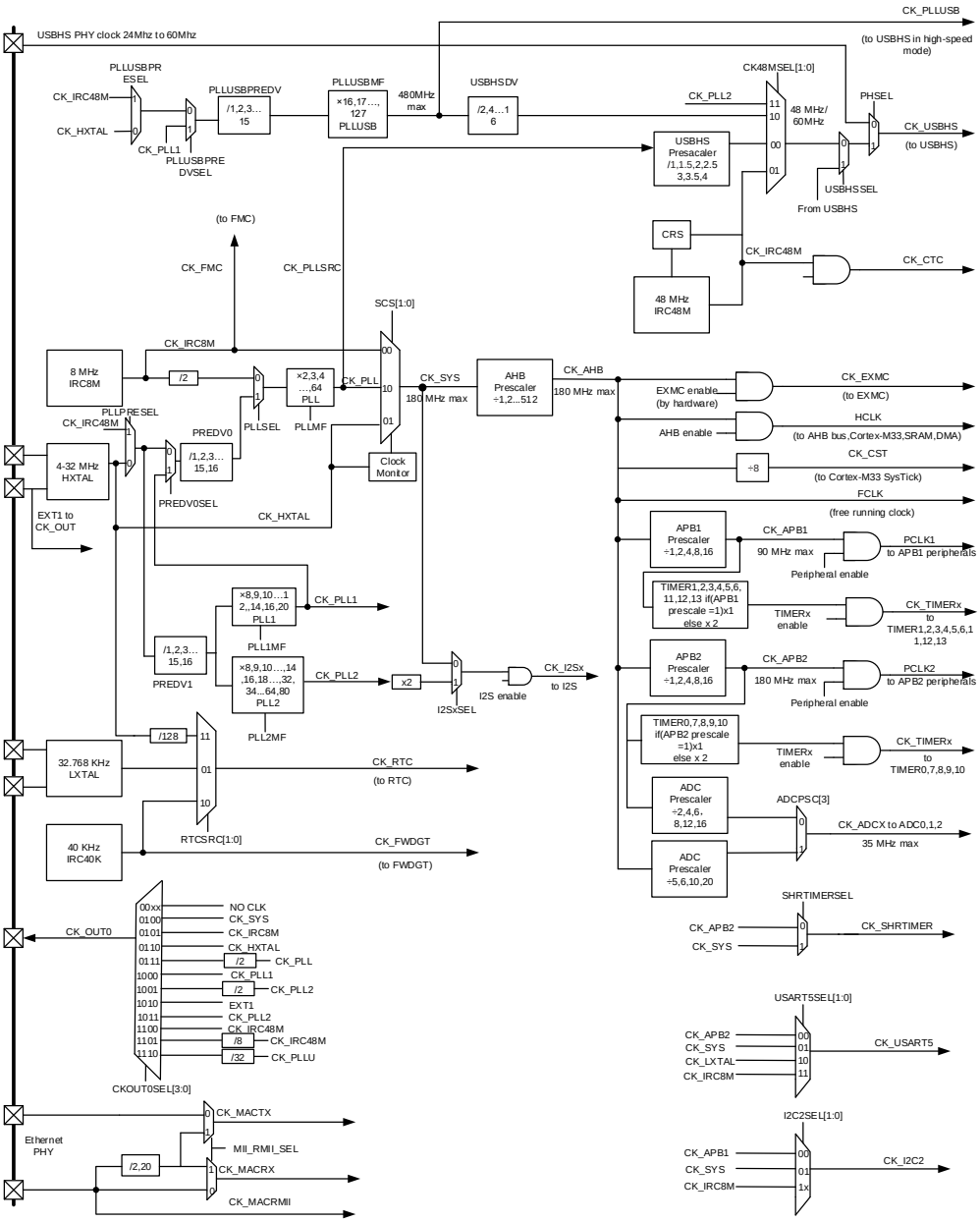
Pre-defined Regions	Bus	Address	Peripherals
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 8400 - 0x4001 FFFF	Reserved
		0x4001 8000 - 0x4001 83FF	Reserved
	APB2	0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	USART5
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	Reserved
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	Reserved
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
		0x4001 3C00 - 0x4001 3FFF	ADC2
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	GPIOE
		0x4001 1400 - 0x4001 17FF	GPIOD
		0x4001 1000 - 0x4001 13FF	GPIOC
		0x4001 0C00 - 0x4001 0FFF	GPIOB
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 CC00 - 0x4000 CFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	I2C2
		0x4000 8C00 - 0x4000 BFFF	Reserved
		0x4000 8800 - 0x4000 8BFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 8400 - 0x4000 87FF	USBSRAM_B
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	USBD SRAM 512 bytes
		0x4000 5C00 - 0x4000 5FFF	USBD
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	I2S2_add
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	I2S1_add
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
		0x2002 0000 - 0x2002 FFFF	Reserved
		0x2000 0000 - 0x2001 FFFF	SRAM

Pre-defined Regions	Bus	Address	Peripherals
Code	AHB	0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option Bytes
		0x1FFF B000 - 0x1FFF F7FF	Boot loader
		0x1FFF 7800 - 0x1FFF AFFF	Reserved
		0x1FFF 7000 - 0x1FFF 77FF	OTP
		0x1FFF 0000 - 0x1FFF 6FFF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x083C 0000 - 0x0FFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0808 0000 - 0x082F FFFF	Reserved
		0x0800 0000 - 0x0807 FFFF	Main Flash
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Reserved
		0x0008 0000 - 0x000F FFFF	Reserved
		0x0002 0000 - 0x0007 FFFF	Aliased to Main Flash or Boot loader
		0x0000 0000 - 0x0001 FFFF	

2.5. Clock tree

Figure 2-4. GD32EPRTxx clock tree



Note:

The TIMERs are clocked by the clock divided from CK_APB2 and CK_APB1. The frequency of TIMERs clock is equal to CK_APBx(APB prescaler is 1), twice the CK_APBx(APB prescaler is not 1).

Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillator

IRC40K: Internal 40K RC oscillator

IRC48M: Internal 48M RC oscillator

2.6. Pin definitions

2.6.1. GD32EPRTVDT6 LQFP100 pin definitions

Table 2-3. GD32EPRTVDT6 LQFP100 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
PE2	1	I/O	5VT	Default: PE2 Alternate2: TRACECK, EXMC_A23
PE3	2	I/O	5VT	Default: PE3 Alternate2: TRACED0, EXMC_A19
PE4	3	I/O	5VT	Default: PE4 Alternate2:TRACED1, EXMC_A20
PE5	4	I/O	5VT	Default: PE5 Alternate2:TRACED2, EXMC_A21
PE6	5	I/O	5VT	Default: PE6 Alternate2:TRACED3, EXMC_A22, WKUP2
V_{BAT}	6	P		Default: V_{BAT}
PC13-TAMPER-RTC	7	I/O		Default: PC13 Alternate2: TAMPER-RTC, WKUP1
PC14-OSC32IN	8	I/O		Default: PC14 Alternate2: OSC32IN
PC15-OSC32OUT	9	I/O		Default: PC15 Alternate2: OSC32OUT
V_{SS_5}	10	P		Default: V_{SS_5}
V_{DD_5}	11	P		Default: V_{DD_5}
OSCIN	12	I		Default: OSCIN Remap: PD0
OSCOUT	13	O		Default: OSCOUT Remap: PD1
NRST	14	I/O		Default: NRST
PC0	15	I/O		Default: PC0 Alternate2: ADC012_IN10
PC1	16	I/O		Default: PC1 Alternate2: ADC012_IN11, ETH_MII_MDC, ETH_RMII_MDC
PC2	17	I/O		Default: PC2 Alternate1: I2S1_ADD_SD Alternate2: ADC012_IN12, ETH_MII_TXD2
PC3	18	I/O		Default: PC3 Alternate2: ADC012_IN13, ETH_MII_TX_CLK

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
V_{SSA}	19	P		Default: V_{SSA}
V_{REF-}	20	P		Default: V_{REF-}
V_{REF+}	21	P		Default: V_{REF+}
V_{DDA}	22	P		Default: V_{DDA}
PA0-WKUP0	23	I/O		Default: PA0 Alternate2: WKUP0, USART1_CTS, ADC012_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, ETH_MII_CRS
PA1	24	I/O		Default: PA1 Alternate2: USART1_RTS, ADC012_IN1, TIMER4_CH1, TIMER1_CH1, ETH_MII_RX_CLK, ETH_RMII_REF_CLK
PA2	25	I/O		Default: PA2 Alternate2: USART1_TX, TIMER4_CH2, ADC012_IN2, TIMER1_CH2, ETH_MII_MDIO, ETH_RMII_MDIO, SPI0_IO2, WKUP3
PA3	26	I/O		Default: PA3 Alternate2: USART1_RX, TIMER4_CH3, ADC012_IN3, TIMER1_CH3, ETH_MII_COL, SPI0_IO3
V_{SS_4}	27	P		Default: V_{SS_4}
V_{DD_4}	28	P		Default: V_{DD_4}
PA4	29	I/O		Default: PA4 Alternate2: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4 Remap: SPI2_NSS, I2S2_WS
PA5	30	I/O		Default: PA5 Alternate2: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	31	I/O		Default: PA6 Alternate2: SPI0_MISO, TIMER7_BRKIN, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BRKIN
PA7	32	I/O		Default: PA7 Alternate2: SPI0_MOSI, TIMER7_CH0_ON, ADC01_IN7, TIMER2_CH1, ETH_MII_RX_DV, ETH_RMII_CRS_DV Remap: TIMER0_CH0_ON
PC4	33	I/O		Default: PC4 Alternate2: ADC01_IN14, ETH_MII_RXD0, ETH_RMII_RXD0
PC5	34	I/O		Default: PC5 Alternate2: ADC01_IN15, ETH_MII_RXD1, ETH_RMII_RXD1, WKUP4
PB0	35	I/O		Default: PB0 Alternate2: ADC01_IN8, TIMER2_CH2,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
				TIMER7_CH1_ON, ETH_MII_RXD2 Remap: TIMER0_CH1_ON
PB1	36	I/O		Default: PB1 Alternate2: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON, ETH_MII_RXD3 Remap: TIMER0_CH2_ON
PB2	37	I/O	5VT	Default: PB2, BOOT1
PE7	38	I/O	5VT	Default: PE7 Alternate2: EXMC_D4 Remap: TIMER0_ETI
PE8	39	I/O	5VT	Default: PE8 Alternate2: EXMC_D5 Remap: TIMER0_CH0_ON
PE9	40	I/O	5VT	Default: PE9 Alternate2: EXMC_D6 Remap: TIMER0_CH0
PE10	41	I/O	5VT	Default: PE10 Alternate2: EXMC_D7 Remap: TIMER0_CH1_ON
PE11	42	I/O	5VT	Default: PE11 Alternate2: EXMC_D8 Remap: TIMER0_CH1
PE12	43	I/O	5VT	Default: PE12 Alternate2: EXMC_D9 Remap: TIMER0_CH2_ON
PE13	44	I/O	5VT	Default: PE13 Alternate2: EXMC_D10 Remap: TIMER0_CH2
PE14	45	I/O	5VT	Default: PE14 Alternate2: EXMC_D11 Remap: TIMER0_CH3
PE15	46	I/O	5VT	Default: PE15 Alternate2: EXMC_D12 Remap: TIMER0_BRKIN
PB10	47	I/O	5VT	Default: PB10 Alternate2: I2C1_SCL, USART2_TX, ETH_MII_RX_ER Remap: TIMER1_CH2
PB11	48	I/O	5VT	Default: PB11 Alternate2: I2C1_SDA, USART2_RX, ETH_MII_TX_EN, ETH_RMII_TX_EN Remap: TIMER1_CH3
V_{SS_1}	49	P		Default: V_{SS_1}
V_{DD_1}	50	P		Default: V_{DD_1}

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
PB12	51	I/O	5VT	Default: PB12 Alternate2: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, ETH_MII_TXD0, ETH_RMII_TXD0
PB13	52	I/O	5VT	Default: PB13 Alternate2: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, ETH_MII_TXD1, ETH_RMII_TXD1, I2C1_TXFRAME
PB14	53	I/O	5VT	Default: PB14 Alternate1: I2S1_ADD_SD Alternate2: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON
PB15	54	I/O	5VT	Default: PB15 Alternate2: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, WKUP6
PD8	55	I/O	5VT	Default: PD8 Alternate2: EXMC_D13 Remap: USART2_TX, ETH_MII_RX_DV, ETH_RMII_CRS_DV
PD9	56	I/O	5VT	Default: PD9 Alternate2: EXMC_D14 Remap: USART2_RX, ETH_MII_RXD0, ETH_RMII_RXD0
PD10	57	I/O	5VT	Default: PD10 Alternate2: EXMC_D15 Remap: USART2_CK, ETH_MII_RXD1, ETH_RMII_RXD1
PD11	58	I/O	5VT	Default: PD11 Alternate2: EXMC_A16 Remap: USART2_CTS, ETH_MII_RXD2
PD12	59	I/O	5VT	Default: PD12 Alternate2: EXMC_A17 Remap: TIMER3_CH0, USART2_RTS, ETH_MII_RXD3
PD13	60	I/O	5VT	Default: PD13 Alternate2: EXMC_A18 Remap: TIMER3_CH1
PD14	61	I/O	5VT	Default: PD14 Alternate2: EXMC_D0 Remap: TIMER3_CH2
PD15	62	I/O	5VT	Default: PD15 Alternate2: EXMC_D1 Remap: TIMER3_CH3, CTC_SYNC
PC6	63	I/O	5VT	Default: PC6

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
				Alternate1: USART5_TX Alternate2: I2S1_MCK, TIMER7_CH0 Remap: TIMER2_CH0
PC7	64	I/O	5VT	Default: PC7 Alternate1: USART5_RX Alternate2: I2S2_MCK, TIMER7_CH1 Remap: TIMER2_CH1
PC8	65	I/O	5VT	Default: PC8 Alternate1: USART5_CK Alternate2: TIMER7_CH2 Remap: TIMER2_CH2
PC9	66	I/O	5VT	Default: PC9 Alternate1: I2C2_SDA Alternate2: TIMER7_CH3 Remap: TIMER2_CH3
PA8	67	I/O	5VT	Default: PA8 Alternate1: I2C2_SCL Alternate2: USART0_CK, TIMER0_CH0, CK_OUT, CTC_SYNC
PA9	68	I/O	5VT	Default: PA9 Alternate1: I2C2_SMBA Alternate2: USART0_TX, TIMER0_CH1
PA10	69	I/O	5VT	Default: PA10 Alternate2: USART0_RX, TIMER0_CH2
PA11	70	I/O	5VT	Default: PA11 Alternate1: USART5_TX Alternate2: USART0_CTS, USBDM, TIMER0_CH3
PA12	71	I/O	5VT	Default: PA12 Alternate1: USART5_RX Alternate2: USART0_RTS, USBDP, TIMER0_ETI
PA13	72	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
NC	73			-
V_{SS_2}	74	P		Default: V_{SS_2}
V_{DD_2}	75	P		Default: V_{DD_2}
PA14	76	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	77	I/O	5VT	Default: JTDI Alternate2: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS
PC10	78	I/O	5VT	Default: PC10 Alternate1: I2C2_SCL Alternate2: UART3_TX

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
				Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	79	I/O	5VT	Default: PC11 Alternate1: I2S2_ADD_SD Alternate2: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	80	I/O	5VT	Default: PC12 Alternate2: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD0	81	I/O	5VT	Default: PD0 Alternate2: EXMC_D2 Remap: OSCIN
PD1	82	I/O	5VT	Default: PD1 Alternate2: EXMC_D3 Remap: OSCOUT
PD2	83	I/O	5VT	Default: PD2 Alternate2: TIMER2_ETI, UART4_RX
PD3	84	I/O	5VT	Default: PD3 Alternate2: EXMC_CLK Remap: USART1_CTS
PD4	85	I/O	5VT	Default: PD4 Alternate2: EXMC_NOE Remap: USART1_RTS
PD5	86	I/O	5VT	Default: PD5 Alternate2: EXMC_NWE Remap: USART1_TX
PD6	87	I/O	5VT	Default: PD6 Alternate2: EXMC_NWAIT Remap: USART1_RX
PD7	88	I/O	5VT	Default: PD7 Alternate2: EXMC_NE0, EXMC_NCE1 Remap: USART1_CK
PB3	89	I/O	5VT	Default: JTDO Alternate2: SPI2_SCK, I2S2_CK Remap: TIMER1_CH1, PB3, TRACESWO, SPI0_SCK
PB4	90	I/O	5VT	Default: NJTRST Alternate1: I2C2_SDA, I2S2_ADD_SD Alternate2: SPI2_MISO, I2C0_TXFRAME Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	91	I/O		Default: PB5 Alternate1: I2C2_SCL Alternate2: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ETH_MII_PPS_OUT, ETH_RMII_PPS_OUT, WKUP5 Remap: TIMER2_CH1, SPI0_MOSI

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
PB6	92	I/O	5VT	Default: PB6 Alternate2: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2
PB7	93	I/O	5VT	Default: PB7 Alternate2: I2C0_SDA , TIMER3_CH1, EXMC_NADV Remap: USART0_RX, SPI0_IO3
BOOT0	94	I		Default: BOOT0
PB8	95	I/O	5VT	Default: PB8 Alternate1: I2C2_SDA Alternate2: TIMER3_CH2, ETH_MII_TXD3 Remap: I2C0_SCL
PB9	96	I/O	5VT	Default: PB9 Alternate2: TIMER3_CH3 Remap: I2C0_SDA
PE0	97	I/O	5VT	Default: PE0 Alternate2: TIMER3_ETI, EXMC_NBL0
PE1	98	I/O	5VT	Default: PE1 Alternate2: EXMC_NBL1
V_{SS_3}	99	P		Default: V_{SS_3}
V_{DD_3}	100	P		Default: V_{DD_3}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Alternate1: The specified function can be mapped to the specific pin by configuring AFIO_PCFA ~ AFIO_PCFG registers.

Alternate2: These functions can be enabled with correct GPIO and function module mode configurations.

Remap: A group of the specified module functions can be mapped to the specified pins by configuring AFIO_PCF0 ~ AFIO_PCF1 registers.

2.6.2. GD32EPRTRDT6 LQFP64 pin definitions

Table 2-4. GD32EPRTRDT6 LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Alternate2: TAMPER-RTC, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Alternate2: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Alternate2: OSC32OUT
OSCIN	5	I		Default: OSCIN Remap: PD0
OSCOUT	6	O		Default: OSCOUT Remap: PD1
NRST	7	I/O		Default: NRST
PC0	8	I/O		Default: PC0 Alternate2: ADC012_IN10
PC1	9	I/O		Default: PC1 Alternate2: ADC012_IN11, ETH_MII_MDC, ETH_RMII_MDC
PC2	10	I/O		Default: PC2 Alternate1: I2S1_ADD_SD Alternate2: ADC012_IN12, ETH_MII_TXD2
PC3	11	I/O		Default: PC3 Alternate2: ADC012_IN13, ETH_MII_TX_CLK
V_{SSA}	12	P		Default: V_{SSA}
V_{DDA}	13	P		Default: V_{DDA}
PA0-WKUP0	14	I/O		Default: PA0 Alternate2: WKUP0, USART1_CTS, ADC012_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, ETH_MII_CRS
PA1	15	I/O		Default: PA1 Alternate2: USART1_RTS, ADC012_IN1, TIMER4_CH1, TIMER1_CH1, ETH_MII_RX_CLK, ETH_RMII_REF_CLK
PA2	16	I/O		Default: PA2 Alternate2: USART1_TX, TIMER4_CH2, ADC012_IN2, TIMER1_CH2, ETH_MII_MDIO, ETH_RMII_MDIO, SPI0_IO2, WKUP3
PA3	17	I/O		Default: PA3 Alternate2: USART1_RX, TIMER4_CH3, ADC012_IN3,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
				TIMER1_CH3, ETH_MII_COL, SPI0_IO3
V_{SS_4}	18	P		Default: V_{SS_4}
V_{DD_4}	19	P		Default: V_{DD_4}
PA4	20	I/O		Default: PA4 Alternate2: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4 Remap: SPI2_NSS, I2S2_WS
PA5	21	I/O		Default: PA5 Alternate2: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	22	I/O		Default: PA6 Alternate2: SPI0_MISO, TIMER7_BRKIN, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BRKIN
PA7	23	I/O		Default: PA7 Alternate2: SPI0_MOSI, TIMER7_CH0_ON, ADC01_IN7, TIMER2_CH1, ETH_MII_RX_DV, ETH_RMII_CRS_DV Remap: TIMER0_CH0_ON
PC4	24	I/O		Default: PC4 Alternate2: ADC01_IN14, ETH_MII_RXD0, ETH_RMII_RXD0
PC5	25	I/O		Default: PC5 Alternate2: ADC01_IN15, ETH_MII_RXD1, ETH_RMII_RXD1, WKUP4
PB0	26	I/O		Default: PB0 Alternate2: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON, ETH_MII_RXD2 Remap: TIMER0_CH1_ON
PB1	27	I/O		Default: PB1 Alternate2: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON, ETH_MII_RXD3 Remap: TIMER0_CH2_ON
PB2	28	I/O	5VT	Default: PB2, BOOT1
PB10	29	I/O	5VT	Default: PB10 Alternate2: I2C1_SCL, USART2_TX, ETH_MII_RX_ER Remap: TIMER1_CH2
PB11	30	I/O	5VT	Default: PB11 Alternate2: I2C1_SDA, USART2_RX, ETH_MII_TX_EN, ETH_RMII_TX_EN Remap: TIMER1_CH3
V_{SS_1}	31	P		Default: V_{SS_1}
V_{DD_1}	32	P		Default: V_{DD_1}
PB12	33	I/O	5VT	Default: PB12

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
				Alternate2: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, ETH_MII_TXD0, ETH_RMII_TXD0
PB13	34	I/O	5VT	Default: PB13 Alternate2: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, ETH_MII_TXD1, ETH_RMII_TXD1, I2C1_TXFRAME
PB14	35	I/O	5VT	Default: PB14 Alternate1: I2S1_ADD_SD Alternate2: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON
PB15	36	I/O	5VT	Default: PB15 Alternate2: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, WKUP6
PC6	37	I/O	5VT	Default: PC6 Alternate1: USART5_TX Alternate2: I2S1_MCK, TIMER7_CH0 Remap: TIMER2_CH0
PC7	38	I/O	5VT	Default: PC7 Alternate1: USART5_RX Alternate2: I2S2_MCK, TIMER7_CH1 Remap: TIMER2_CH1
PC8	39	I/O	5VT	Default: PC8 Alternate1: USART5_CK Alternate2: TIMER7_CH2 Remap: TIMER2_CH2
PC9	40	I/O	5VT	Default: PC9 Alternate1: I2C2_SDA Alternate2: TIMER7_CH3 Remap: TIMER2_CH3
PA8	41	I/O	5VT	Default: PA8 Alternate1: I2C2_SCL Alternate2: USART0_CK, TIMER0_CH0, CK_OUT, CTC_SYNC
PA9	42	I/O	5VT	Default: PA9 Alternate1: I2C2_SMBA Alternate2: USART0_TX, TIMER0_CH1
PA10	43	I/O	5VT	Default: PA10 Alternate2: USART0_RX, TIMER0_CH2
PA11	44	I/O	5VT	Default: PA11 Alternate1: USART5_TX Alternate2: USART0_CTS, USBDM, TIMER0_CH3
PA12	45	I/O	5VT	Default: PA12 Alternate1: USART5_RX

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
				Alternate2: USART0_RTS, USBDP, TIMER0_ETI
PA13	46	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
V_{SS_2}	47	P		Default: V_{SS_2}
V_{DD_2}	48	P		Default: V_{DD_2}
PA14	49	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	50	I/O	5VT	Default: JTDI Alternate2: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS
PC10	51	I/O	5VT	Default: PC10 Alternate1: I2C2_SCL Alternate2: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	52	I/O	5VT	Default: PC11 Alternate1: I2S2_ADD_SD Alternate2: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	53	I/O	5VT	Default: PC12 Alternate2: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD2	54	I/O	5VT	Default: PD2 Alternate2: TIMER2_ETI, UART4_RX
PB3	55	I/O	5VT	Default: JTDO Alternate2: SPI2_SCK, I2S2_CK Remap: TIMER1_CH1, PB3, TRACESWO, SPI0_SCK
PB4	56	I/O	5VT	Default: NJTRST Alternate1: I2C2_SDA, I2S2_ADD_SD Alternate2: SPI2_MISO, I2C0_TXFRAME Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	57	I/O		Default: PB5 Alternate1: I2C2_SCL Alternate2: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ETH_MII_PPS_OUT, ETH_RMII_PPS_OUT, WKUP5 Remap: TIMER2_CH1, SPI0_MOSI
PB6	58	I/O	5VT	Default: PB6 Alternate2: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2
PB7	59	I/O	5VT	Default: PB7 Alternate2: I2C0_SDA , TIMER3_CH1, EXMC_NADV Remap: USART0_RX, SPI0_IO3
BOOT0	60	I		Default: BOOT0

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description(3)
PB8	61	I/O	5VT	Default: PB8 Alternate1: I2C2_SDA Alternate2: TIMER3_CH2, ETH_MII_TXD3 Remap: I2C0_SCL
PB9	62	I/O	5VT	Default: PB9 Alternate2: TIMER3_CH3 Remap: I2C0_SDA
V_{SS_3}	63	P		Default: V_{SS_3}
V_{DD_3}	64	P		Default: V_{DD_3}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Alternate1: The specified function can be mapped to the specific pin by configuring AFIO_PCFA ~ AFIO_PCFG registers.

Alternate2: These functions can be enabled with correct GPIO and function module mode configurations.

Remap: A group of the specified module functions can be mapped to the specified pins by configuring AFIO_PCF0 ~ AFIO_PCF1 registers.

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption.

32-bit Arm® Cortex®-M33 processor core

- Up to 180 MHz operation frequency
- Ultra-low power, energy-efficient operation
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M33 processor is based on the ARMv8 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit (BPU)
- Data Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Memory Protection Unit (MPU)
- Floating Point Unit (FPU)
- DSP Extension (DSP)

3.2. Embedded memory

- Up to 384 Kbytes of Flash memory
- Up to 96 Kbytes of SRAM with hardware parity checking
- Up to 4 Mbytes of PSRAM embedded

384 Kbytes of inner Flash, 96 Kbytes of inner SRAM and 4 Mbytes of inner PSRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with 0~4 waiting time. ***Table 2-2. GD32EPRTxx memory map*** shows the memory map of the GD32EPRTxx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 1.62 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 180 MHz/180 MHz/90 MHz. See ***Figure 2-4. GD32EPRTxx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.56 V and down to 1.52V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.62 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 1.62 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- V_{BAK} range: 1.62 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PD5 and PD6).

3.5. Power saving modes

The MCU supports five kinds of power saving modes to achieve even lower power consumption. They are Sleep, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.1V domain are off, and all of IRC8M, IRC48M, HXTAL and PLLs are disabled. The contents of SRAM and registers are preserved. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, LVD output, USB wakeup, Ethernet wakeup, I2C2 wakeup and USART5 wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Deep-sleep 1** mode
  In Deep-sleep 1 mode, all clocks in the 1.1V domain are off, and all of IRC8M, IRC48M, HXTAL and PLLs are disabled. The power of COREOFF1 domain is cut off. The contents of registers in COREOFF1 domain are lost. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep 1 mode including the 16 external lines, the RTC alarm, LVD output, USB wakeup, Ethernet wakeup, I2C2 wakeup and USART5 wakeup. Waking up from Deep-sleep 1 mode needs an additional delay to power on COREOFF1 domain. When exiting the deep-sleep 1 mode, the IRC8M is selected as the system clock.
- **Deep-sleep 2** mode
  In Deep-sleep 2 mode, all clocks in the 1.1V domain are off, and all of IRC8M, IRC48M, HXTAL and PLLs are disabled. The power of COREOFF0/COREOFF1 domain is cut off. The contents of SRAM except for the first 32K and registers in COREOFF0/COREOFF1 domain are lost. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, LVD output, USB wakeup, Ethernet wakeup, I2C2 wakeup and USART5 wakeup. Waking up from Deep-sleep 2 mode needs an additional delay to power on COREOFF1 domain. Waking up from Deep-sleep 2 mode needs an additional delay to power on COREOFF0/COREOFF1 domain. When exiting the deep-sleep 2 mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.1V domain is power off, the LDO is shut down, and all of IRC8M, IRC48M, HXTAL and PLL are disabled. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pins.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.5 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{REF-} to V_{REF+}
- Temperature sensor

Three 12-bit 2.5 MSPS multi-channel ADCs are integrated in the device. It has a total of 18 multiplexed channels: up to 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}) and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between V_{REF-} and V_{REF+}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx), and the advanced timers (TIMER0 and TIMER7). The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to V_{REF+}/V_{REF-} pins. According to the different packages, V_{REF+} pin can be connected to V_{DDA} pin, or external reference voltage, V_{REF-} pin must be connected to V_{SSA} pin. The V_{REF+} pin is only available on no less than 100-pin packages, or else the V_{REF+} pin is not available and internally connected to V_{DDA}. The V_{REF-} pin is only available on no less than 100-pin packages, or else the V_{REF-} pin is not available and internally connected to V_{SSA}.

3.7. Digital to analog converter (DAC)

- Two 12-bit DACs with independent output channels
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC is used to generate variable analog outputs. The DAC channels can be triggered by the timer, or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF+}.

3.8. DMA

- 7 channels for DMA0 controller and 5 channels for DMA1 controller
- Peripherals supported: Timers, ADCs, DACs, SPIs, I2Cs, USARTs and I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 112 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 80 general purpose I/O pins (GPIO) in GD32EPRTxx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15 and PE0 ~ PE15 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0, TIMER7), one 32-bit general timer (TIMER1), up to three 16-bit general timers (TIMER2 ~ TIMER4), and two 16-bit basic timer (TIMER5, TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0, TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other

general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIMER2 ~ TIMER4 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 &TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32EPRTxx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep, deep-sleep 1, deep-sleep 2 and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC)

- 32-bit programmable counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wakeup event

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

I2C0 and I2C1:

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 2.0 and PMBus compatible
- Supports SAM_V mode

I2C2:

- Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- SMBus 3.0 and PMBus 1.3 compatible
- Wakeup from Deep-sleep mode on address match

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad-SPI configuration available in master mode (only in SPI0)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

USART0~2, UART3~4:

- Maximum speed up to 22.5 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

USART5:

- Maximum speed up to 22.5 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface
- Dual clock domain
- Wake up from Deep-sleep mode

The USART (USART0, USART1, USART2, USART5) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32EPRTxx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.16. Universal Serial Bus full-speed device interface (USBD)

- USB 2.0 full-speed device controller.
- Support USB 2.0 Link Power Management.
- Dedicated 512-byte SRAM used for data packet buffer.
- Integrated USB PHY.

The Universal Serial Bus full-speed device interface (USBD) module contains a full-speed internal USB PHY and no more external PHY chip is needed. USBD supports all the four types of transfer (control, bulk, interrupt and isochronous) defined in USB 2.0 protocol. USBD supports 8 USB endpoints that can be individually configured.

3.17. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.18. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and PC card
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and PC card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.19. Serial/Quad Parallel Interface (SQPI)

- SQPI controller support configuring output clock frequency which is divided by HCLK.
- SQPI controller support no address phase and data phase operation which is named special command by the controller.
- SQPI controller support 256MB external memory space.
  Logic memory address range: 0xB000_0000 - 0xBFFF_FFFF.
- SQPI controller support 6 types mode for different combination of command, address, wait cycle, and data phase.

Serial/Quad Parallel Interface (SQPI) is a controller for external serial/dual/quad parallel

interface memory peripheral. For example: SQPI-PSRAM and SQPI-FLASH. With this controller, users can use external SQPI interface memory as SRAM simply.

Note: There is a 4 Mbytes PSRAM embedded, and the SQPI interface is internally connected to GPIOF ports: SQPI_DO – PF0, SQPI_D1 – PF4, SQPI_D2 – PF2, SQPI_D3 – PF10, SQPI_CLK – PF8, SQPI_CSN – PF6. Users should configure the GPIOF corresponding bits to SQPI function before using the embedded PSRAM.

3.20. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.21. Package and operation temperature

- LQFP100 (GD32EPRTVDT6) and LQFP64 (GD32EPRTRDT6).
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings (1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 6.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

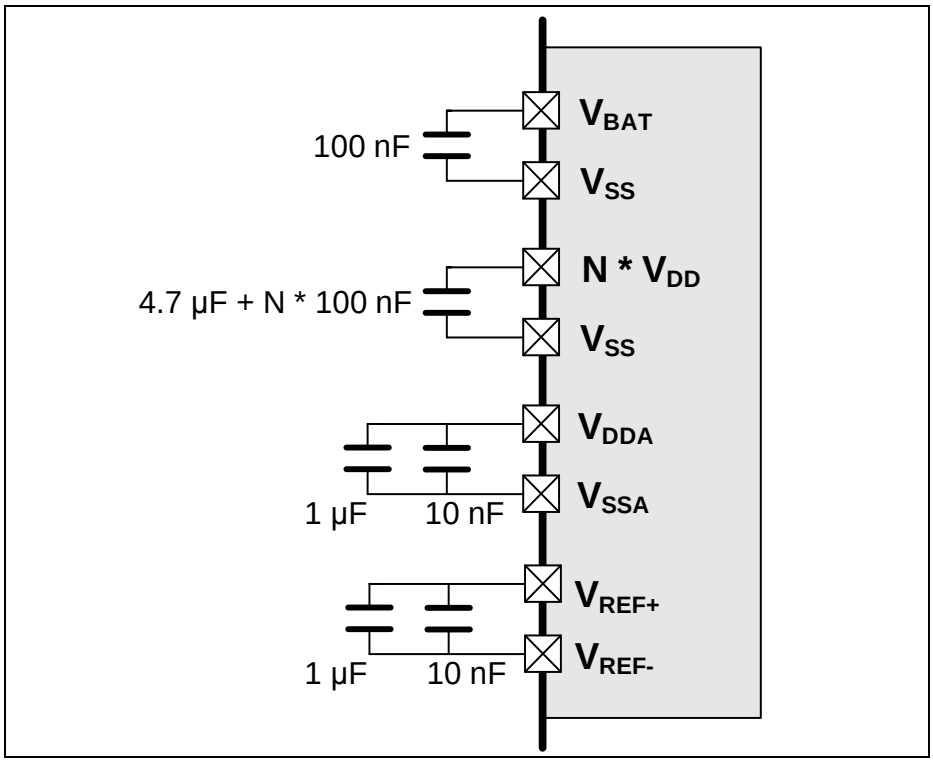
4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.71	3.3	3.6	V
V_{DDA}	Analog supply voltage, f_{ADCMAX} = 35 MHz	—	2.4	3.3	3.6	V
	Analog supply voltage, f_{ADCMAX} = 14 MHz		1.71	—	2.4	
V_{BAT}	Battery supply voltage	—	1.71	—	3.6	V

(1) Based on characterization, not tested in production.

Figure 4-1. Recommended power supply decoupling capacitors (1)(2)



(1) The V_{REF+} and V_{REF-} pins are only available on no less than 100-pin packages, or else the V_{REF+} and V_{REF-} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	180	MHz
f_{APB1}	APB1 clock frequency	—	—	90	MHz
f_{APB2}	APB2 clock frequency	—	—	180	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/ V
	V_{DD} fall time rate		20	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions (1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	—	µs
		Clock source from IRC8M	—	

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics (1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	—	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)	—	
	Wakeup from Deep-sleep mode (LDO in low power mode)	—	
$t_{Standby}$	Wakeup from Standby mode	—	

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics (2)(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals enabled	—	59.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals disabled	—	26.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 160 MHz, All peripherals enabled	—	53.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 160 MHz, All peripherals disabled	—	23.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled	—	41	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled	—	18.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled	—	37.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled	—	16.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals enabled	—	33.4	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 96 MHz, All peripherals disabled	—	15	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals enabled	—	25.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 72 MHz, All peripherals disabled	—	11.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals enabled	—	18	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 48 MHz, All peripherals disabled	—	7.96	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals enabled	—	14	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 36 MHz, All peripherals disabled	—	6.49	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals enabled	—	9.73	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 24 MHz, All peripherals disabled	—	4.83	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals enabled	—	7.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 16 MHz, All peripherals disabled	—	3.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals enabled	—	4.62	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System clock = 8 MHz, All peripherals disabled	—	2.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals enabled	—	—	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals disabled	—	—	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals enabled	—	—	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, All peripherals disabled	—	—	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 180 MHz, CPU clock off, All peripherals enabled	—	47.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 180 MHz, CPU clock off, All peripherals disabled	—	9.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 160 MHz, CPU clock off, All peripherals enabled	—	42.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 160 MHz, CPU clock off, All peripherals disabled	—	8.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals enabled	—	32.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 120 MHz, CPU clock off, All peripherals disabled	—	7.07	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled	—	29.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled	—	6.57	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled	—	26.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled	—	6.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals enabled	—	20.7	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 72 MHz, CPU clock off, All peripherals disabled	—	5.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled	—	14.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled	—	4.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled	—	11.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled	—	3.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals enabled	—	8.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 24 MHz, CPU clock off, All peripherals disabled	—	3.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals enabled	—	6.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 16 MHz, CPU clock off, All peripherals disabled	—	2.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals enabled	—	4.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 8 MHz, CPU clock off, All peripherals disabled	—	2.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System Clock = 4 MHz, CPU clock off, All peripherals enabled	—	—	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System Clock = 4 MHz, CPU clock off, All peripherals disabled	—	—	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, CPU clock off, All peripherals enabled	—	—	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System Clock = 2 MHz, CPU clock off, All peripherals disabled	—	—	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in run mode, IRC40K off, RTC off, All GPIOs analog mode	—	461.33	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode	—	413.00	—	μA
		V_{DD} = V_{DDA} = 3.3 V, Main LDO in under drive mode, IRC40K off, RTC off, All GPIOs analog mode	—	258.00	—	μA
		V_{DD} = V_{DDA} = 3.3 V, Low Power LDO in under drive mode, IRC40K off, RTC off, All GPIOs analog mode	—	210.67	—	μA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	3.79	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	3.58	—	μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off	—	3.08	—	μA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.95	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.82	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.67	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.59	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.53	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.40	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL	—	1.25	—	μA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		Medium High driving				
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.18	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	1.12	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.99	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.84	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	0.77	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	1.00	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.87	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.72	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.64	—	μA

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T_A = 25 °C and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

Figure 4-2. Typical supply current consumption in Run mode

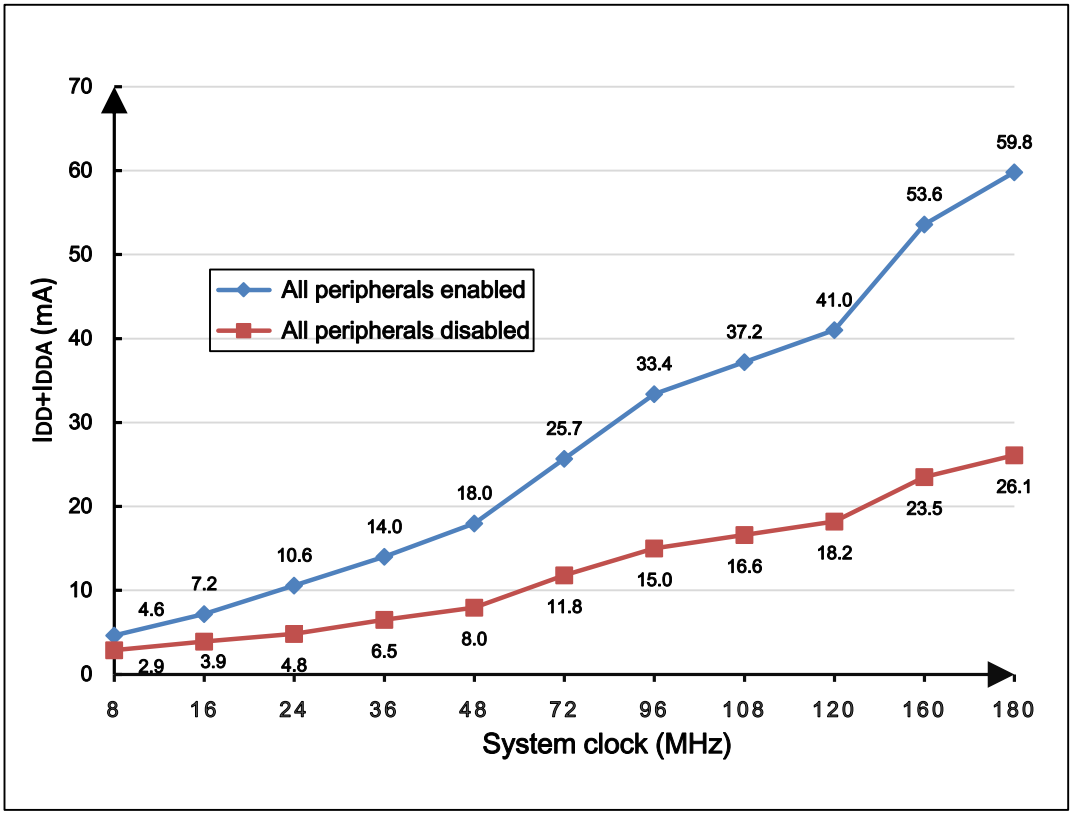


Figure 4-3. Typical supply current consumption in Sleep mode

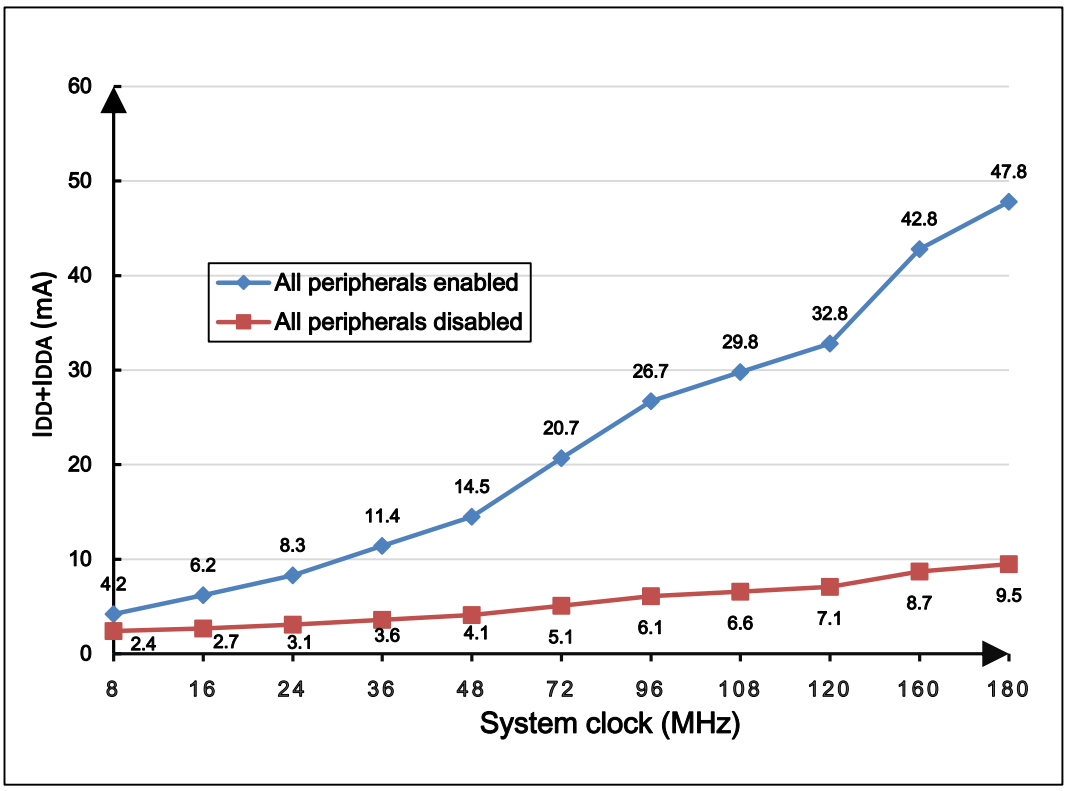


Table 4-8. Peripheral current consumption characteristics (1)

Peripherals(4)		Typical consumption at T_A = 25 ℃ （TYP）	Unit
APB1	CTC	—	mA
	I2C2	—	
	DAC(2)	—	
	PMU	—	
	BKP	—	
	I2C1	—	
	I2C0	—	
	UART4	—	
	UART3	—	
	USART2	—	
	USART1	—	
	SPI2/I2S2	—	
	SPI1/I2S1	—	
	FWDGT	—	
	WWDGT	—	
	RTC	—	
	TIMER5	—	
	TIMER4	—	
	TIMER3	—	
	TIMER2	—	
	TIMER1	—	
APB2	USART5	—	
	USART0	—	
	SPI0	—	
	TIMER0	—	
	ADC1(3)	—	
	ADC0(3)	—	
	GPIOE	—	
	GPIOD	—	
	GPIOC	—	
	GPIOB	—	
	GPIOA	—	
	EXTI	—	
	AFIO	—	
AHB1	ENET	—	
	CRC	—	
	FMC	—	
	DMA1	—	
	DMA0	—	

(1) Based on characterization, not tested in production.

(2) DEN0 and DEN1 bits in the DAC_CTL register are set to 1, and the converted value set to 0x800.

(3) system clock = f_{HCLK} = 180 Mhz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, f_{ADCCLK} = f_{APB2}/2, ADON bit is set to 1.

(4) If there is no other description, then HXTAL = 25 MHz, system clock = f_{HCLK} = 180 MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}.

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-9. EMS characteristics*** [(1)], based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-9. EMS characteristics [(1)]

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C LQFP144, f_{HCLK} = 180 MHz conforms to IEC 61000-4-2	—
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = 25 °C LQFP144, f_{HCLK} = 180 MHz conforms to IEC 61000-4-4	—

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-10. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	—	—	—	V
		LVDT<2:0> = 000(falling edge)	—	—	—	
		LVDT<2:0> = 001(rising edge)	—	—	—	
		LVDT<2:0> = 001(falling edge)	—	—	—	
		LVDT<2:0> = 010(rising edge)	—	—	—	
		LVDT<2:0> = 010(falling edge)	—	—	—	
		LVDT<2:0> = 011(rising edge)	—	—	—	
		LVDT<2:0> = 011(falling edge)	—	—	—	
		LVDT<2:0> = 100(rising edge)	—	—	—	
		LVDT<2:0> = 100(falling edge)	—	—	—	
		LVDT<2:0> = 101(rising edge)	—	—	—	
		LVDT<2:0> = 101(falling edge)	—	—	—	
		LVDT<2:0> = 110(rising edge)	—	—	—	
		LVDT<2:0> = 110(falling edge)	—	—	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		LVDT<2:0> = 111(rising edge)	—	—	—	
		LVDT<2:0> = 111(falling edge)	—	—	—	
$V_{LVDhyst}$(2)	LVD hysteresis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	1.56	—	V
V_{PDR}(1)	Power down reset threshold	—	—	1.52	—	V
$V_{PDRhyst}$(2)	PDR hysteresis	—	—	40	—	mV
V_{BOR3}(2)	Brownout level 3 threshold	Falling edge	—	2.8	—	V
		Rising edge	—	2.9	—	V
V_{BOR2}(2)	Brownout level 2 threshold	Falling edge	—	2.5	—	V
		Rising edge	—	2.6	—	V
V_{BOR1}(2)	Brownout level 1 threshold	Falling edge	—	2.2	—	V
		Rising edge	—	2.3	—	V
$V_{BORhyst}$(2)	BOR hysteresis	—	—	100	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization	—	—	2.88	—	ms

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-11. ESD characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	—	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	—	V

(1) Based on characterization, not tested in production.

Table 4-12. Static latch-up characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	—	mA
	V_{supply} over voltage		—	—	—	V

(1) Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	4	8	32	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2)(3)	Recommended load capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	25	—	mA/V
$I_{DDHXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	—	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	2	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$(2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$(2)	OSCIN rise or fall time	—	—	—	10	ns
C_{IN}(2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$(2)	Duty cycle	—	40	—	60	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic

characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	V_{DD} = 3.3 V	—	32.768	—	kHz
C_{LXTAL}(2)(3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Ducy_{(LXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	Lower driving capability	—	4	—	μA/V
		Medium low driving capability	—	6	—	
		Medium high driving capability	—	12	—	
		Higher driving capability	—	18	—	
$I_{DDLXTAL}$(1)	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	—	0.7	—	μA
		LXTALDRI[1:0] = 01	—	0.8	—	
		LXTALDRI[1:0] = 10	—	1.2	—	
		LXTALDRI[1:0] = 11	—	1.5	—	
$t_{SULXTAL}$(1)(4)	Crystal or ceramic startup time	—	—	2	—	s

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on SC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$(2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$(2)	OSC32IN rise or fall time	—	—	—	50	
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$(2)	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-17. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C(1)	-2.5	—	+2.5	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C ~ +85 °C(1)	-1.8	—	+1.8	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
$Ducy_{IRC8M}$(2)	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC8M}$(1)	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V,	—	80	—	μA
$t_{SUIRC8M}$(1)	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V,	—	1.5	—	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-18. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}(1)	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	20	40	45	kHz
$I_{DDAIRC40K}$(2)	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz T_A = 25 °C	—	0.4	—	μA
$t_{SUIRC40K}$(2)	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz T_A = 25 °C	—	80	—	μs

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

Table 4-19. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C(1)	-4.0	—	+5.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C ~ +85 °C (1)	-3.0	—	+3.0	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-2.0	—	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.12	—	%
D_{IRC48M}(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC48M}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	—	—	μA
$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	—	—	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.9. PLL characteristics

Table 4-20. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	200	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	32	—	400	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 400 MHz	—	700	—	μA
I_{DD}(1)(3)	Current consumption on V_{DD}	VCO freq = 400 MHz	—	500	—	μA
$Jitter_{PLL}$(1)(4)	Cycle to cycle Jitter（rms）	System clock	—	40	—	ps
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) System clock = IRC8M = 8 MHz, PLL clock source = IRC8M/2 = 4 MHz, f_{PLLOUT} = 200 MHz.

(4) Value given with main PLL running.

Table 4-21. PLL1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	100	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	32	—	200	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)	Current consumption on V_{DDA}	VCO freq = 200 MHz	—	400	—	μA
I_{DD}(1)	Current consumption on V_{DD}	VCO freq = 200 MHz	—	250	—	μA
$Jitter_{PLL}$(1)	Cycle to cycle Jitter	—	—	40	—	ps

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-22. PLL2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	200	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	32	—	400	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1)	Current consumption on V_{DDA}	VCO freq = 200 MHz	—	700	—	μA
I_{DD}(1)	Current consumption on V_{DD}	VCO freq = 200 MHz	—	500	—	μA
$Jitter_{PLL}$(1)	Cycle to cycle Jitter	—	—	40	—	ps

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-23. PLLUSB characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	4	—	25	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	—	480	—	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	—	480	—	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DD}(1)	Current consumption on V_{DDA}	VCO freq = 480 MHz	—	2.5	—	mA
$Jitter_{PLL}$(1)	Cycle to cycle Jitter	—	—	40	—	ps

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.10. Memory characteristics

Table 4-24. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40 °C ~ +85 °C	10	—	—	kcycles
t_{RET}	Data retention time	—	10	—	—	years
t_{PROG}	Word programming time	T_A = -40 °C ~ +85 °C	—	37.5	—	μs
t_{ERASE}	Page erase time	T_A = -40 °C ~ +85 °C	—	11	—	ms
t_{MERASE}	Mass erase time	T_A = -40 °C ~ +85 °C	—	12	—	s

(1) Based on characterization, not tested in production.

Table 4-25. SIP PSRAM memory characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{SB_STDroom}$	Standby current (standard room temp)	T_A = +25 °C	—	40	μA
I_{SB}	Standby current	T_A = -40 °C ~ +85 °C	—	150	μA
I_{CC}	Operation current(standard room temp)	T_A = +25 °C	—	6	mA
$t_{CLK\ for\ read}$	For Read('h03) and Read ID('h9F) command	T_A = -40 °C ~ +85 °C	2	33	MHz
$t_{CLK\ for\ others}$	For command except read and read ID command	T_A = -40 °C ~ +85 °C	2	45	MHz
t_{RST}	Time between end of RST CMD to next valid CMD	T_A = -40 °C ~ +85 °C	50	—	ns

(1) Guaranteed by design, not tested in production.

(2) Need to configure specified pins to PSRAM functions respectively (PF0 to SQPI_D0, PF2 to SQPI_D2, PF4 to SQPI_D1, PF6 to SQPI_CSN, PF8 to SQPI_CLK and PF10 to SQPI_D3).

4.11. NRST pin characteristics

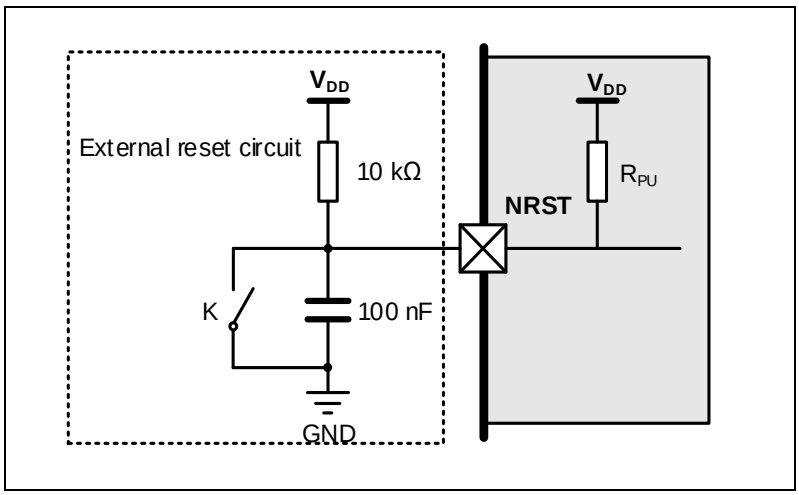
Table 4-26. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 1.71 V	—	—	—	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		—	—	—	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	—	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 2.5 V	—	—	—	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		—	—	—	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	—	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	—	—	—	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		—	—	—	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	—	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	—	—	—	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		—	—	—	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	—	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit



4.12. GPIO characteristics

Table 4-27. I/O port DC characteristics (1)(3)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage		1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	—	V
	5V-tolerant IO Low level input voltage		1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	—	V
V_{IH}	Standard IO Low level input voltage		1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	—	V
	5V-tolerant IO Low level input voltage		1.8 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	—	V
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 1.8V	—	—	—	V
			V_{DD} = 3.3 V	—	—	—	
			V_{DD} = 3.6V	—	—	—	
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 1.8V	—	—	—	V
			V_{DD} = 3.3 V	—	—	—	
			V_{DD} = 3.6V	—	—	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 1.8V	—	—	—	V
			V_{DD} = 3.3 V	—	—	—	
			V_{DD} = 3.6V	—	—	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 1.8V	—	—	—	V
			V_{DD} = 3.3 V	—	—	—	
			V_{DD} = 3.6V	—	—	—	
R_{PU}(2)	Internal pull-up resistor	All pins	—	—	—	—	kΩ
		PA10	—	—	—	—	
R_{PD}(2)	Internal pull-down resistor	All pins	—	—	—	—	kΩ
		PA10	—	—	—	—	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-28. I/O port AC characteristics (1)(2)

GPIOx_MDy[1:0] bit value(3)	Parameter	Conditions	Max	Unit
GPIOx_CTL->MDy[1:0]=10 （IO_Speed = 2MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	
GPIOx_CTL->MDy[1:0] = 01 （IO_Speed = 10MHz）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	
GPIOx_CTL->MDy[1:0]=11	Maximum	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	MHz

GPIOx_MDy[1:0] bit value(3)	Parameter	Conditions	Max	Unit
（IO_Speed = 50MHz）	frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	
GPIOx_CTL->MDy[1:0]=11 and GPIOx_SPDy=1 （IO_Speed = MAX）	Maximum frequency(4)	1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	—	MHz
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	—	
		1.8 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	—	

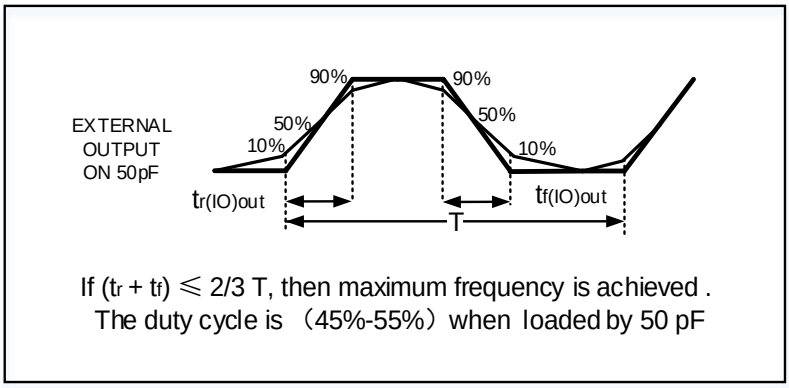
(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all test results given for T_A = 25 °C.

(3) The I/O speed is configured using the GPIOx_CTL -> MDy[1:0] bits. Refer to the GD32E50x user manual which is selected to set the GPIO port output speed.

(4) The maximum frequency is defined in ***Figure 4-5. I/O port AC characteristics definition***, and maximum frequency cannot exceed 180 MHz.

Figure 4-5. I/O port AC characteristics definition



4.13. Temperature sensor characteristics

Table 4-29. Temperature sensor characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	VSENSE linearity with temperature	—	—	—	°C
Avg_Slope	Average slope	—	—	—	mV/°C
V_{25}	Voltage at 25 °C	—	—	—	V
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	—	—	μs

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

4.14. ADC characteristics

Table 4-30. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	1.71	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REF+}	V
V_{REF+}(2)	Positive Reference Voltage	—	1.8	—	V_{DDA}	V
V_{REF-}(2)	Negative Reference	—	—	V_{SSA}	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Voltage					
f_{ADC}(1)	ADC clock	V_{DDA} = 1.71 V to 2.4 V	0.1	—	14	MHz
		V_{DDA} = 2.4 V to 3.6 V	0.1	—	35	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	2.86	MSPS
		10-bit	0.008	—	3.33	
		8-bit	0.01	—	4	
		6-bit	0.012	—	5	
V_{AIN}(1)	Analog input voltage	16 external; 2 internal	0	—	V_{DDA}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	37.73	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.55	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 40 MHz	—	3.275	—	μs
t_s(2)	Sampling time	f_{ADC} = 40 MHz	0.0375	—	5.99	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	14	—	1/f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}(2)	Startup time	—	—	—	1	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1:

R_{AIN} max formula $$R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-31. ADC R_{AIN} max for f_{ADC} = 35 MHz

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.0429	0.25
7.5	0.2143	3.46
13.5	0.3857	6.68
28.5	0.8143	14.71
41.5	1.1857	21.67
55.5	1.5857	29.16
71.5	2.0429	37.73
239.5	6.8429	N/A

Table 4-32. ADC dynamic accuracy at f_{ADC} = 14 MHz (1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 14 MHz	—	—	—	bits

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	—	—	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	—	—	
THD	Total harmonic distortion	Temperature = 25 °C	—	—	—	

(1) Based on characterization, not tested in production.

Table 4-33. ADC dynamic accuracy at f_{ADC} = 35 MHz (1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 35 MHz	—	—	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{REF+} = 3.3 V	—	—	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	—	—	
THD	Total harmonic distortion	Temperature = 25 °C	—	—	—	

(1) Based on characterization, not tested in production.

Table 4-34. ADC static accuracy at f_{ADC} = 14 MHz (1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 14 MHz V_{DDA} = V_{REF+} = 3.3 V	—	—	LSB
DNL	Differential linearity error		—	—	
INL	Integral linearity error		—	—	

(1) Based on characterization, not tested in production.

4.15. DAC characteristics

Table 4-35. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	1.8	3.3	3.6	V
V_{REF+}(2)	Positive Reference Voltage	—	1.8	—	V_{DDA}	V
V_{REF-}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
R_{LOAD}(2)	Load resistance	Resistive load with buffer ON	5	—	—	kΩ
Ro(2)	Impedance output with buffer OFF	—	—	—	15	kΩ
C_{LOAD}(2)	Load capacitance	No pin/pad capacitance included	—	—	50	pF
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	—	0.2	—	—	V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	—	—	—	V_{DDA}-0.2	V
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	—	—	0.5	—	mV
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	—	—	—	V_{DDA}-1LSB	V
I_{DDA}(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	—	400	—	uA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V	—	450	—	uA
$I_{DDVREF+}$(1)	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V	—	100	—	uA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V	—	150	—	uA
DNL(1)	Differential non-linearity error	DAC in 12-bit mode	—	—	±2	LSB
INL(1)	Integral non-linearity	DAC in 12-bit mode	—	—	±4	LSB
Offset(1)	Offset error	DAC in 12-bit mode	—	—	10	LSB
GE(1)	Gain error	DAC in 12-bit mode	—	—	0.5	%
$T_{setting}$(1)	Settling time	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	—	—	0.5	μs
T_{wakeup}(2)	Wakeup from off state	—	—	—	5	μs
Update rate(2)	Max frequency for a correct DAC_OUT change from code i to i±1LSBs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	—	—	4	MS/s
PSRR(2)	Power supply rejection	—	55	80	—	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	ratio (to V_{DDA})					

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.16. I2C characteristics

Table 4-36. I2C characteristics (1)(2)(3)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	2	—	0.8	—	0.1	—	ns
$t_{h(SDA)}$	SDA data hold time	—	250	—	250	—	130	—	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	20	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	4	300	4	300	4	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs

(1) Guaranteed by design, not tested in production.
(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz, To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.
(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

4.17. SPI characteristics

Table 4-37. Standard SPI characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	22.5	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 90 MHz, presc = 8	43.94	44.44	44.94	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 90 MHz, presc = 8	43.94	44.44	44.94	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	5	6	ns
$t_{H(MO)}$	Data output hold time	—	3	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns

SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	5	—	9	ns
$t_{DIS(SO)}$	Data output disable time	—	6	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	10	12	ns
$t_{H(SO)}$	Data output hold time	—	8	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Based on characterization, not tested in production.

4.18. I2S characteristics

Table 4-38. I2S characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	3.075	3.077	3.079	MHz
		Slave mode	0	—	10	
t_H	Clock high time	—	162	—	—	ns
t_L	Clock low time		163	—	—	ns
$t_{V(WS)}$	WS valid time	Master mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Master mode	0	—	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	2	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	1	—	—	ns
$t_{su(SD_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD_SR)}$		Slave receiver	1	—	—	ns
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	12	ns
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7	—	—	ns
$t_{v(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	6	ns
$t_{h(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	2	—	—	ns

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production

4.19. USART characteristics

Table 4-39. USART characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 180 MHz	—	—	90	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 180 MHz	5	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 180 MHz	5	—	—	ns

(1) Guaranteed by design, not tested in production.

4.20. USBD characteristics

Table 4-40. USBD start up time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USBD startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 4-41. USBD DC electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels(1)	V_{DD}	USBFS operating voltage	—	3	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	1.3	—	2.0	
Output levels (2)	V_{OL}	Static output level low	R_L of 1.0 kΩ to 3.6 V	—	0.064	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	

(1) Guaranteed by design, not tested in production.

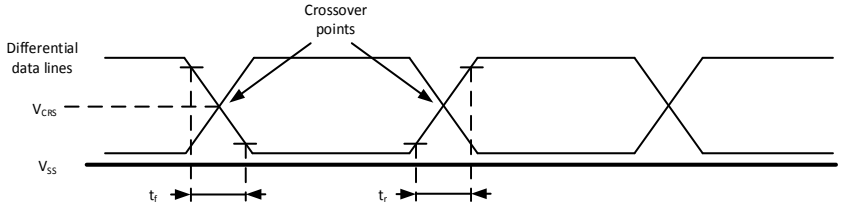
(2) Based on characterization, not tested in production.

Table 4-42. USBD full speed-electrical characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	CL = 50 pF	4	—	20	ns
t_F	Fall time	CL = 50 pF	4	—	20	ns
t_{RFM}	Rise/ fall time matching	t_R / t_F	90	—	110	%
V_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Guaranteed by design, not tested in production.

Figure 4-6. USBD timings: definition of data signal rise and fall time



4.21. EXMC characteristics

Table 4-43. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	27	29	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	27	29	ns
$t_{h(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{su(DATA_NE)}$	Data to EXMC_NEx high setup time	21.4	—	ns
$t_{su(DATA_NOE)}$	Data to EXMC_NOEx high setup time	21.4	—	ns
$t_{h(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.6	6.6	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: f_{HCLK} = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-44. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	15.8	17.8	ns
$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	4.6	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	4.6	6.6	ns
$t_{h(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	4.6	6.6	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.6	6.6	ns
$t_{h(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	10.2	—	ns
$t_{h(A_NWE)}$	Address hold time after EXMC_NWE high	4.6	—	ns
$t_{h(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	4.6	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	15.8	17.8	ns
$t_{v(DATA_NADV)}$	EXMC_NADV high to DATA valid	4.6	—	ns
$t_{h(DATA_NWE)}$	Data hold time after EXMC_NWE high	4.6	6.6	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: f_{HCLK} = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-45. Asynchronous multiplexed PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	38.2	40.2	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	15.8	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	21.4	23.4	ns
$t_{h(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(A_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{h(BL_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA_NE)}$	Data to EXMC_NEx high setup time	22.4	—	ns
$t_{su(DATA_NOE)}$	Data to EXMC_NOEx high setup time	22.4	—	ns
$t_{h(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.6	6.6	ns
$T_{h(AD_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	4.6	6.6	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: f_{HCLK} = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-46. Asynchronous multiplexed PSRAM/NOR write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	27	29	ns
$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	7.3	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	15.8	17.8	ns
$t_{h(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	4.6	—	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	4.6	6.6	ns
$t_{h(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	4.6	—	ns
$t_{h(A_NWE)}$	Address hold time after EXMC_NWE high	4.6	—	ns
$t_{h(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	4.6	—	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA_NADV)}$	EXMC_NADV high to DATA valid	4.6	—	ns
$t_{h(DATA_NWE)}$	Data hold time after EXMC_NWE high	4.6	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: f_{HCLK} = 180 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-47. Synchronous multiplexed PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	22.4	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	10.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	10.2	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	10.2	—	ns
$t_{d(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: f_{HCLK} = 180 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-48. Synchronous multiplexed PSRAM write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	22.4	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	10.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	10.2	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	10.2	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: f_{HCLK} = 180 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-49. Synchronous non-multiplexed PSRAM/NOR read timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	22.4	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	10.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	10.2	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	10.2	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: HCLK=180 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-50. Synchronous non-multiplexed PSRAM write timings (1)(2)(3)(4)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	22.4	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	10.2	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	10.2	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	10.2	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on characterization, not tested in production.
(4) Based on configure: HCLK = 180 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.22. Serial/Quad Parallel Interface (SQPI) characteristics

Table 4-51.SQPI characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}(2)	CLK period	11.0(4)	—	—	ns
t_{CD}(2)	CLK high level duty for even clock divided	45	50	55	%
	CLK high level duty for odd clock divided	45	—	71	
t_{KHKL}(3)	CLK rise or fall time	—	—		ns
t_{CPH}(2)	CE# high between subsequent burst operations	22.2	—	—	ns
t_{CEM}(2)	CE# low pulse width	88.8	—	—	ns
t_{CSP}(2)	CE# setup time to CLK rising edge	5.5	—	177.7	ns
t_{CHD}(2)	CE# hold time from CLK rising edge	5.5	—	177.7	ns
t_{SP}(2)	Setup time to active CLK edge	5.5	—	177.7	ns
t_{HD}(2)	Hold time from active CLK edge	5.5	—	177.7	ns
t_{HZ}(2)	CE# rise to data output high-Z	—	0	—	ns
t_{ACLK}(2)	CLK fall to data output valid delay	—	0	—	ns
t_{KOH}(2)	Data hold time from CLK falling edge	—	0	—	ns

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Output driven mode is 50 MHz.
(4) This is designed minimal period. The operating minimal clock period is 22.2 ns(45 MHz = 180 MHz/4).

4.23. TIMER characteristics

Table 4-52. TIMER characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	5.6	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$/2	MHz
		$f_{TIMERxCLK}$ = 180 MHz	0	90	MHz
RES	Timer resolution	TIMERx (except TIMER1)	—	16	bit
		TIMER1	—	32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	0.0056	367	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	—	24.1	s

(1) Guaranteed by design, not tested in production.

4.24. WDGT characteristics

Table 4-53. FWDGT min/max timeout period at 40 kHz (IRC40K) (1)

Prescaler divider	PR[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.1	409.6	ms
1/8	001	0.2	819.2	
1/16	010	0.4	1638.4	
1/32	011	0.8	3276.8	
1/64	100	1.6	6553.6	
1/128	101	3.2	13107.2	
1/256	110 or 111	6.4	26214.4	

(1) Guaranteed by design, not tested in production.

Table 4-54. WWDGT min-max timeout value at 90 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	45.5	µs	2.91	ms
1/2	01	91.0		5.83	
1/4	10	182.0		11.65	
1/8	11	364.1		23.30	

(1) Guaranteed by design, not tested in production.

4.25. Parameter condition

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C.

5. Package information

5.1. LQFP100 package outline dimensions

Figure 5-1. LQFP100 package outline

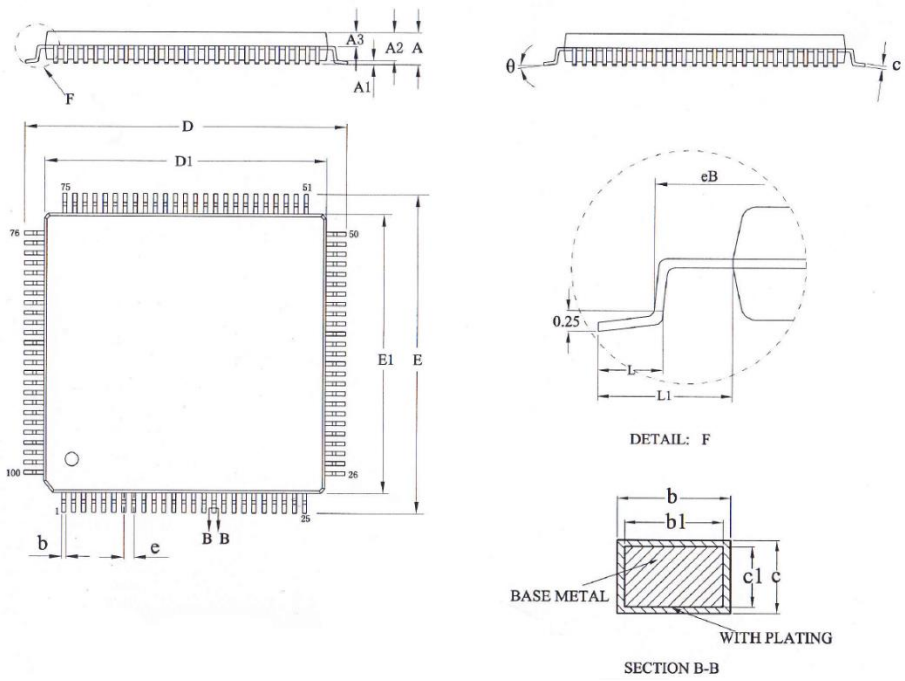


Table 5-1. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
D	15.80	16.0	16.20
D1	13.90	14.0	14.10
E	15.80	16.0	16.20
E1	13.90	14.0	14.10
θ	0°	3.5°	7°
c	0.13	—	0.17
c1	0.12	0.13	0.14
L	0.45	0.6	0.75
L1	—	1.0 REF	—
b	0.18	0.20	0.26
b1	0.17	0.20	0.23
eB	15.05	—	15.35
e	—	0.50 BSC	—

(Original dimensions are in millimeters)

5.2. LQFP64 package outline dimensions

Figure 5-2. LQFP64 package outline

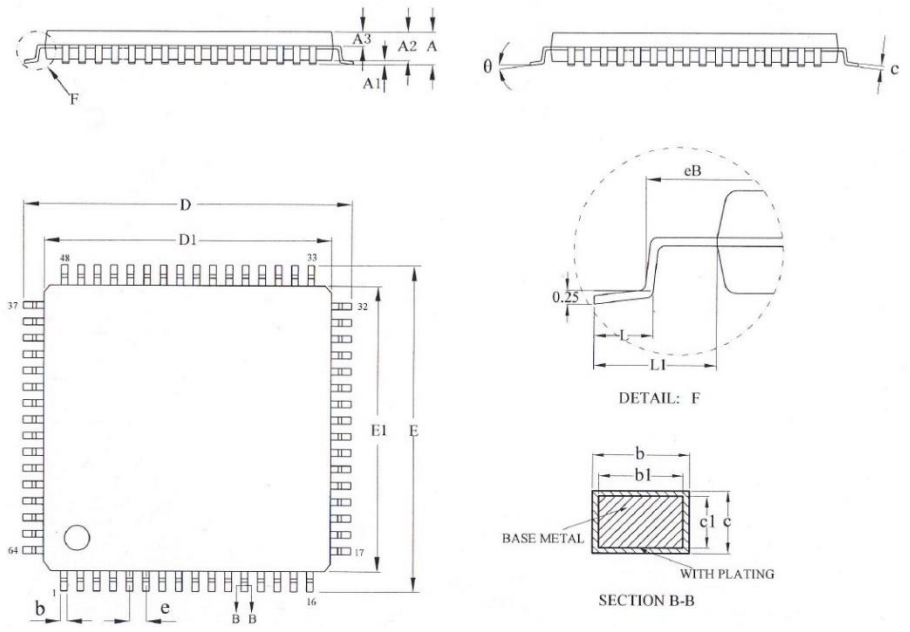


Table 5-2. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
θ	0°	3.5°	7°
c	0.13	—	0.17
L	0.45	0.60	0.75
L1	—	1.00 REF	—
b	0.17	0.20	0.27
e	—	0.50 BSC	—
eB	11.25	—	11.45

(Original dimensions are in millimeters)

6. Ordering information

Table 6-1. Part ordering code for GD32EPRTxx devices

Ordering code	Flash	SRAM	Package	Package type	Temperature operating range
GD32EPRTRDT6	384 KB	96 KB + 4 MB PSRAM	LQFP64	Green	Industrial -40°C to +85°C
GD32EPRTVDT6	384 KB	96 KB + 4 MB PSRAM	LQFP100	Green	Industrial -40°C to +85°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.17, 2020

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