



# TF0215/16

## High Speed, Low-Side, Single Gate Driver

### Features

- Efficient, low-cost solution for driving MOSFETs and IGBTs
- Wide supply voltage operating range: 4.5V to 18V
- 1.9A source / 1.8A sink output current capability
- Inverting and non-inverting input configurations
- Undervoltage lockout for  $V_{CC}$  supply.
- Fast propagation delays (35ns typical)
- Fast rise and fall times (15ns typical)
- Logic input (IN) 3.3V capability
- Space saving SOT23-5L package
- Extended temperature range: -40°C to +125°C

### Applications

- Switch mode power supplies
- Motor Drive
- Line Drivers
- DC-DC Converters



SOT-23-5L

### Description

The TF0215/16 high speed, low side MOSFET and IGBT drivers are capable of driving 1.9A of peak current. The TF0215/16 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. Internal undervoltage lockout (UVLO) will protect MOSFET with loss of supply by turning off the output when  $V_{CC}$  falls below operating range. Fast and well matched propagation delays allow high speed operation, enabling a smaller, more compact power switching design using smaller associated components.

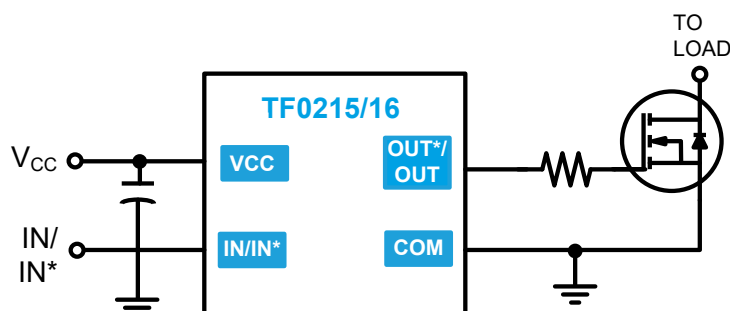
These devices are highly resistant to noise by being able to withstand up to 5V positive or negative on the ground pin without damage. Also they can accept 500mA of reverse current forced back into its outputs without damage or logic change. The TF0215 provides an inverted output and the TF0216 provides a noninverting output. The TF0215/16 comes in a space-saving SOT23-5L package and it operates over an extended -40 °C to +125 °C temperature range.

### Ordering Information

Year Year Week Week

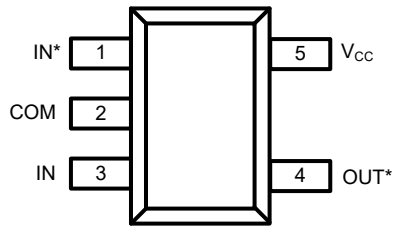
PART NUMBER	PACKAGE	PACK / Qty	MARK
TF0215-USQ	SOT-23-5L	T&R / 3,000	T0215/16
TF0216-USQ	SOT-23-5L	T&R / 3,000	YYWW

### Typical Application



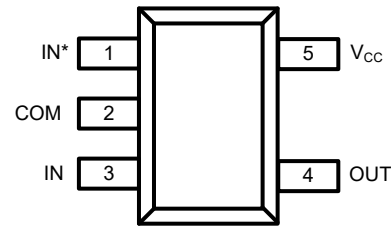


**Pin Diagrams**



TF0215

**Top View: SOT23-5L**

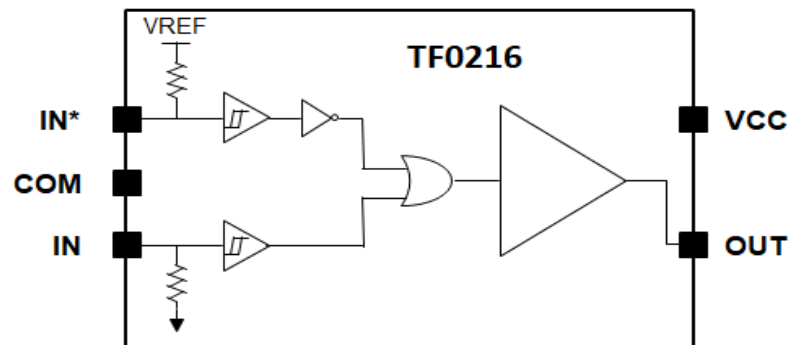
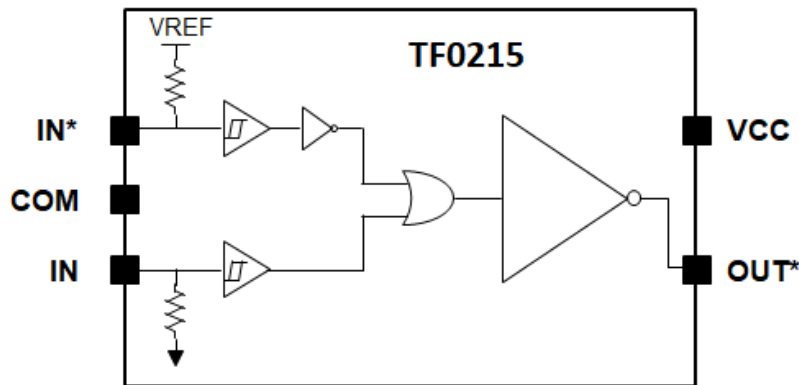


TF0216

**Pin Descriptions**

PIN NAME	PIN NUMBER	PIN DESCRIPTION
IN*	1	Logic input, in phase with OUT* (TF0215), out of phase with OUT (TF0216), leave open when not in use.
COM	2	Supply return
IN	3	Logic input, out of phase with OUT* (TF0215), in phase with OUT (TF0216), leave open when not in use.
OUT*/OUT	4	Gate drive output
V <sub>CC</sub>	5	Supply input

**Functional Block Diagram**





## Absolute Maximum Ratings (NOTE1)

$V_{CC}$ - Low-side fixed supply voltage.....	-0.3V to +22V
$V_{OUT}$ - Output voltage (OUT/OUT*).....	-0.3V to $V_{CC}$ +0.3V
$V_{IN}$ - Logic input voltage (IN).....	-5V to $V_{CC}$ +0.3V
ESD Protection on all pins.....	2kV (HBM) 400V (MM)

**NOTE1** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$P_D$ - Package power dissipation at $T_A \leq 25^\circ\text{C}$	
SOT23-5L.....	TBD
SOT23-5L Thermal Resistance <b>(NOTE2)</b>	
$\theta_{JA}$ .....	TBD $^\circ\text{C}/\text{W}$
$\theta_{JC}$ .....	TBD $^\circ\text{C}/\text{W}$
$T_J$ - Junction operating temperature.....	+150 $^\circ\text{C}$
$T_L$ - Lead Temperature (soldering, 10 seconds).....	+300 $^\circ\text{C}$
$T_{stg}$ - Storage temperature .....	-55 to 150 $^\circ\text{C}$

**NOTE2** When mounted on a standard JEDEC 2-layer FR-4 board.

## Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
$V_{CC}$	Supply voltage	4.5	18	V
$V_{OUT}$	Output voltage (OUT/OUT*)	0	$V_{CC}$	V
$V_{IN}$	Logic input voltage (IN)	0	5	V
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$



## Electrical Characteristics (NOTE3)

$V_{BIAS}$  (4.5V <  $V_{CC}$  < 18V),  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
<b>DC Characteristics</b>						
$V_{IH}$	Logic "1" input voltage		2.4	1.6		V
$V_{IL}$	Logic "0" input voltage			1.3	0.8	
$I_{IN+}$	Logic "1" input bias current	$V_{IN} = 3V, V_{IN*} = 0V$			5	$\mu\text{A}$
$I_{IN-}$	Logic "0" input bias current	$V_{IN} = 0V, V_{IN*} = 3V$			2	
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$			25		mV
$V_{OL}$	Low level output voltage			25		
$I_{CCQ}$	$V_{CC}$ quiescent supply current	$V_{IN} = 0V$ or $3V$		50	100	$\mu\text{A}$
$I_{O+}$	Output high short circuit pulsed current	$V_{CC} = 12V$		1.9		A
$I_{O-}$	Output low short circuit pulsed current	$V_{CC} = 12V$		1.8		
$R_{OH}$	Output Resistance, High	$I_{OUT} = 10\text{mA}, V_{CC} = 12V$		3.3		$\Omega$
$R_{OL}$	Output Resistance, Low	$I_{OUT} = 10\text{mA}, V_{CC} = 12V$		2.3		$\Omega$
<b>Switching Characteristics</b>						
$t_r$	Turn-on rise time	$C_L = 1000\text{pF}, V_{CC} = 12V$		15	25	ns
$t_f$	Turn-off fall time	$C_L = 1000\text{pF}, V_{CC} = 12V$		15	25	ns
$t_{on}$	Turn-on propagation delay	$V_{CC} = 12V$		35	50	ns
$t_{off}$	Turn-off propagation delay	$V_{CC} = 12V$		35	55	ns

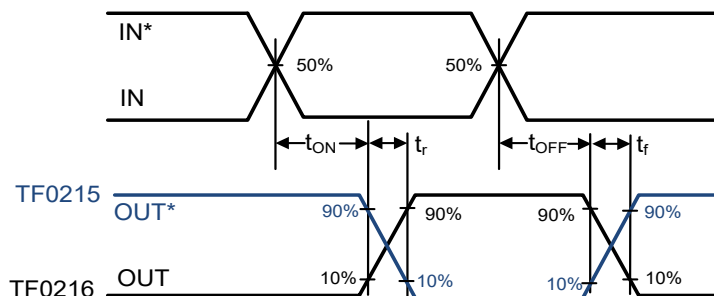
**NOTE3** The  $V_{IN}$  and  $I_{IN}$  parameters are applicable to the logic input pin: IN. The  $V_O$  and  $I_O$  parameters are applicable to the output pins: OUT and OUT\*



## Electrical Characteristics (over operating temperature range)

$V_{BIAS}$  (4.5V <  $V_{CC}$  < 18V),  $-40^{\circ}\text{C} < T_C < 125^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
<b>DC Characteristics</b>						
$V_{IH}$	Logic "1" input voltage		2.4			V
$V_{IL}$	Logic "0" input voltage				0.8	
$I_{IN+}$	Logic "1" input bias current	$V_{IN} = 3\text{V}$			10	$\mu\text{A}$
$I_{IN-}$	Logic "0" input bias current	$V_{IN} = 0\text{V}$		0	5	
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$			25		mV
$V_{OL}$	Low level output voltage			25		
$I_{CCQ}$	$V_{CC}$ quiescent supply current	$V_{IN} = 0\text{V}$ or $3\text{V}$		0.1	0.2	mA
$R_{OH}$	Output Resistance, High	$I_{OUT} = 10\text{mA}$ , $V_{CC} = 12\text{V}$			10	$\Omega$
$R_{OL}$	Output Resistance, Low	$I_{OUT} = 10\text{mA}$ , $V_{CC} = 12\text{V}$			7	$\Omega$
<b>Switching Characteristics</b>						
$t_r$	Turn-on rise time	$C_L = 1000\text{pF}$ , $V_{CC} = 12\text{V}$		30	40	ns
$t_f$	Turn-off fall time	$C_L = 1000\text{pF}$ , $V_{CC} = 12\text{V}$		30	40	ns
$t_{on}$	Turn-on propagation delay	$V_{CC} = 12\text{V}$		45	55	ns
$t_{off}$	Turn-off propagation delay	$V_{CC} = 12\text{V}$		50	60	ns



**Figure 1.** Switching Time Waveform Definitions

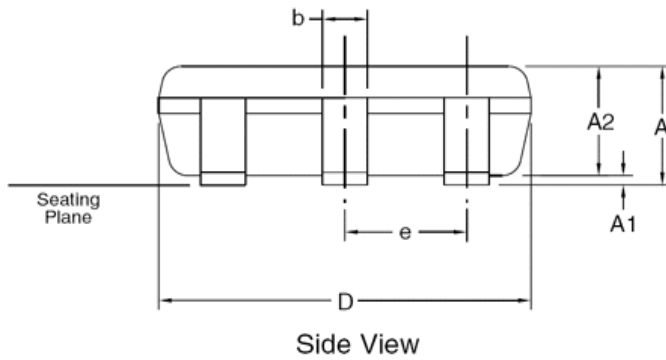
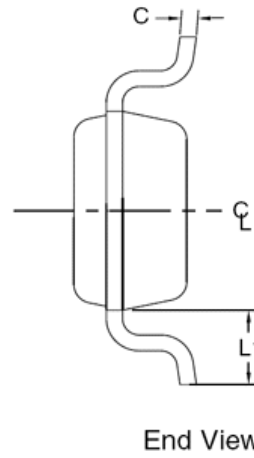
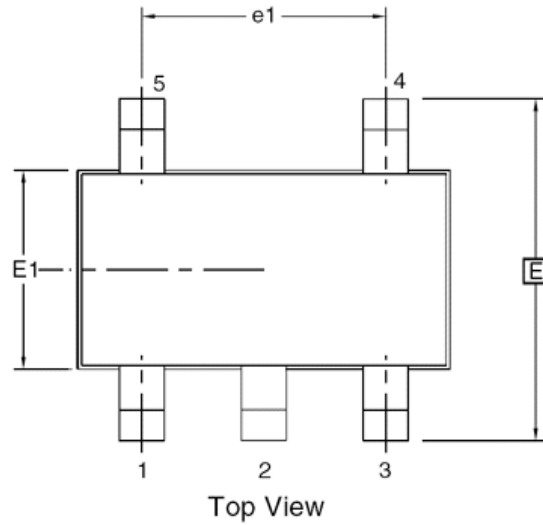
## Input/Output response table

Input pin	Input logic	TF0215 (OUT*)	TF0216 (OUT)
IN	H	L	H
IN	L	H	L
IN*	H	H	L
IN*	L	L	H



**Package Dimensions (SOT23-5L)**

Please contact support@tfsemi.com for package availability.



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.10	
A1	0.00	-	0.10	
A2	0.70	0.90	1.00	
c	0.08	-	0.20	4
D	2.90 BSC			2, 3
E	2.80 BSC			2, 3
E1	1.60 BSC			2, 3
L1	0.60 REF			
e	0.95 BSC			
e1	1.90 BSC			
b	0.30	-	0.50	4, 5



## Revision History

Rev.	Change	Owner	Date
1.0	First release	Keith Spaulding	6/21/2017
1.1	Specs adjusted from pre production testing	Keith Spaulding	2/8/2018
1.2	Add Order Information	Duke Walton	12/15/2020

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