Current Mode PWM Controller

Features

- Low Start up Ciarent
- Maximum Duty Chmp
- UVLO With Hysteresis
- 384xA Operating Frequency up to 300KHz
- 384xAM Openting Frequency iq> to 500KHz

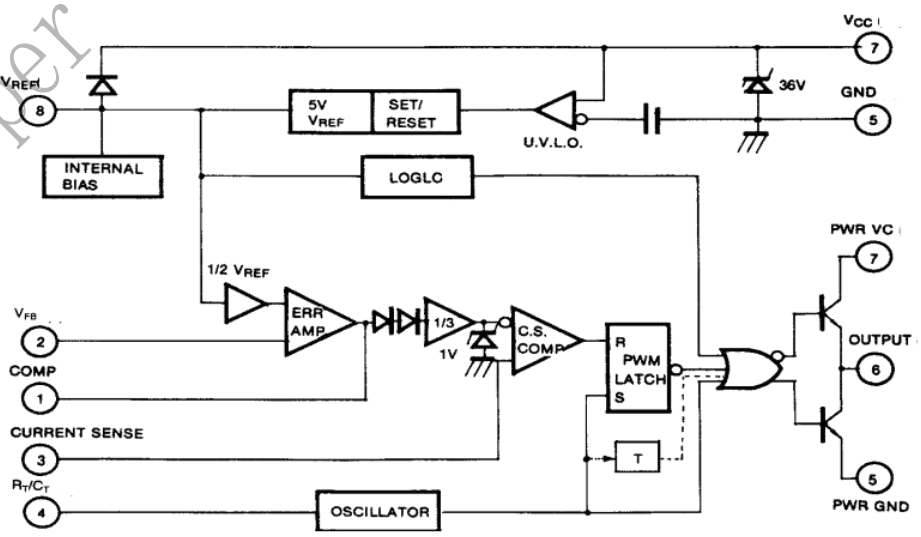
Description

The DP3842/DP3843/DP3844/DP3845 are fixed frequencycurrent-mode PWM controller. They are specially designed for Off-Line and DC to DC converter applications with minimum external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference,high gain errorr amplifier, current sensing comparator and a high current totempole output for driving a Power MOSFET.The The DP3842 and DP3844 have UVLO thresholds of 16V(on) and 10V(off).The DP3843 and DP3845 are 8.4V(on) and 7.6(off).The DP3842 and DP3843 can operate within 100% duty cycle.The DP3844 and DP3845 operate with 50% duty cycle

Ordering Information

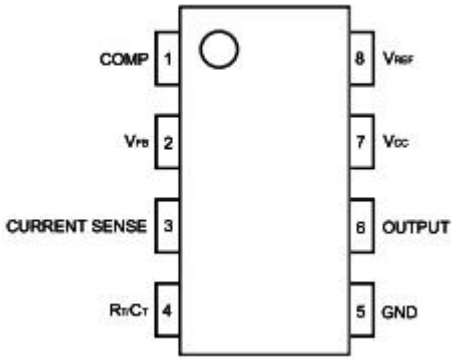
封装	描述
DP384X	SOP8, Halogen free,4000Pcs/Reel
	DIP8, Pb free, 50Pcs/Tube

TYPICAL APPLICATION CIRCUIT



Product description

➢ Pin Arrangement



DOP8/DIP8

➢ Marking Information

UC184XA is the first line of silk screen name of the product：

DPXXXXXX： DP is DeveloPer The first X reresents the last year,2014 is 4; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said; The last two X represents the wafer batch code.

➢ Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	VCC	30	V
Output Current	IO	±1	A
Analog Inputs(Pin 2.3)	$V_{(ANA)}$	-3 to 5.5	V
Error Amp Output Sink Current	I_{SINK}(E.A)	10	mA
Power Dissipation at TA≤25℃（DIP8）	P_D(Note1,2)	-	mW
Power Dissipation at TA≤25℃（SOP8）	P_D(Note1,2)	-	mW
Power Dissipation at TA≤25℃（SOP8）	P_D(Note1,2)	-	mW
Storage Temperature Range	T_{STG}	- 60~ +150	°C
Lead temperature(Solsering,10sec)	T_{LEAD}	+260	°C
Thermal Resistance Junction-ambient(DIP8)	Rthj-amb(MAX)	100	°C/W
Thermal Resistance Junction-ambient(SOP8)	Rthj-amb(MAX)	265	°C/W

Note：

1. Board Thickness 1.6mm,Board Dimension 76.2mm*114.3mm,(Reference EIA/JSED51-3,51-7)
2. Do not exceeed PD and SOA (Safe Operation Area)

Electrical Characteristics (VCC=15V,RT=3.3nF,TA=0°Cto70°C,unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE SECTION						
REFERENCE Output Voltage	VREF	TJ=25°C,IREF=1mA	4.9	5	5.1	V
Line Regulation	△VREF	12V≤VCC≤25V		6	20	mV
Load Regulation	△VREF	1mA≤IREF≤20mA		6	25	mV
Short Circuit Output Current	IMAX	TA=25°C		-100	-180	mA
OSCILLATOR SECTION						
Oscillation Frequency	f	TJ=25℃	47	52	57	KHZ
Frequency Change With Voltage	△f/△VCC	12V≤VCC≤25V		0.05	1	%
Oscillator Amplitude	VOSC			1.6		Vp-p
ERROR AMPLIFIER SECTION						
Input Bias Current	IBIAS			-0.1	-2	uA
Input Voltage	VI(E＞A)	Vpin1=2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	GVO	2V≤VO≤4V(Note3)	65	90		dB
Power Supply Rejection Ratio	PSRR	12V≤VCC≤25V(Note3)	60	70		dB
Output Sink Current	ISINK	Vpin2=2.7V,Vpin1=2.1V	2	7		mA
Output Source Current	ISOUREC	Vpin2=2.3V,Vpin1=5V	-0.5	-1		mA
High Output Voltage	VOH	Vpin2=2.3V,RL=15KΩ to GND	5	6		V
Low Output Voltage	VOL	Vpin2=2.7V,RL=15KΩ to Pin 8		0.8	1.1	V
CURRENT SENSE SECTION						
Gain	GV	(Note1&2)	2.85	3	3.15	V/V
Maximum Input Signal	VI(MAX)	Vpin1=5V(Note1)	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	12V≤VCC≤25V(Note1,3)		70		dB
Input Bias Current	IBIAS			-3	-10	uA
OUTPUT SECTION						
Low Output Voltage	VOL	ISINK=20mA		0.08	0.4	V
		ISINK=200mA		1.4	2.2	V
High Output Voltage		ISOURCE=20mA	13	13.5		V
	VOH	ISOURCE=200mA	12	13		V
RiseTIme	tR	TJ=25℃,CL=1nF(Note3)		45	150	ns

Fall Time	tF	TJ=25℃,CL=1nF(Note3)		35	150	ns
UNDER-VOLTAGE LOCKOUT SECTION						
	VTH(ST)	DP3842/DP3844	14.5	16	17.5	V
		DP3843/DP3845	7.8	8.4	9	V
Min Operating Voltage (After Turn On)		DP3842/DP3844	7.5	10	11.5	V
		DP3843/DP3845	7	7.6	8.2	V

Electrical Characteristics (Continued)

(VCC=15V,RT=10KΩ,CT=3.3nF,TA=0°Cto70°C,unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWMSECTION						
Max Duty Cycle	D(MAX)	DP3842/DP3843	95	97	100	%
	D(MAX)	DP3844/DP3845	47	48	50	%
Min Duty Cycle	D(MIN)	12V≤VCC≤25V			0	%
TOTAL STANDBY CURRENT						
Start-UP Current	IST	TA=25°C		0.17	0.3	mA
Operating Supply Current	ICC(OPR)			14	17	mA
Zener Voltage	VZ		30	38		V

Adjust VCC above the stat threshould before setig at 15V

Note:

1. Parameter measured at trip point of latch
2. 2. Gain defined as:

$\mathbf{A} = \frac{\triangle \mathbf{Vpin1}}{\triangle \mathbf{Vpin3}}$,0 ≤Vpin3 ≤0.8V

3.These parameters,although guaranteed, are not 100 tested in production.

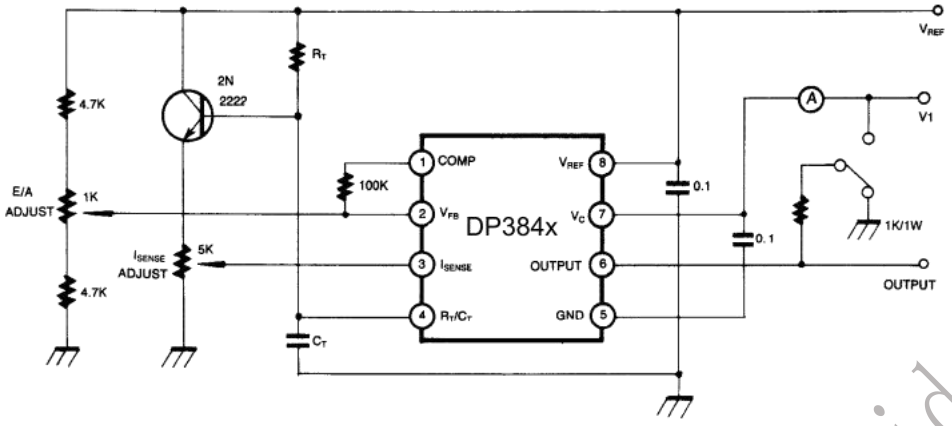


Figure 1. Open Loop Test Circuit

High peak currents associated with capacitive loads necessitate careful grounding techniques Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5kΩ potentiometer are used to samnle the oscillator waveform and apply an adjustable ramp to pin 3.

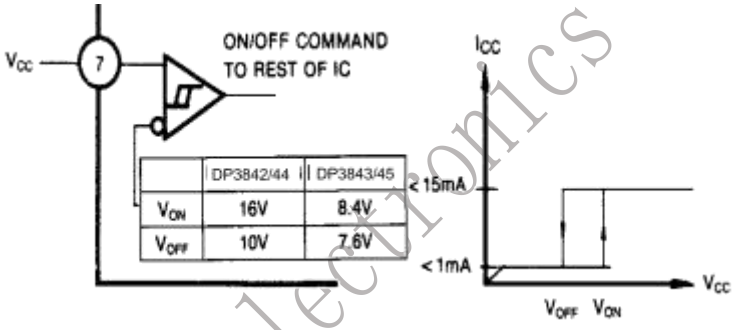


Figure 2. Under Voltage Lockout

During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

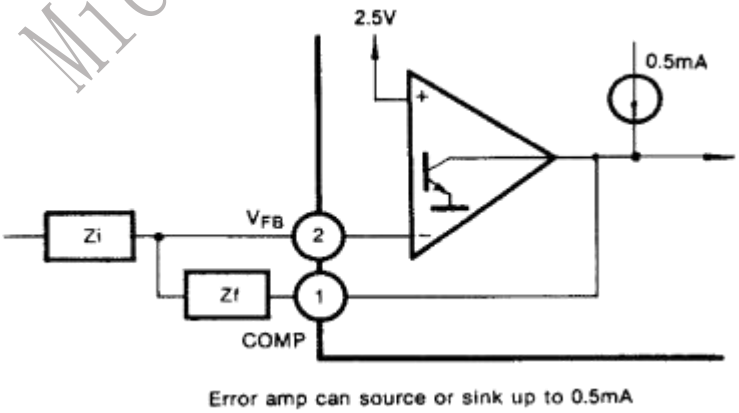


Figure 3. Error Amp Configuration

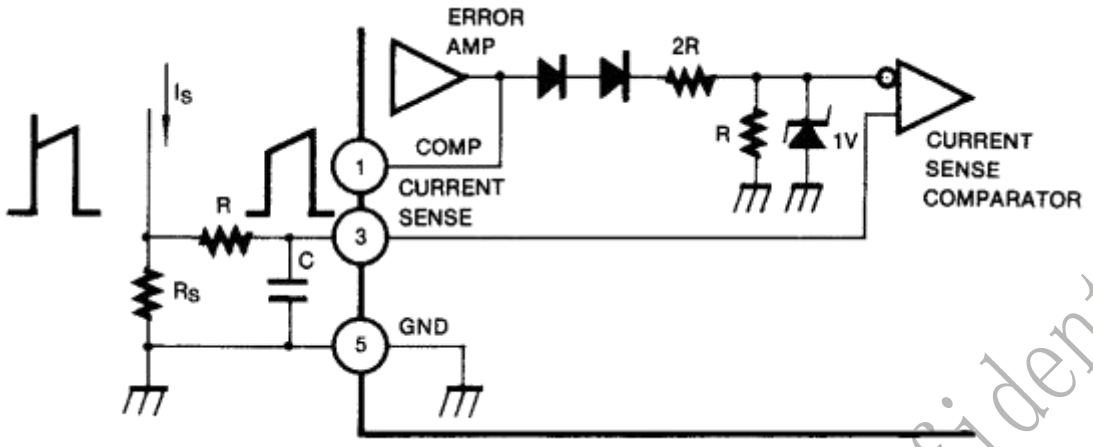


Figure 4. Current Sense Circuit

Peak current (Is) is determined by the formula:

$$IS(MAX) = \frac{1.0V}{RS}$$

A small RC filter may be required to suppress switch transients.

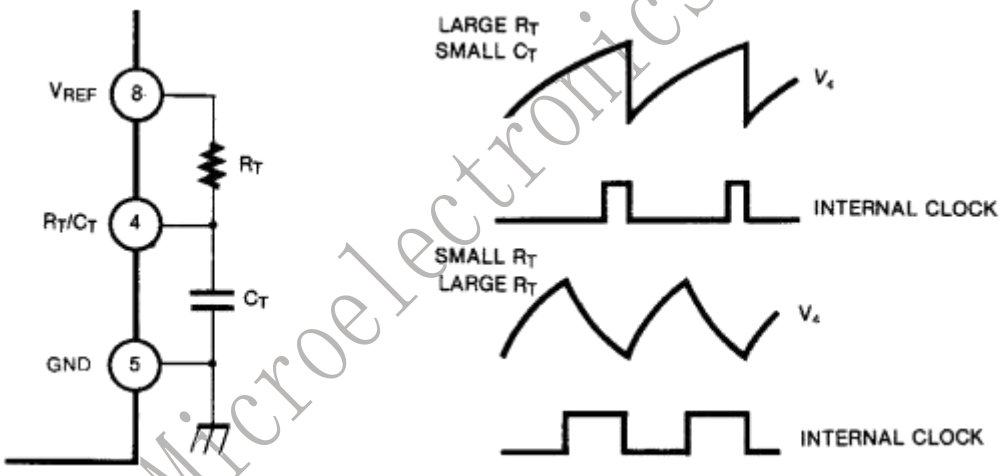


Figure 5. Oscillator Waveforms and Maximum Duty Cycle

Oscillator timing capacitor,CT,is charged by VREF through RRT and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of RT and CT therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas

$$Tc=0.55R_TC_T$$

$$T_d=RTCTIn\frac{0.0063RT-2.7}{0.0063RT-4}$$

Frequency, then, is:$f=(tc+td)^{-1}$

ForRT＞5KΩ，$f=\frac{1.8}{RTCT}$

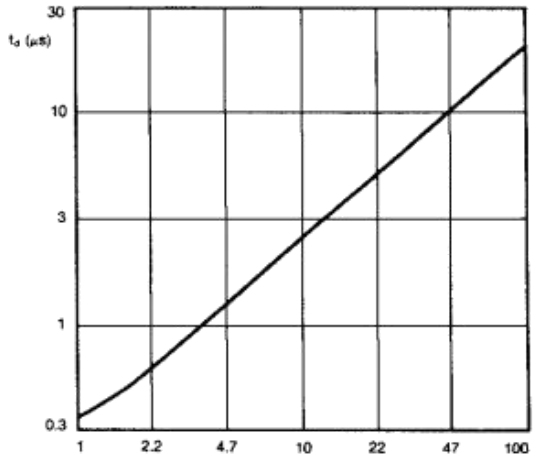


Figure 6. Oscillator Dead Time & Frequency

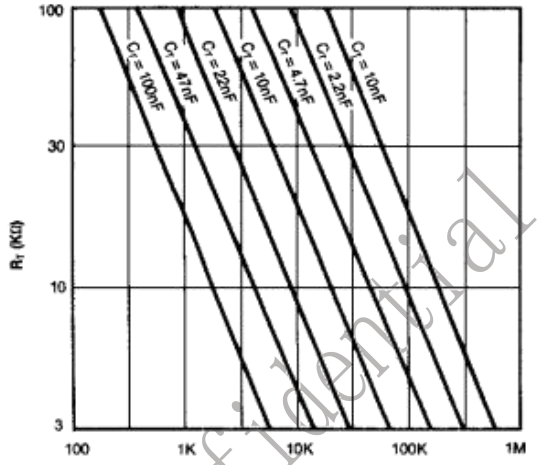


Figure 7.Timing Resistance vs Frequency

(Deadtime vs C_TR_T＞5KΩ)

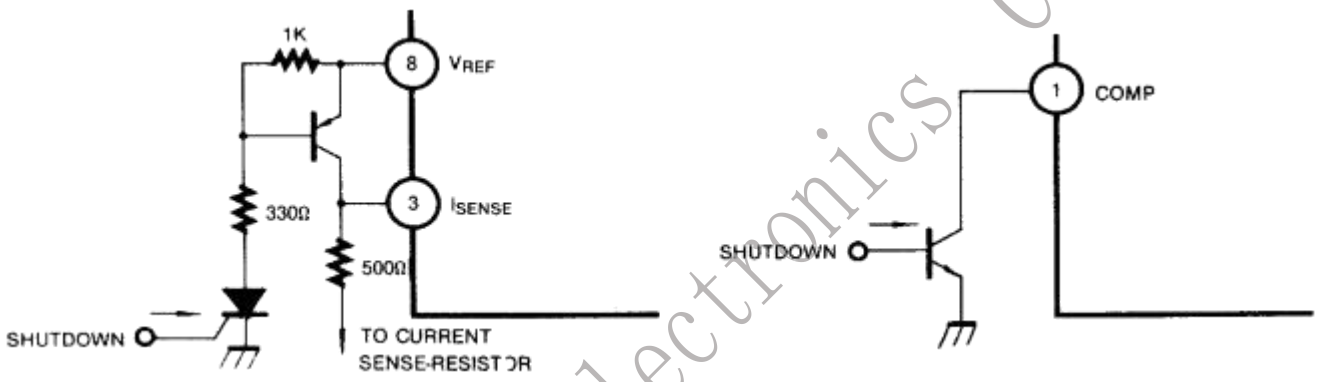


Figure 8. Shutdown Techniques

Shutdown of the DP3842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin1 below a voltage two diode drops above ground. Either method causes the output of tthe PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins l and/or 3 is removed.In one example,an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. Atthis point the reference turns off, allowing the SCR to reset.

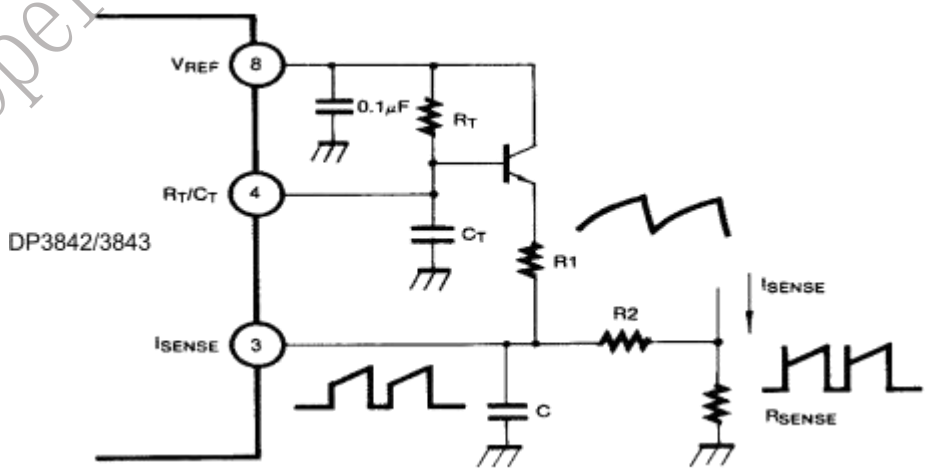


Figure 9. Slope Compensation

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor, CT, forms a filter with R2 to suppress the leading edge switch spikes.

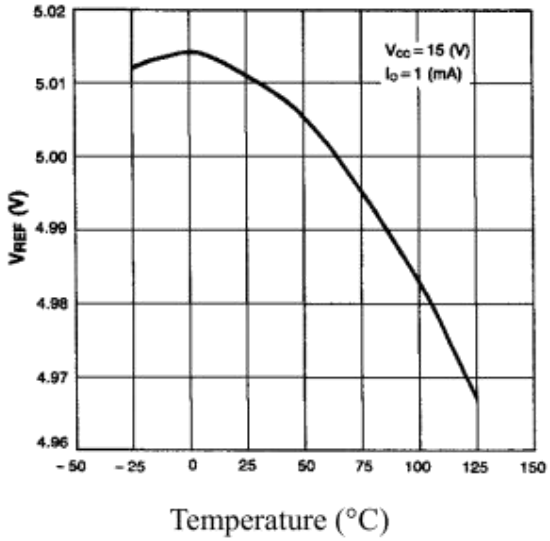


Figure 10. Temperature Drift (Vref)

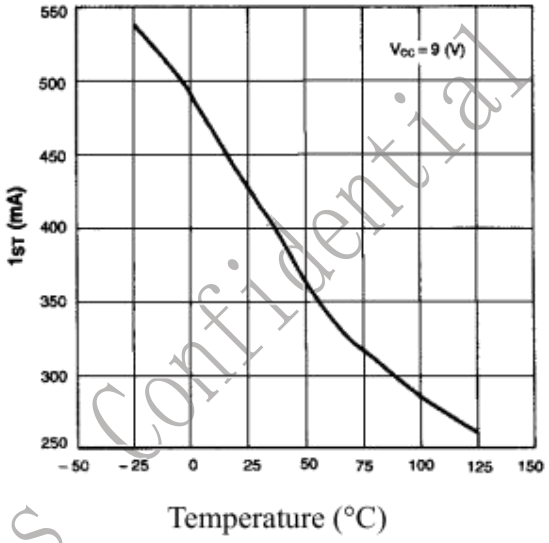


Figure 11. Temperature Drift (Ist)

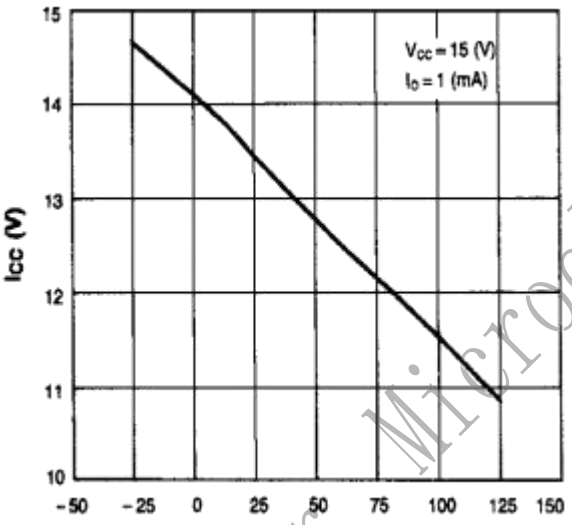
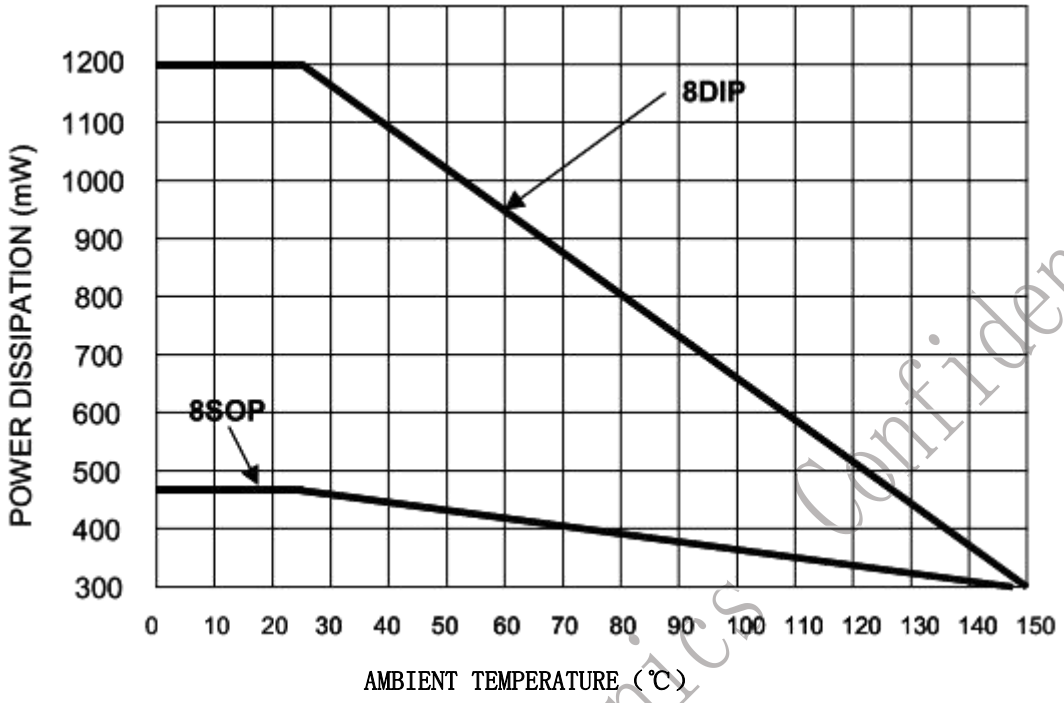


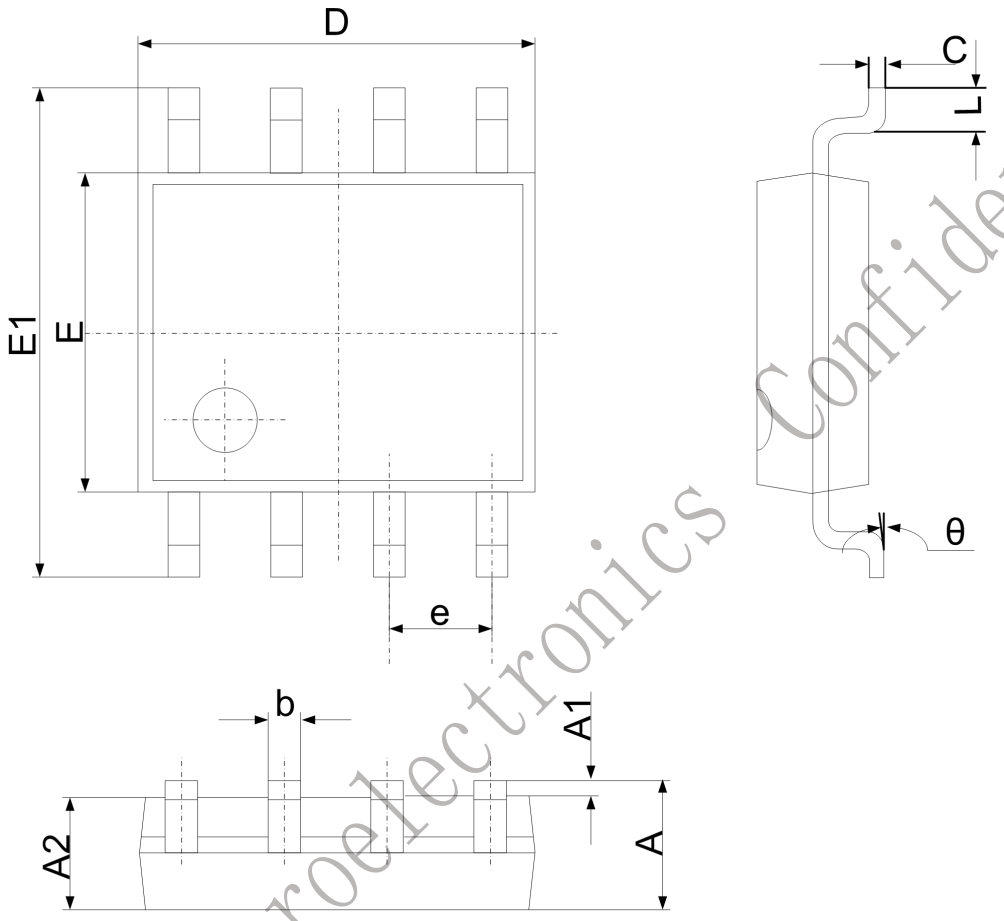
Figure 12.Temperature Drift (Icc)

Power Dissipation Curve



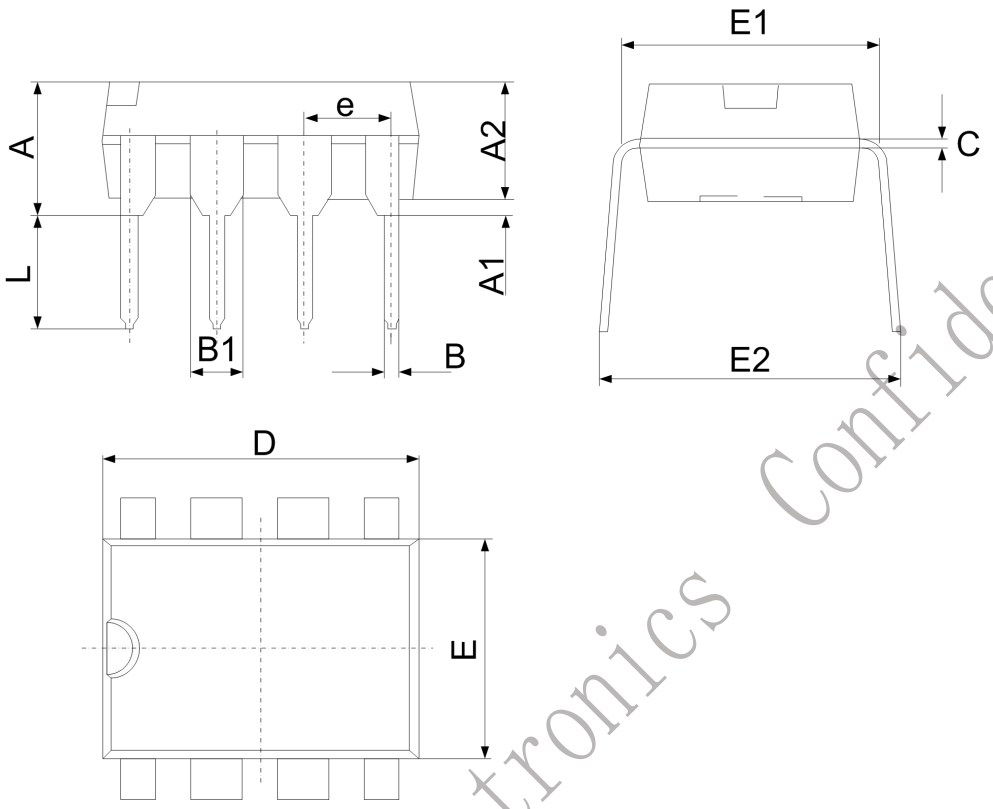
Package Dimension

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270（BSC）		0.050（BSC）	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（(BSC)）		0.060（(BSC)）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540（(BSC)）		0.100（(BSC)）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

Intellectual Property Declaration

If the contents disclosed in this specification relate to intellectual property rights, the company shall not make any warranty, express or implied, nor shall any third party use, copy or convert it, and compensate for any losses caused to the company.