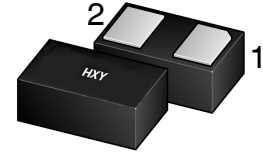




### Discription

The ESD8LL5.0C protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. Excellent clamping capability, low leakage, low capacitance, and fast response time provide best in class protection on designs that are exposed to ESD. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.



DFN1006-2L

### Specification Features:

- ★ Ultra Low Capacitance 0.35 pF
- ★ Low Clamping Voltage
- ★ Small Body Outline Dimensions:  
0.039" x 0.024" (1.00 mm x 0.60 mm)
- ★ Low Body Height: 0.020" (0.5 mm)
- ★ Stand-off Voltage: 5 V
- ★ Low Leakage
- ★ Response Time is Typically < 1.0 ns
- ★ IEC61000-4-2 Level 4 ESD Protection
- ★ This is a Pb-Free Device



Circuit Diagram

### Ordering information

Product ID	Pack	Qty(PCS)
ESD8LL5.0C	DFN1006-2L	10000

### Absolute Ratings (T<sub>amb</sub>=25°C )

Symbol	Parameter	Value	Units
P <sub>pp</sub>	Peak Pulse Power (t <sub>p</sub> = 8/20μs)	88	W
T <sub>L</sub>	Maximum lead temperature for soldering during 10s	260	°C
T <sub>stg</sub>	Storage Temperature Range	-55 to +150	°C
T <sub>op</sub>	Operating Temperature Range	-40 to +125	°C
T <sub>j</sub>	Maximum junction temperature	150	°C
	IEC61000-4-2 (ESD)	air discharge contact discharge	± 10 ± 15 KV



**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Device	$V_{RWM}$ (V)	$I_R$ ( $\mu\text{A}$ ) @ $V_{RWM}$	$V_{BR}$ (V) @ $I_T$ (Note 2)		$I_T$	C (pF)	$V_C$ (V) @ $I_{PP} = 1\text{ A}$ (Note 3)	$I_{PF}$ (A)	$P_{PK}$ (W)*	$V_C$
	Max	Max	Min	Max	mA	Max	Max	Max	Max	Per IEC61000-4-2 (Note 4)
ESD8LL5.0C	5.0	1.0	6.5	9.0	1.0	0.35	22	4	88	Figures 1 and 2 See Below

- $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .
- Surge current waveform per Figure 4.
- For test procedure see Figures 3.

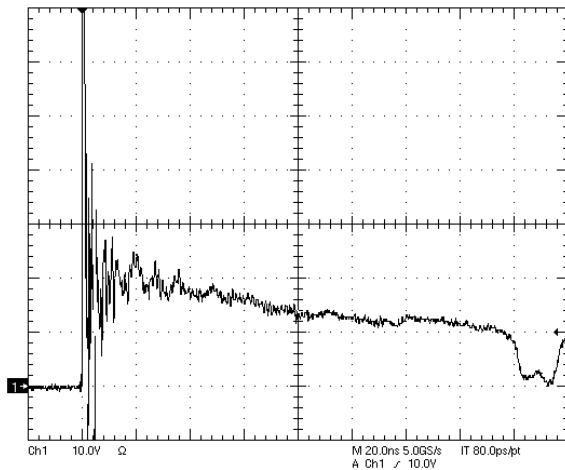


Figure 1. ESD Clamping Voltage Screenshot  
Positive 8 kV Contact per IEC61000-4-2

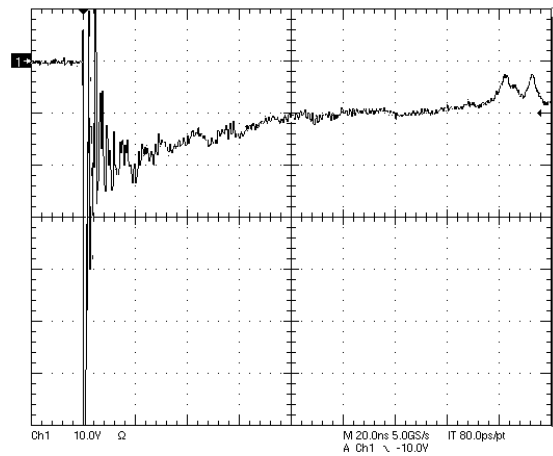


Figure 2. ESD Clamping Voltage Screenshot  
Negative 8 kV Contact per IEC61000-4-2



IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

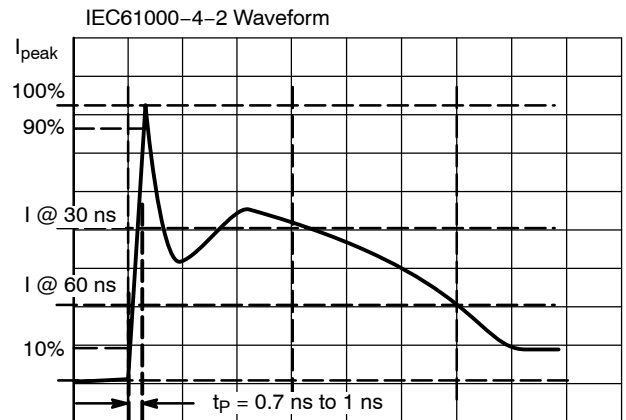


Figure 3. IEC61000-4-2 Spec

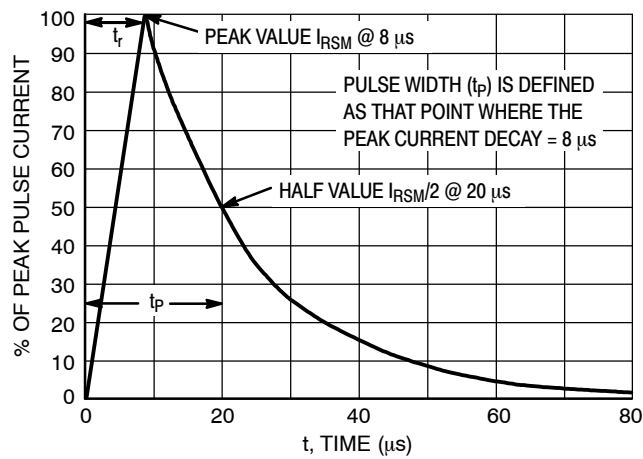
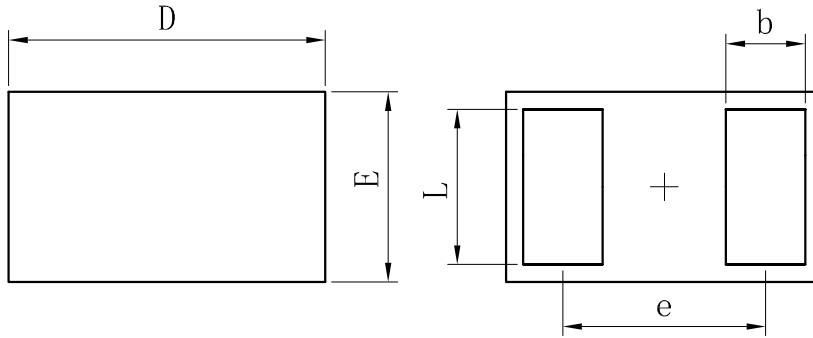


Figure 4. 8 X 20  $\mu$ s Pulse Waveform



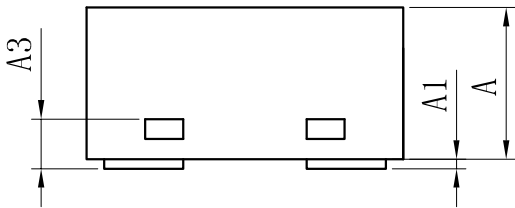
**OUTLINE AND DIMENSIONS**



TOP VIEW

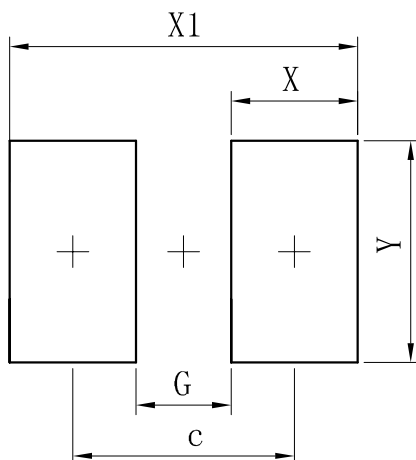
BOTTOM VIEW

DFN1006-2L			
Dim	Min	Typ	Max
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	-	0.64	-
L	0.44	0.49	0.54
b	0.20	0.25	0.30
A	0.43	0.48	0.53
A1	0	-	0.05
A3	0.127REF.		
All Dimensions in mm			



SIDE VIEW

**SOLDERING FOOTPRINT**



Dimensions	(mm)
c	0.70
G	0.30
X	0.40
X1	1.10
Y	0.70



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