

## 650V N-Channel Enhancement Mode MOSFET

### Description

The APJ47N65MP is generation super junction MOSFET family that is utilizing charge balance technology for extremely low on-resistance and low gate charge performance.

APJ47N65MP is suitable for applications which require superior power density and outstanding efficiency

### General Features

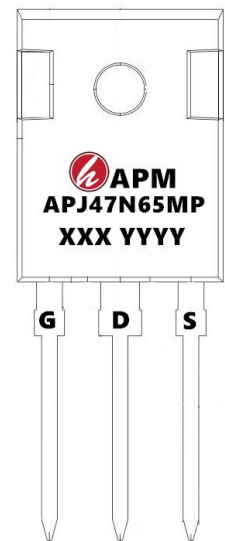
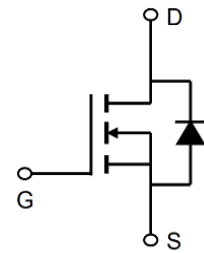
$V_{DS} = 650V$   $I_D = 47A$

$R_{DS(ON)} < 72m\Omega$  @  $V_{GS}=10V$  (Type: 60m $\Omega$ )

### Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APJ47N65MP	TO-247L	APJ47N65MP XXX YYYY	500

### Absolute Maximum Ratings ( $T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage ( $V_{GS} = 0V$ )	650	V
$I_D$	Continuous Drain Current	47	A
$I_{DM}$	Pulsed Drain Current (note1)	138	A
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy (note2)	1210	mJ
Dv/dt	MOSFET dv/dt ruggedness (@ $V_{DS} = 0\sim 400V$ )	25	V/ns
Dv/dt	Peak diode Recovery dv/dt (4)	15	V/ns
$P_D$	Power Dissipation ( $T_c = 25^{\circ}C$ )	3.34	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55~+150	$^{\circ}C$
$R_{thJC}$	Thermal Resistance, Junction-to-Case	0.33	$^{\circ}C/W$
$R_{thJA}$	Thermal Resistance, Junction-to-Ambient	40	$^{\circ}C/W$

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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

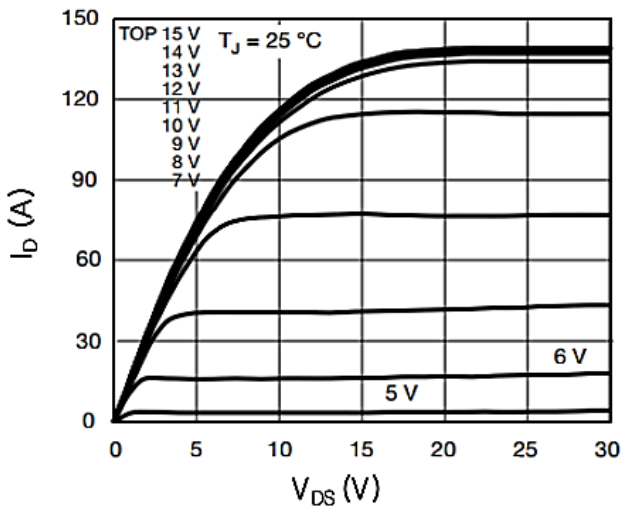
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	650	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown voltage temperature coefficient	I <sub>D</sub> =250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V	--	--	1	uA
		V <sub>DS</sub> =520V, T <sub>C</sub> =125°C	--	--	50	uA
IGSS	Gate to source leakage current, forward	V <sub>GS</sub> =30V, V <sub>DS</sub> =0V	--	--	100	nA
	Gate to source leakage current, reverse	V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	3	4	5	V
RDS(ON)	Drain to source on state resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =24A	--	60	72	mΩ
Rg	Gate resistance		--	1	--	Ω
Ciss	Input capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz	--	4655	--	pF
Coss	Output capacitance		--	185	--	
Crss	Reverse transfer capacitance		--	5.1	--	
td(on)	Turn on delay time	V <sub>DS</sub> =380V, I <sub>D</sub> =15A, R <sub>G</sub> =4.7Ω, V <sub>GS</sub> =10V	--	34	--	ns
tr	Rising time		--	31	--	
td(off)	Turn off delay time		--	80	--	
tf	Fall time		--	26	--	
Qg	Total gate charge	V <sub>DS</sub> =520V, V <sub>GS</sub> =10V, I <sub>D</sub> =24A	--	104	130	nC
Qgs	Gate-source charge		--	30	--	
Qgd	Gate-drain charge		--	34	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	47	A
ISM	Pulsed source current		--	--	138	A
VSD	Diode forward voltage drop.	I <sub>S</sub> =24A, V <sub>GS</sub> =0V	--	0.9	1.2	V
T <sub>rr</sub>	Reverse recovery time	I <sub>S</sub> =24A, V <sub>GS</sub> =0V, V <sub>DD</sub> =25, di <sub>F</sub> /dt=60A/us,	--	633	--	ns
Q <sub>rr</sub>	Reverse recovery Charge		--	8	--	uC

#### Note :

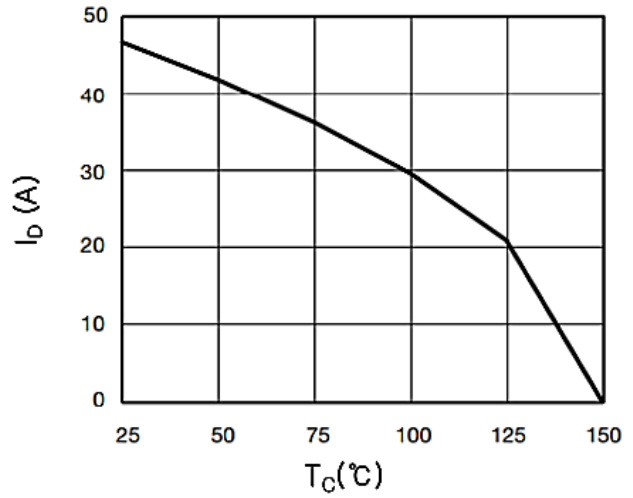
- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . L=20mH, IAS =11A, VDD =100, RG=25Ω
- 3、 The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD ≤ BVDSS, Starting at T<sub>J</sub> =25oC
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

**650V N-Channel Enhancement Mode MOSFET**

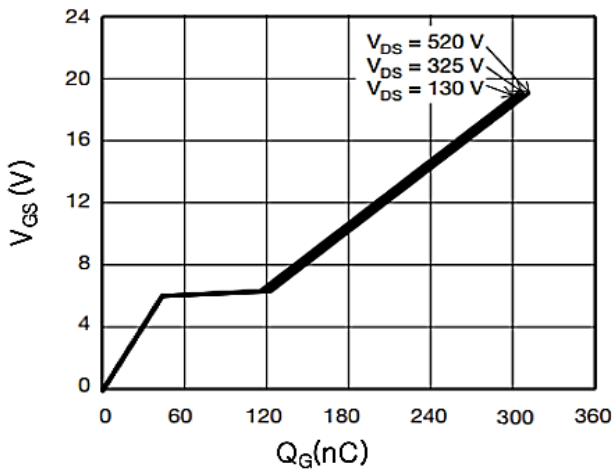
**Typical Characteristics**



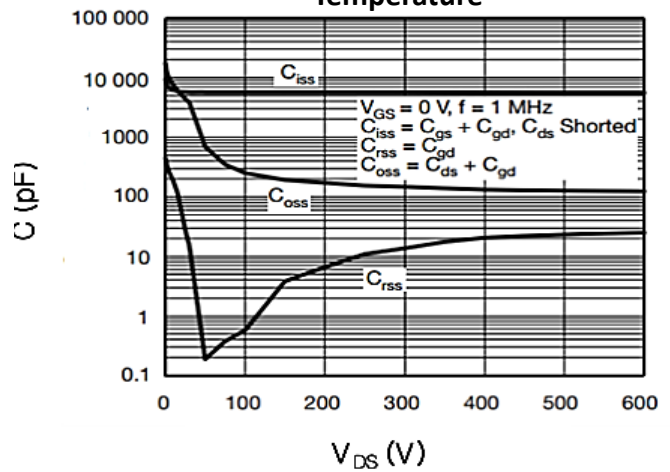
**Fig1. Output characteristics**



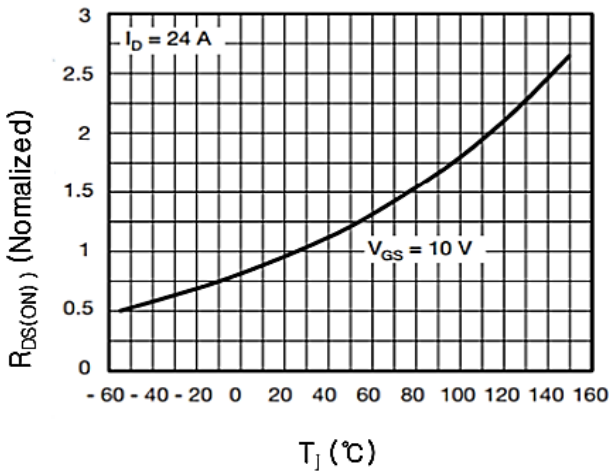
**Fig2. - Maximum Drain Current vs. Case Temperature**



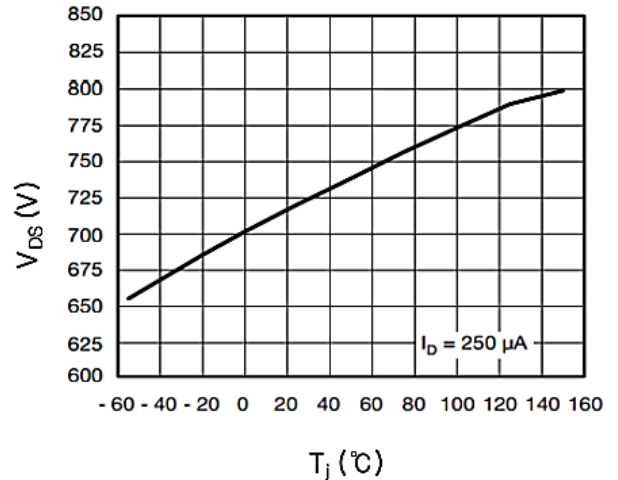
**Fig3. Gate charge characteristics**



**Fig 4. Capacitance Characteristics**



**Fig 5.  $R_{DS(ON)}$  vs junction temperature**



**Fig 6. - Temperature vs. Drain-to-Source Voltage**

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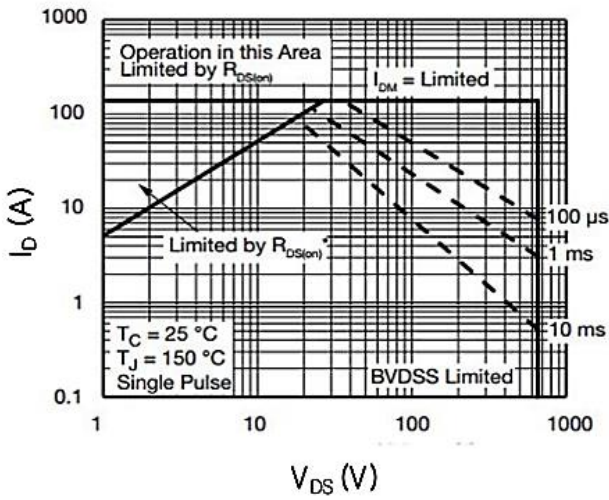


Fig 7 . Safe operating area

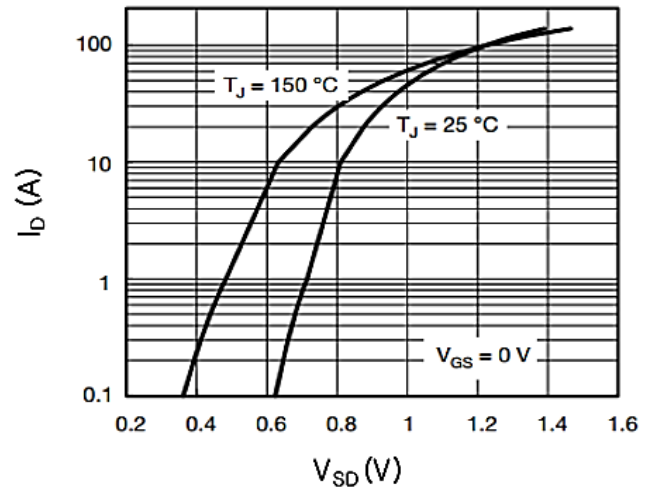


Fig 8. Forward characteristics of reverse diode

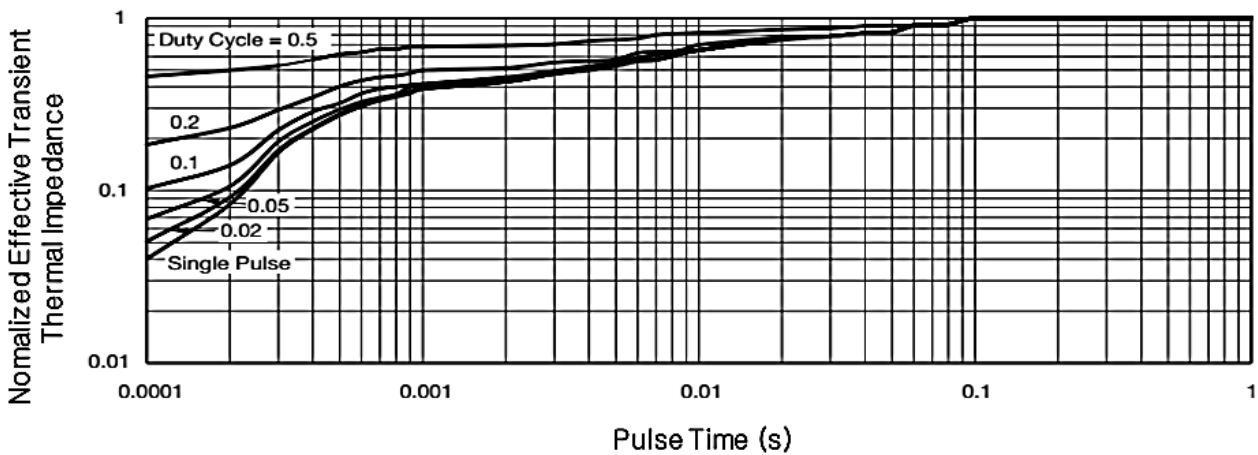
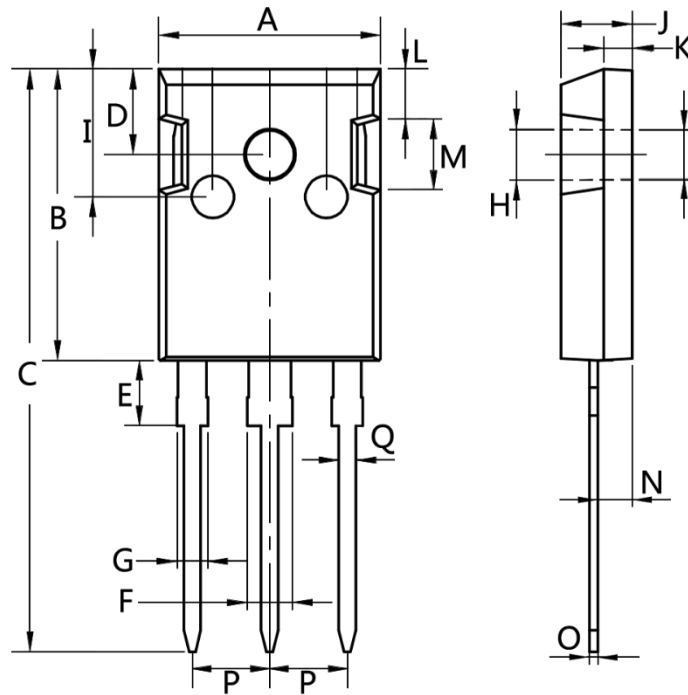


Fig 9 . Transient thermal impedance

**Package Mechanical Data-TO-247-SLK**



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

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Edition	Date	Change
Rve1.0	2018/1/31	Initial release

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