

APJ10N65D (AP65R950)

650V N-Channel Enhancement Mode MOSFET

Description

The APJ10N65D is **CoolFET II** MOSFET family that is utilizing charge balance technology for extremely low on-resistance and low gate charge performance. APJ10N65D is suitable for applications which require superior power density and outstanding efficiency

General Features

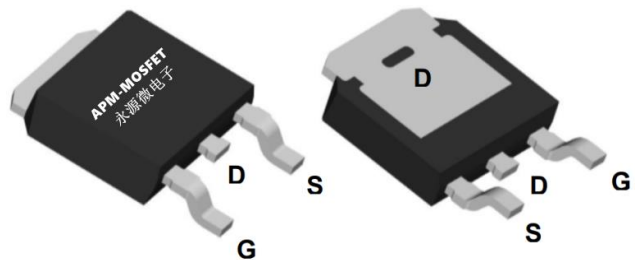
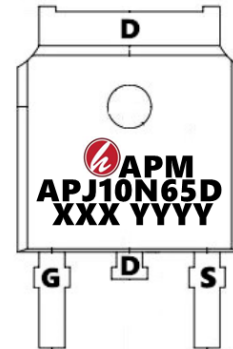
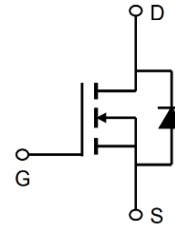
$V_{DS} = 650V$ (Type: 720V) $I_{DM} = 10A$

$R_{DS(ON)} < 950m\Omega$ @ $V_{GS} = 10V$ (Type: 890m Ω)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APJ10N65D	TO-252-3L	APJ10N65D XXX YYYY	2500

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	650	V
I_D	Continuous Drain Current	10	A
I_{DM}	Pulsed Drain Current (note1)	30	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	125	mJ
P_D	Power Dissipation ($T_C = 25^\circ C$)	25.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	4.9	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	49	$^\circ C/W$



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V _{GS} =0V, I _D =250uA	650	720	--	V
ΔBV _{DSS} / ΔT _J	Breakdown voltage temperature coefficient	I _D =250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V _{DS} =650V, V _{GS} =0V	--	--	1	uA
		V _{DS} =520V, T _C =125°C	--	--	50	uA
IGSS	Gate to source leakage current, forward	V _{GS} =30V, V _{DS} =0V	--	--	100	nA
	Gate to source leakage current, reverse	V _{GS} =-30V, V _{DS} =0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V _{DS} =V _{GS} , I _D =250uA	2.5	3.3	4.5	V
RDS(ON)	Drain to source on state resistance	V _{GS} =10V, I _D =3.2A	--	860	950	mΩ
Ciss	Input capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	--	263	--	pF
Coss	Output capacitance		--	13.7	--	
Crss	Reverse transfer capacitance		--	1.06	--	
td(on)	Turn on delay time	V _{DS} =400V, I _D =2.2A, R _G =4.7Ω, V _{GS} =10V	--	12.8	--	ns
tr	Rising time		--	26.4	--	
td(off)	Turn off delay time		--	22.2	--	
tf	Fall time		--	75.6	--	
Q _g	Total gate charge	V _{DS} =480V, V _{GS} =10V, I _D =2A	--	1.07	--	nC
Q _{gs}	Gate-source charge		--	3.63	--	
Q _{gd}	Gate-drain charge		--	7.72	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	5	A
ISM	Pulsed source current		--	--	15	A
VSD	Diode forward voltage drop.	I _S =3.2A, V _{GS} =0V	--	0.7	1.5	V
T _{rr}	Reverse recovery time	I _S =3.2A, V _{GS} =0V, V _{dd} =400V, di _F /dt=100A/us,	--	313	--	ns
Q _{rr}	Reverse recovery Charge		--	0.92	--	uC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The EAS data shows Max. rating . L=0.5mH, I_{AS} =2.3A, V_{DD} =50V, R_G=25Ω
- The test condition is Pulse Test: I_{SD} ≤ I_D, di/dt = 100A/us, V_{DD} ≤ BVDSS, Starting at T_J =25°C
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

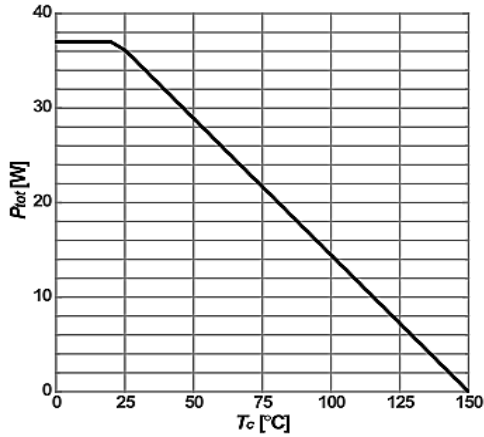


Figure1: Power dissipation (Non FullPAK)

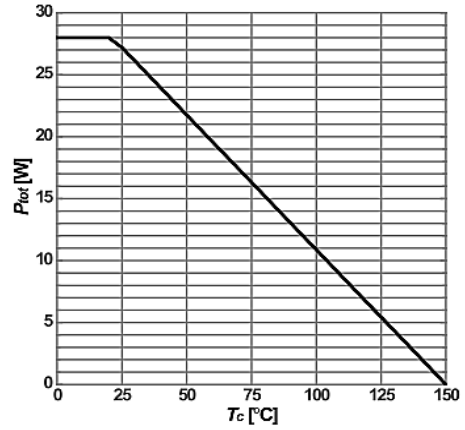


Figure2: Power dissipation (FullPAK)

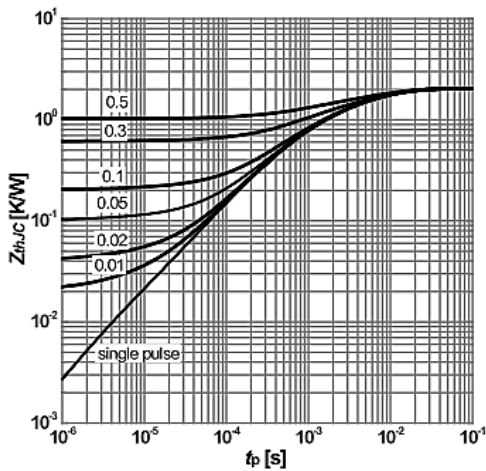


Figure3: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D = t_p/T$

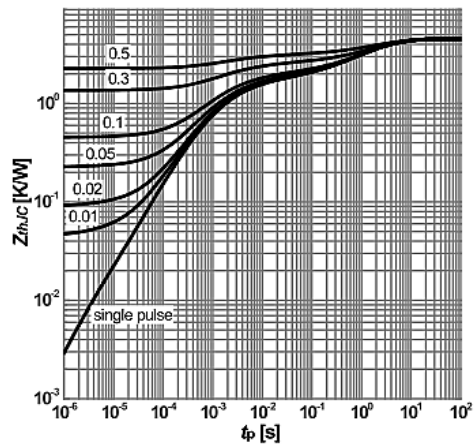


Figure4: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D = t_p/T$

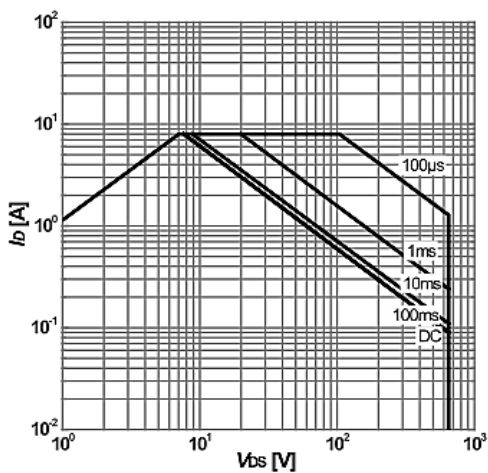


Figure5: Safe operating area (Non FullPAK)
 $I_D=f(V_{DS})$; $T_J=25^\circ\text{C}$; $D=0$; parameter: t_p

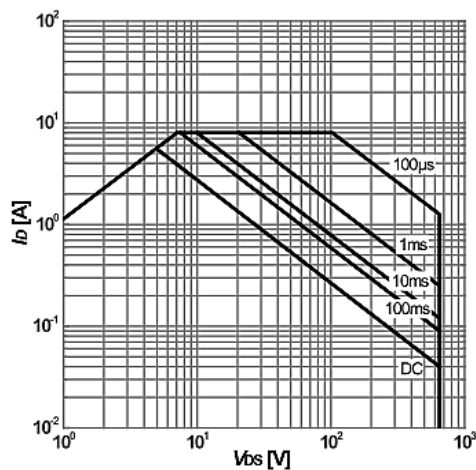


Figure6: Safe operating area (FullPAK)
 $I_D=f(V_{DS})$; $T_J=25^\circ\text{C}$; $D=0$; parameter: t_p

APJ10N65D (AP65R950)

650V N-Channel Enhancement Mode MOSFET

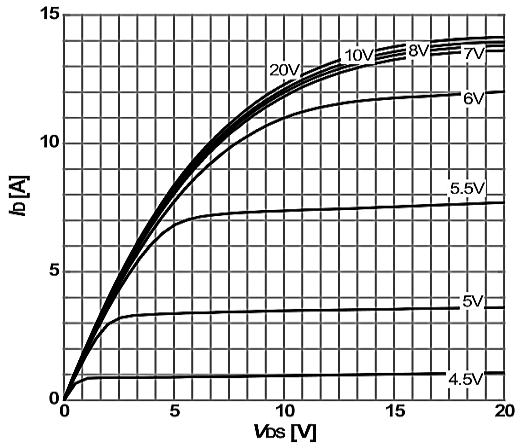


Figure 7: Typ. output characteristics
 $I_D=f(V_{DS}); T_J=25^\circ\text{C}; \text{parameter: } V_{GS}$

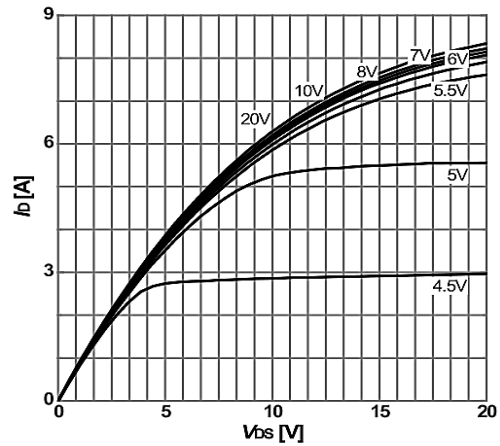


Figure 8: Typ. output characteristics
 $I_D=f(V_{DS}); T_J=125^\circ\text{C}; \text{parameter: } V_{GS}$

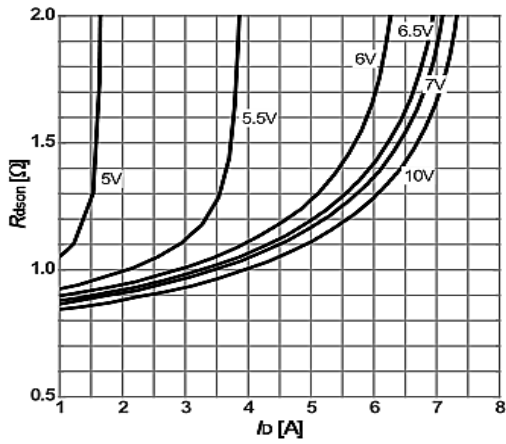


Figure 9: Typ. drain-source on-state resistance
 $R_{DS(on)}=f(I_D); T_J=25^\circ\text{C}; \text{parameter: } V_{GS}$

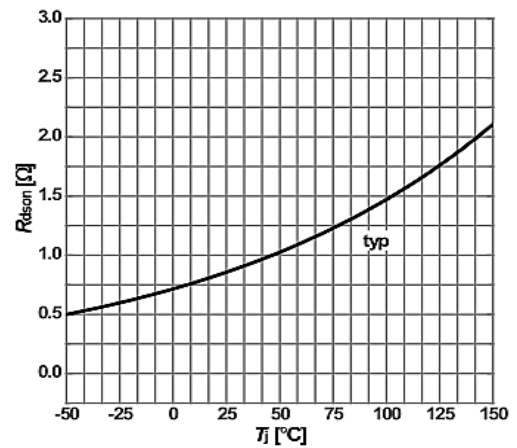


Figure 10: drain-source on-state resistance
 $R_{DS(on)}=f(T_J); I_D=3.2\text{A}; V_{GS}=10\text{V}$

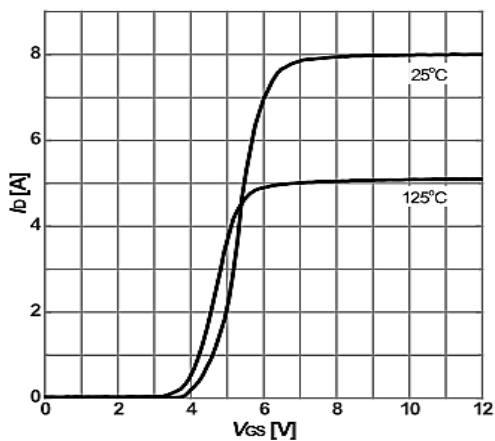


Figure 11: Type. transfer characteristics
 $I_D=f(V_{GS}); V_{DS}=20\text{V}; \text{parameter: } T_J$

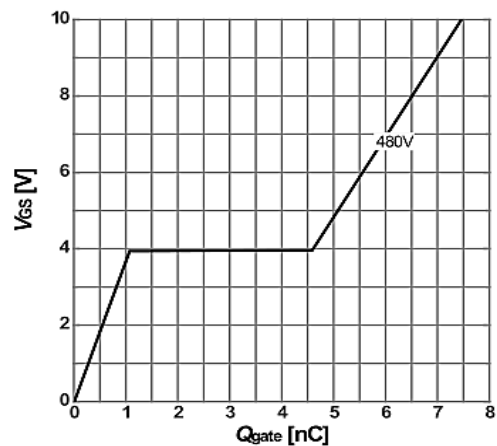
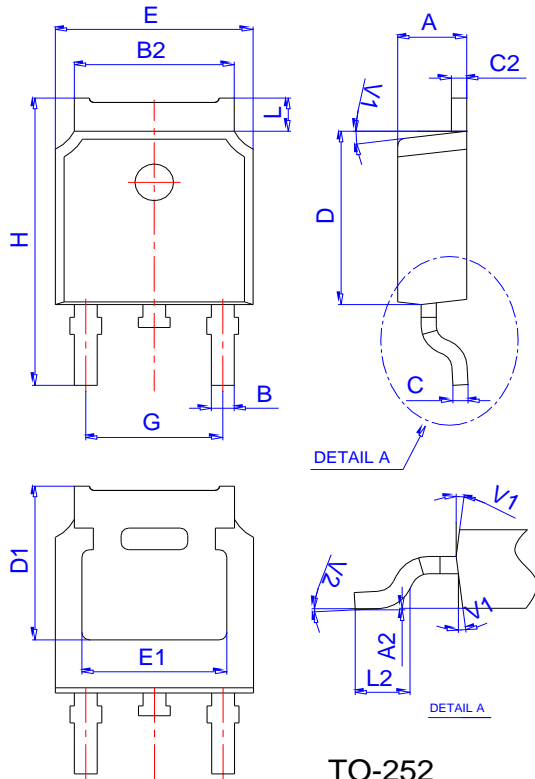


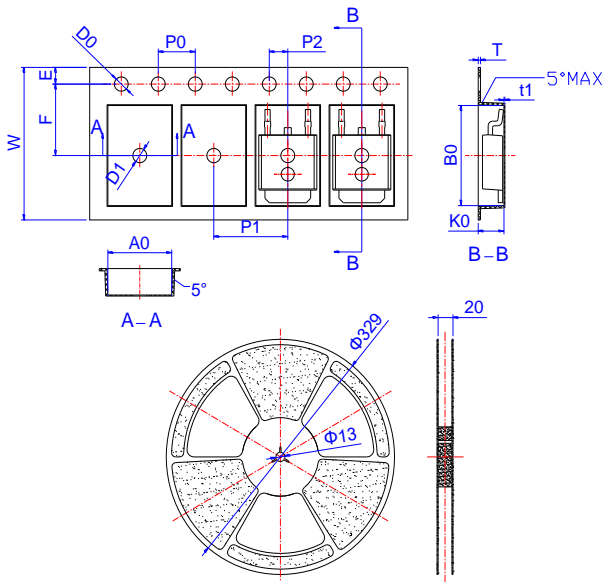
Figure 12: Type. gate charge
 $V_{GS}=f(Q_{gate}); I_D=3.2\text{A pulsed}; V_{DS}=480\text{V}$

Package Mechanical Data: TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

Attention

1, Any and all APM Microelectronics products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your APM Microelectronics representative nearest you before using any APM Microelectronics products described or contained herein in such applications.

2, APM Microelectronics assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all APM Microelectronics products described or contained herein.

3, Specifications of any and all APM Microelectronics products described or contained here instipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

4, APM Microelectronics Semiconductor CO., LTD. strives to supply high quality high reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

5, In the event that any or all APM Microelectronics products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

6, No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of APM Microelectronics Semiconductor CO., LTD.

7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. APM Microelectronics believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the APM Microelectronics product that you intend to use.

APJ10N65D (AP65R950)

650V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2021/9/24	Initial release

Copyright Attribution "APM-Microelectronice"