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100V N-SGT Enhancement Mode MOSFET

Description

The APG120N12NF uses advanced trench technology to provide excellent RDS(ON), low gate charge and

operation with gate voltages as low as 10V. This

device is suitable for use as a

Battery protection or in other Switching application.

General Features

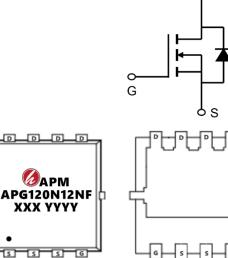
V_{DS} = 120V I_D = 120 A

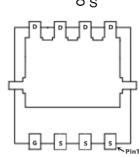
 $R_{DS(ON)} < 7.5 m\Omega @ V_{GS} = 10V$

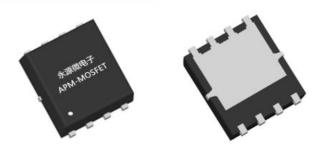
Application

Battery protection

Load switch Uninterruptible power supply







Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)	
APG120N12NF	PDFN5*6-8L	APG120N12NF XXX YYYY	5000	

Absolute Maximum Ratings (Tc=25°Cunless otherwise noted)

Symbol	Parameter	Value	Units
VDSS	Drain-to-Source Voltage	120	V
I₀@T _A =25℃	Continuous Drain Current ¹	120	А
I ⊳@T A =70 ℃	Continuous Drain Current ¹	70	А
IDM ^{a1}	Pulsed Drain Current	320	А
EASa2	Single pulse avalanche energy	240	mJ
IAR	Single pulse avalanche current	40	А
VGS	Gate-to-Source Voltage	±20	V
PD	Power Dissipation	125	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55 to 150	°C
ΤL	Maximum Temperature for Soldering	300	°C
RθJC	Thermal Resistance, Junction-to-Case	1.0	°C/W
RθJA	Thermal Resistance, Junction-to-Ambient	50	°C/W

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Electrical Characteristics (TJ=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
VDSS	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250µA	120			V
IDSS	Drain to Source Leakage Current	V _{DS} = 120V, V _{GS} = 0V			1	μA
IGSS(F)	Gate to Source Forward Leakage	V _{GS} =+20V			100	nA
IGSS(R)	Gate to Source Reverse Leakage	V _{GS} =-20V			-100	nA
VGS(TH)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D = 250 \mu A$	2.5	3.0	3.5	V
RDS(ON)1	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =20A		6.0	6.8	mΩ
gFS	Forward Transconductance	V _{DS} =5V, I _D =50A		130		S
Ciss	Input Capacitance			4282		pF
Coss	Output Capacitance	V _{GS} = 0V V _{DS} = 50V f =		429		pF
Crss	Reverse Transfer Capacitance	1.0MHz		17		pF
Rg	Gate resistance			2.5		Ω
td(ON)	Turn-on Delay Time			20		ns
tr	Rise Time	- I _D =20A V _{DS} = 50V		11		ns
td(OFF)	Turn-Off Delay Time	$V_{GS} = 10V$ $R_G = 5\Omega$		55		ns
tf	Fall Time	- NG - 332		28		ns
Qg	Total Gate Charge	V _{GS} =0~10V		61.4		nC
Qgs	Gate Source Charge	V _{DS} = 50V		17.4		nC
Qgd	Gate Drain Charge	I _D =20A		14.1		nC
IS	Diode Forward Current	T 05 00			100	Α
ISM	Diode Pulse Current	T _C =25 °C			320	А
VSD	Diode Forward Voltage	Is=6.0A, V _{GS} =0V			1.2	V
trr	Reverse Recovery time	I _S =20A, V _{DD} =50V		100		ns
Qrr	Reverse Recovery Charge	dl⊧/dt=100A/µs		250		nC

Note :

1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%

3、The EAS data shows Max. rating . The test condition is VDD=50V, L=0.3mH, Rg=25 Ω , Starting TJ=25 $^\circ$ C

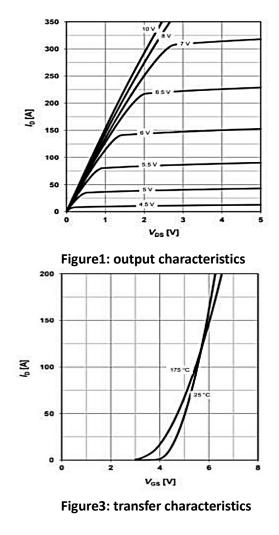
4. The power dissipation is limited by 150° junction temperature

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Typical Characteristics

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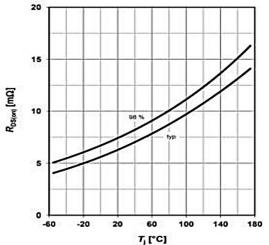


Figure5: Drain-source on-state resistance

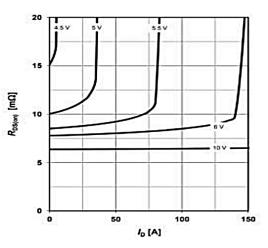


Figure2: Typcal drain-source on resistance

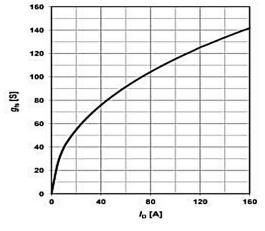


Figure4: forward transconductance

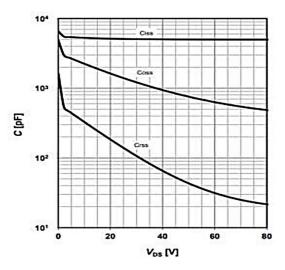


Figure6: Typ. capacitances

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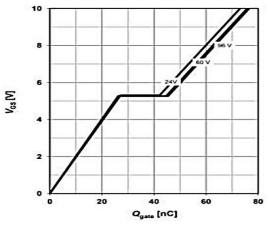


Figure7: Typ. gate charge

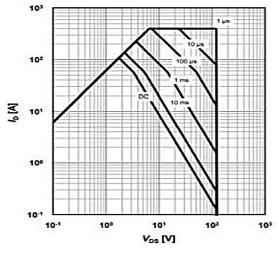


Figure9: Safe operating area

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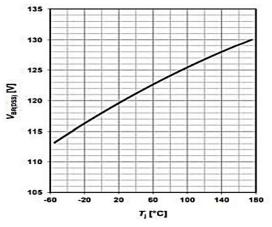


Figure8: Drain-source breakdown voltage

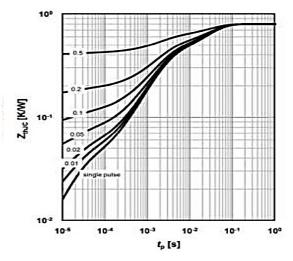
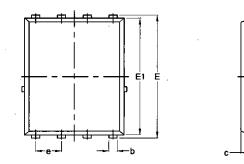
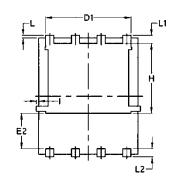


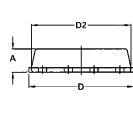
Figure 10: Max. transient thermal impedance



100V N-SGT Enhancement Mode MOSFET Package Mechanical Data-DFN5*6-8L-JQ Single







	Common				
Symbol	mm		Inch		
	Mim	Max	Min	Max	
А	1.03	1.17	0.0406	0.0461	
b	0.34	0.48	0.0134	0.0189	
С	0.824	0.0970	0.0324	0.082	
D	4.80	5.40	0.1890	0.2126	
D1	4.11	4.31	0.1618	0.1697	
D2	4.80	5.00	0.1890	0.1969	
E	5.95	6.15	0.2343	0.2421	
E1	5.65	5.85	0.2224	0.2303	
E2	1.60	/	0.0630	/	
е	1.27	7 BSC 0.05 B		3SC	
L	0.05	0.25	0.0020	0.0098	
L1	0.38	0.50	0.0150	0.0197	
L2	0.38	0.50	0.0150	0.0197	
Н	3.30	3.50	0.1299	0.1378	
l	/	0.18	/	0.0070	

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Edition	Date	Change
Rve1.0	2020/11/1	Initial release

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