

## 68V N-Channel Enhancement Mode MOSFET

### Description

The AP80N07P/T uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with High EAS. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 68V$   $I_D = 80A$

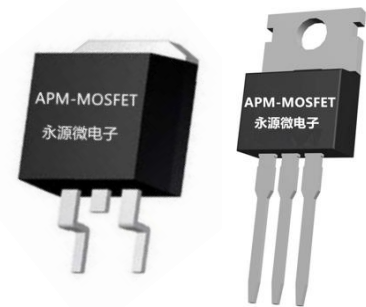
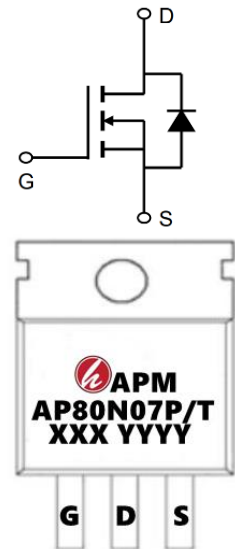
$R_{DS(ON)} < 9.0m\Omega$  @  $V_{GS}=10V$  (Type: 7.2m $\Omega$ )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N07P	TO-220-3L	AP80N07P XXX YYYY	1000
AP80N07T	TO-263-3L	AP80N07T XXX YYYY	800

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	68	V
VGS	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	80	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	52	A
IDM	Pulsed Drain Current <sup>2</sup>	320	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	110	mJ
IAS	Avalanche Current	22	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	103	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	63	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.46	$^\circ C/W$

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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	68	72	---	V
ΔBVDSS/ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.023	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	---	7.2	9.0	mΩ
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	2.0	3.0	4.0	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	-4.2	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =68V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =68V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =30V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	---	35	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	11	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	9	---	
Td(on)	Turn-On Delay Time	V <sub>DS</sub> =30V, I <sub>D</sub> =30A, R <sub>GEN</sub> =3Ω, V <sub>GS</sub> =10V	---	15	---	ns
T <sub>r</sub>	Rise Time		---	90	---	
Td(off)	Turn-Off Delay Time		---	45	---	
T <sub>f</sub>	Fall Time		---	30	---	
Ciss	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	400	---	pF
Coss	Output Capacitance		---	267	---	
Crss	Reverse Transfer Capacitance		---	250	---	
IS	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	80	A
ISM	Pulsed Source Current <sup>2,5</sup>		---	---	320	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =80A	---	---	1.2	V
trr	Reverse Recovery Time	T <sub>J</sub> =25°C I <sub>F</sub> =20A, dI/dt=100A/μs	---	78	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	51	---	nC

#### Note :

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width .The EAS data shows Max. rating .
- 3、The test cond ≅ 300us duty cycle ≅ 2%, duty cycle ition is T<sub>J</sub>=25°C, V<sub>DD</sub> =35V, V<sub>G</sub> =10V, R<sub>G</sub> =25Ω, L=0.5mH, I<sub>AS</sub> =21A
- 4、The power dissipation is limited by 175°C junction temperature
- 5、The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

### Typical Characteristics

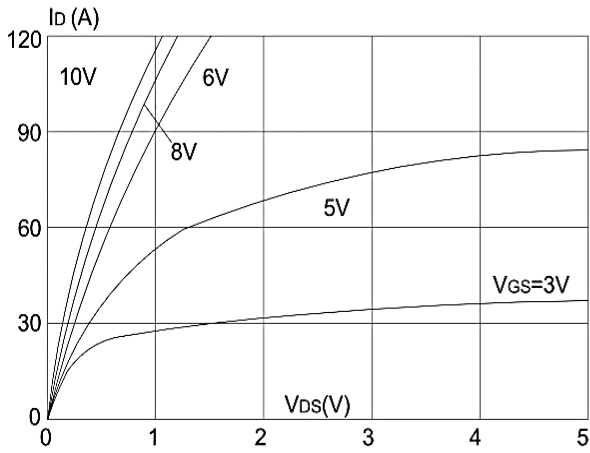


Figure 1: Output Characteristics

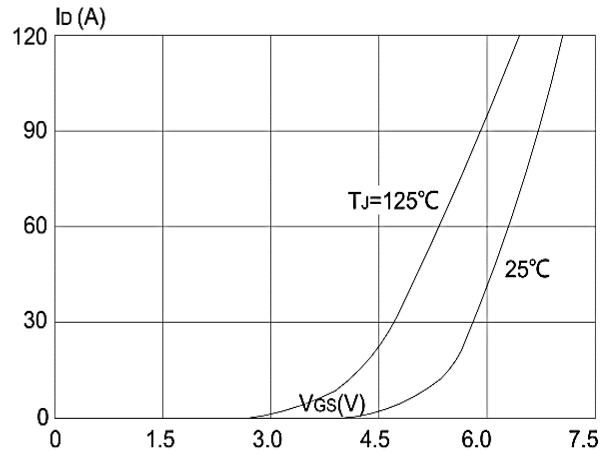


Figure 2: Typical Transfer Characteristics

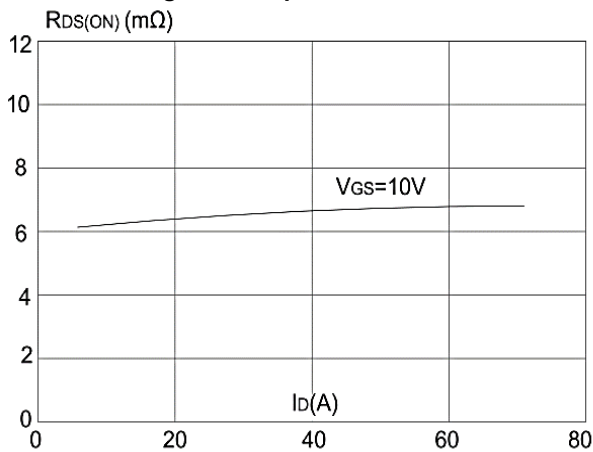


Figure 3: On-resistance vs. Drain Current

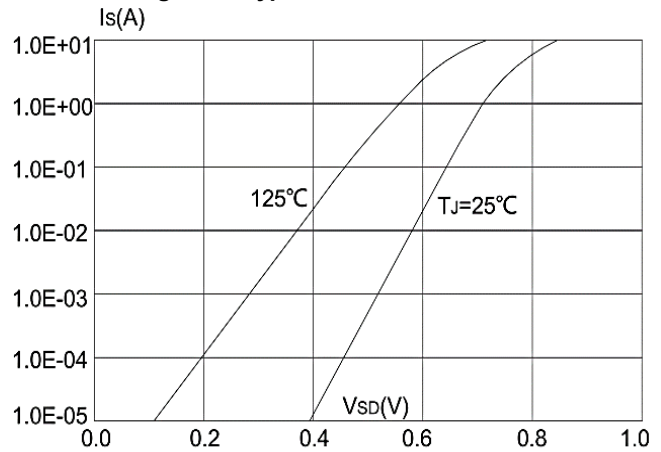


Figure 4: Body Diode Characteristics

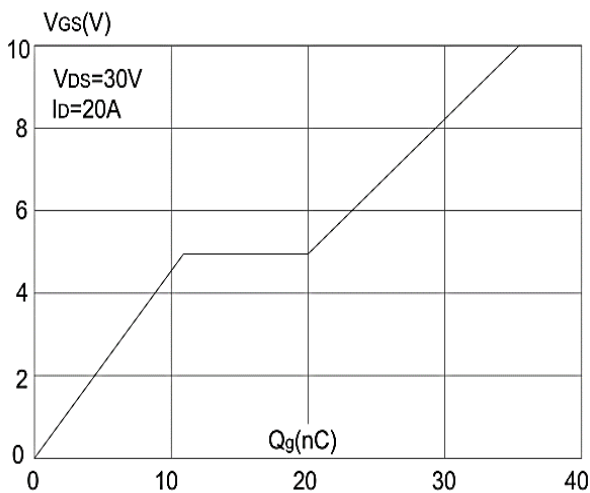


Figure 5: Gate Charge Characteristics

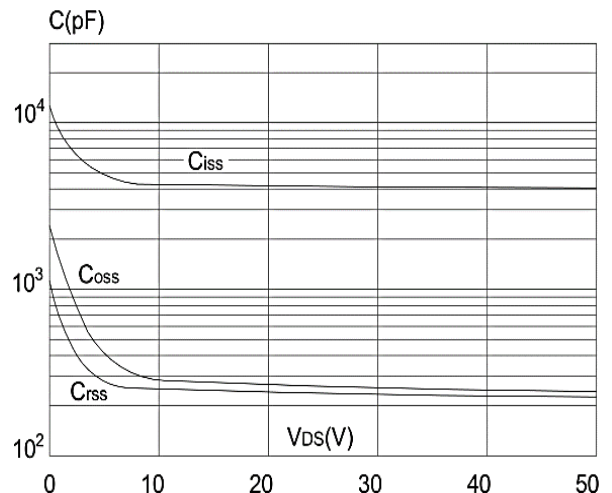
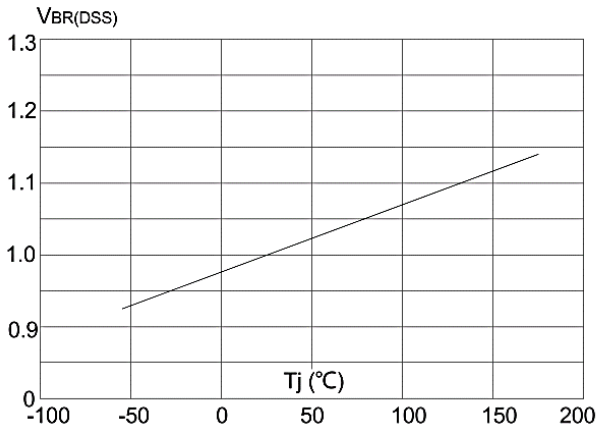
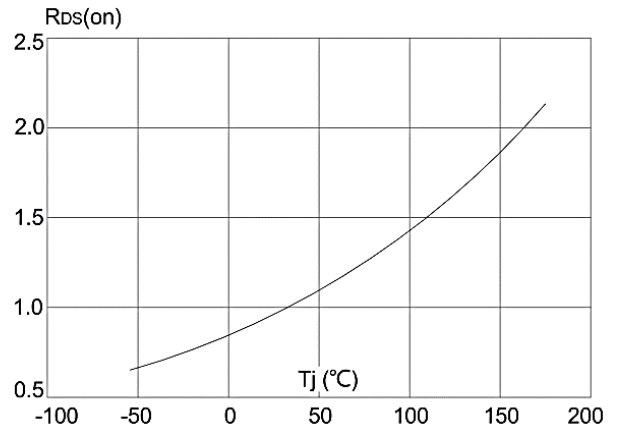


Figure 6: Capacitance Characteristics

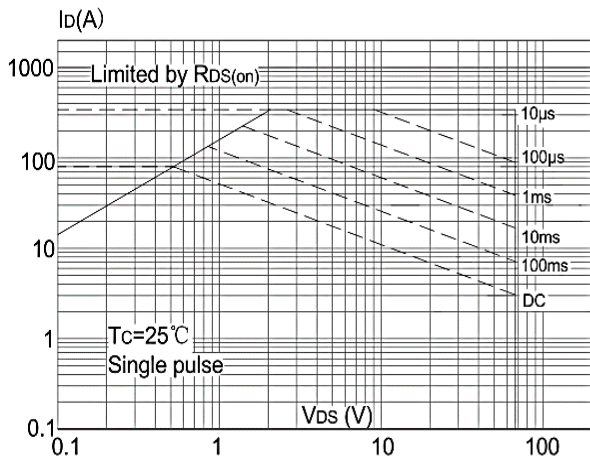
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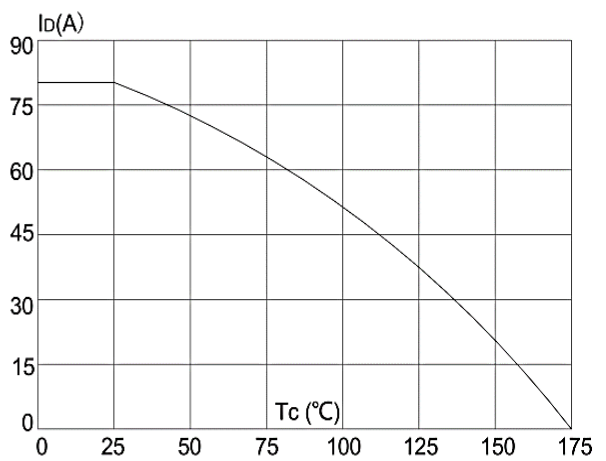
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



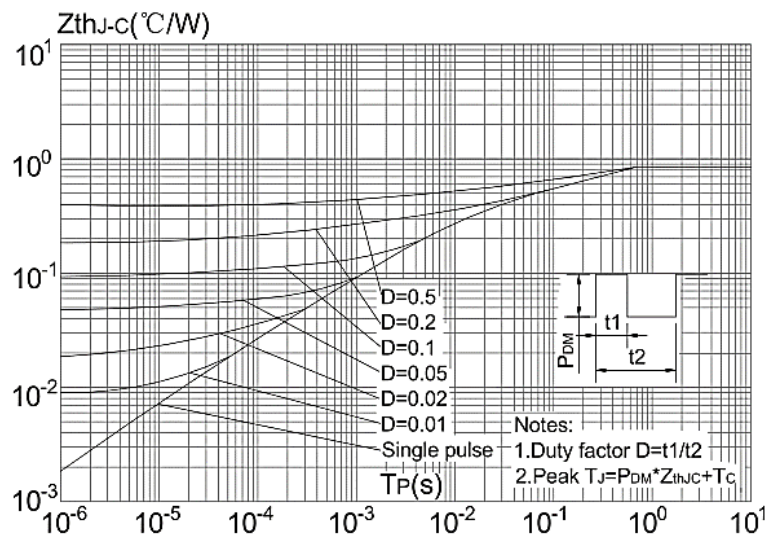
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area**

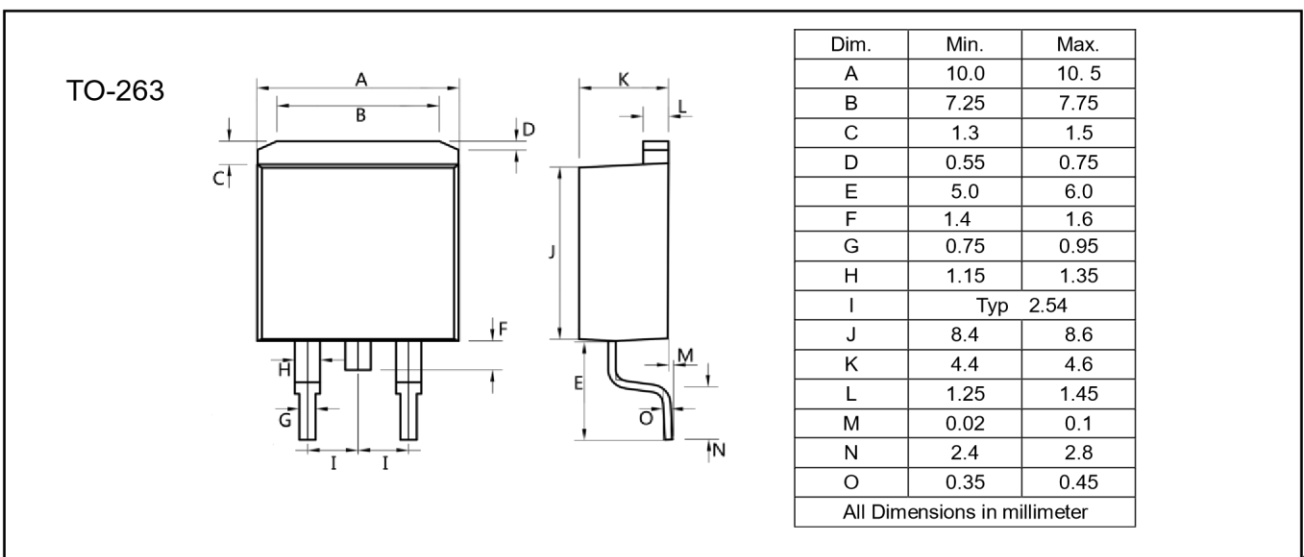
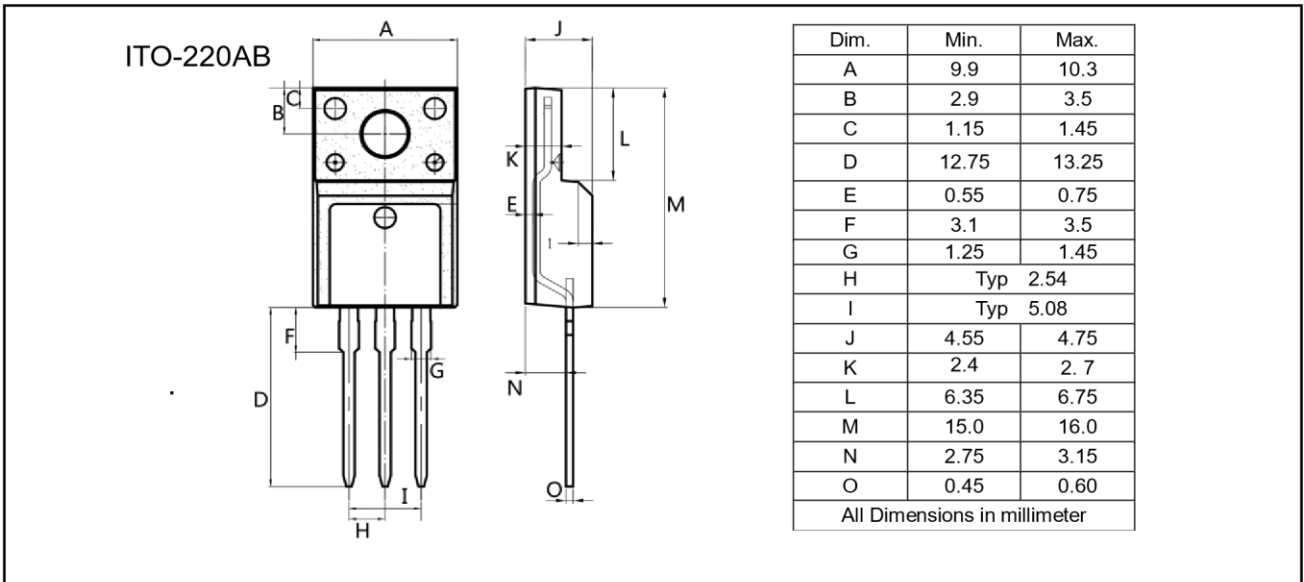
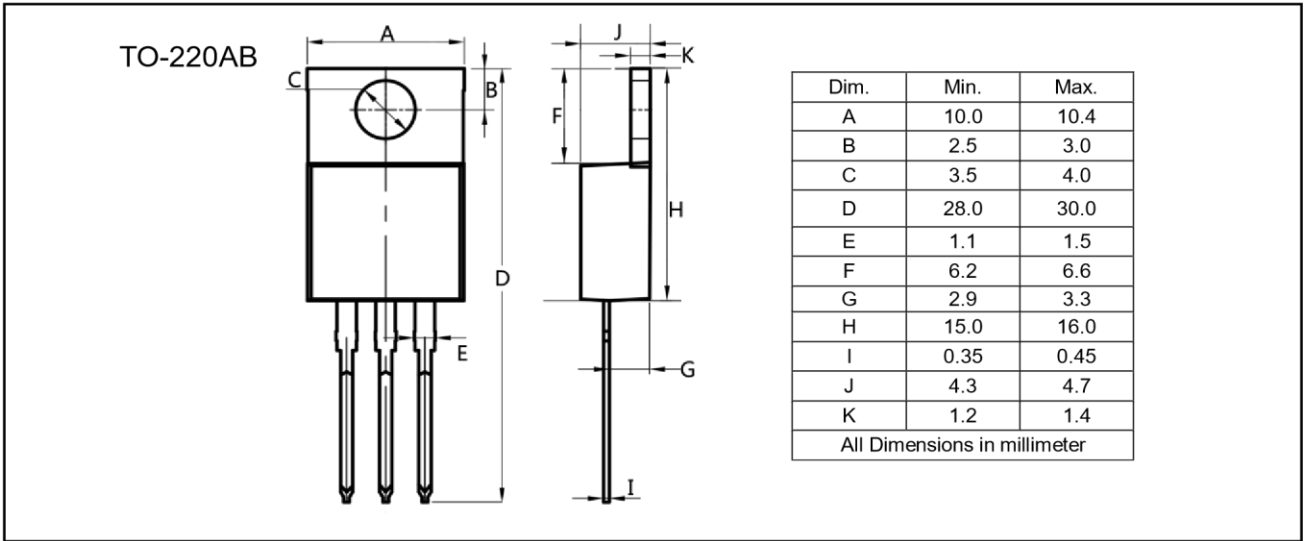


**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien**

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<b>Edition</b>	<b>Date</b>	<b>Change</b>
RVE3.8	2018/12/21	Initial release
RVE3.9	2021/1/21	Reduce QG and CISS

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