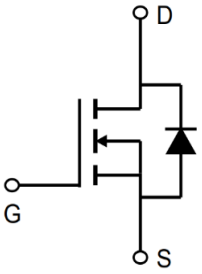
AP80N02DF

20V N-Channel Enhancement Mode MOSFET

Description

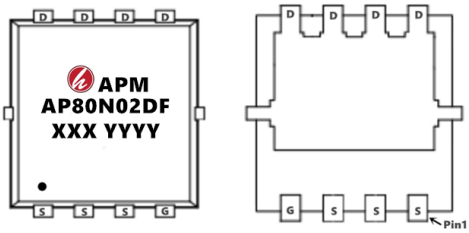
The AP80N02DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = 20V I_D =80 A

$R_{DS(ON)}$ < 2mΩ @ V_{GS}=4.5V



Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N02DF	PDFN3*3-8L	AP80N02DF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D@T_C=25℃	Continuous Drain Current[1]	80	A
I_D@T_C=100℃	Continuous Drain Current[1]	39	A
I_{DM}	Pulsed Drain Current[2]	200	A
EAS	Single Pulse Avalanche Energy[3]	80	mJ
I_{AS}	Avalanche Current	40	A
P_D@T_C=25℃	Total Power Dissipation[4]	83	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1](t≦10S)	20	℃/W
	Thermal Resistance Junction-ambient [1](Steady State)	55	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-case [1]	1.5	℃/W

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Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20	---	---	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.4	---	1.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=20A	1.05	1.5	2	mΩ
		V_{GS}=2.5V , I_D=20A	1.4	2	2.7	mΩ
I_{DSS}	Drain-Source Leakage Current	V_{DS}=16V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=16V , V_{GS}=0V , T_J=125℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±10V , V_{DS}=0V	---	---	±10	uA
Rg	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.2	---	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=15V , V_{GS}=10V , I_D=20A	---	77	---	nC
Q_{gs}	Gate-Source Charge		---	8.7	---	
Q_{gd}	Gate-Drain Charge		---	14	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3□, I_D=20A	---	10.2	---	ns
T_r	Rise Time		---	11.7	---	
$T_{d(off)}$	Turn-Off Delay Time		---	56.4	---	
T_f	Fall Time		---	16.2	---	
C_{iss}	Input Capacitance	V_{DS}=10V , V_{GS}=0V , f=1MHz	---	4307	---	pF
C_{oss}	Output Capacitance		---	501	---	
C_{rss}	Reverse Transfer Capacitance		---	321	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	50	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V
t_{rr}	Reverse Recovery Time	I_F=20A , di/dt=100A/μs , T_J=25℃	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	72	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=40A
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

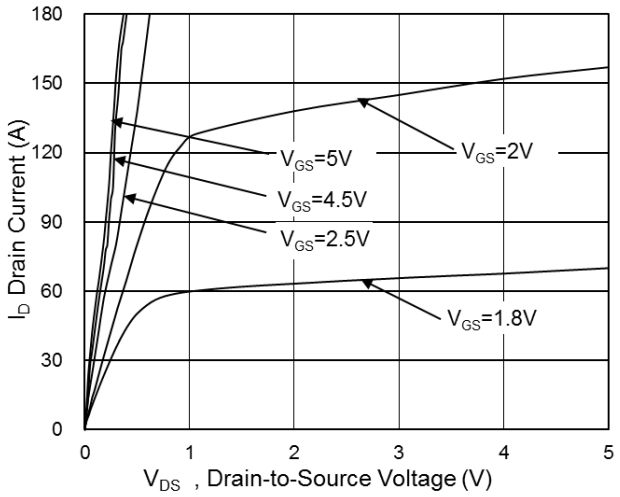


Fig.1 Typical Output Characteristics

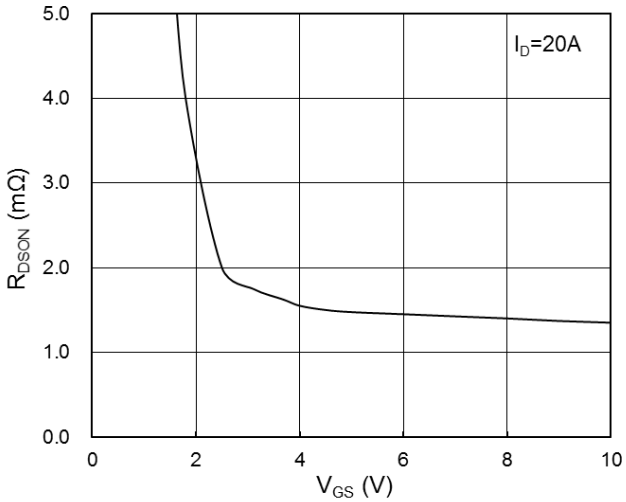


Fig.2 On-Resistance vs. Gate-Source Voltage

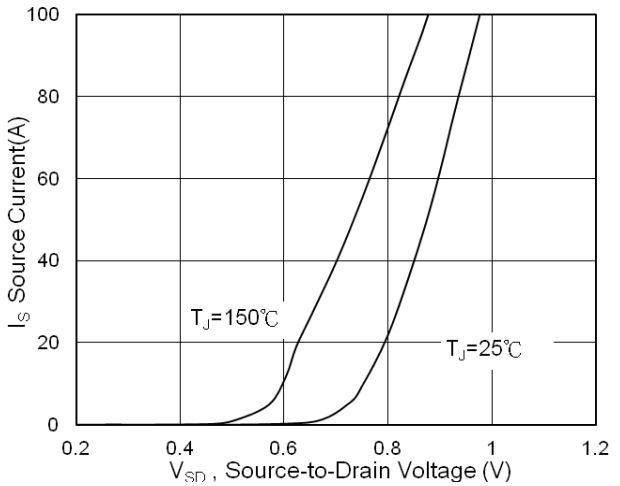


Fig.3 Forward Characteristics of Reverse

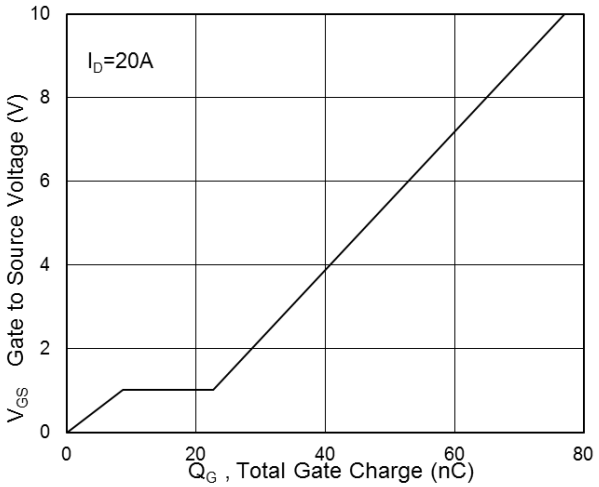


Fig.4 Gate-Charge Characteristics

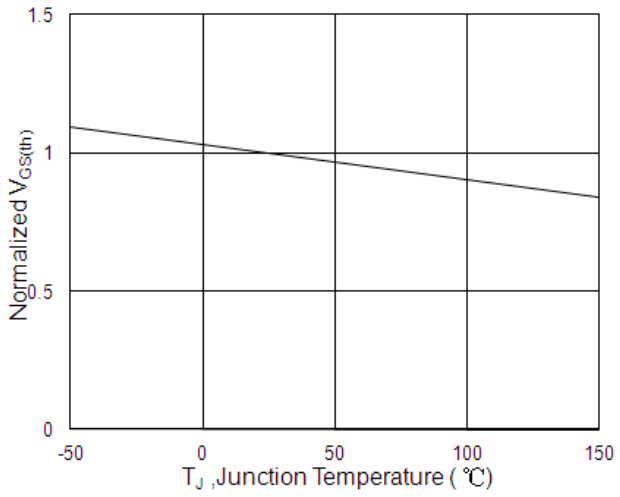


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

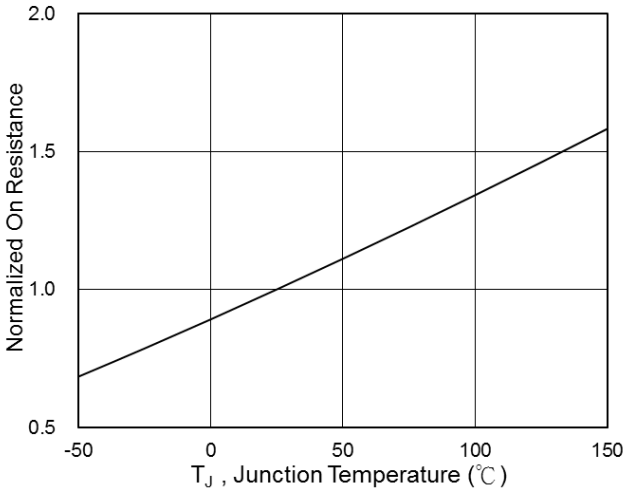


Fig.6 Normalized R_{DSON} vs. T_J

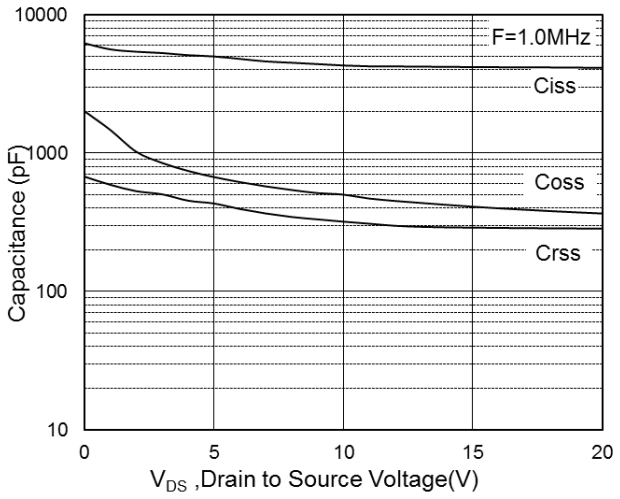


Fig.7 Capacitance

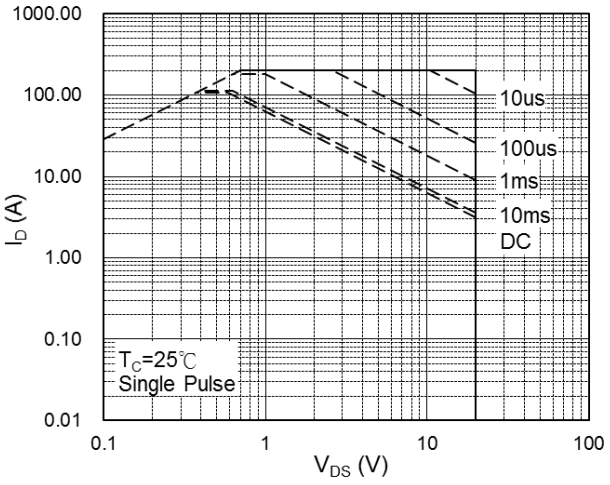


Fig.8 Safe Operating Area

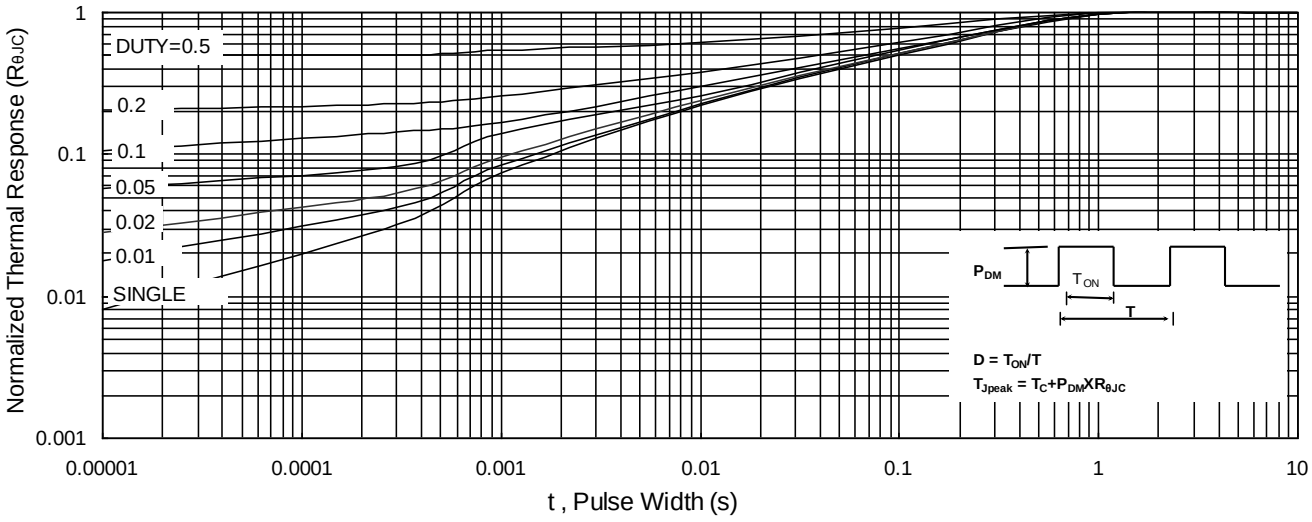


Fig.9 Normalized Maximum Transient Thermal Impedance

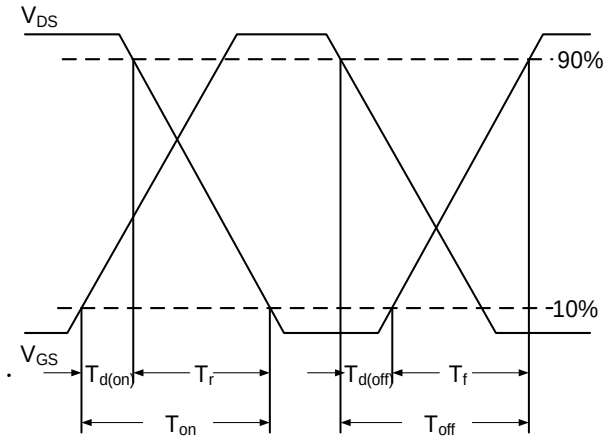


Fig.10 Switching Time Waveform

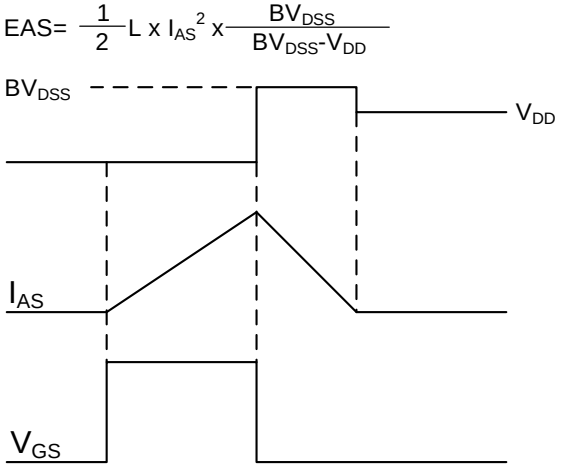
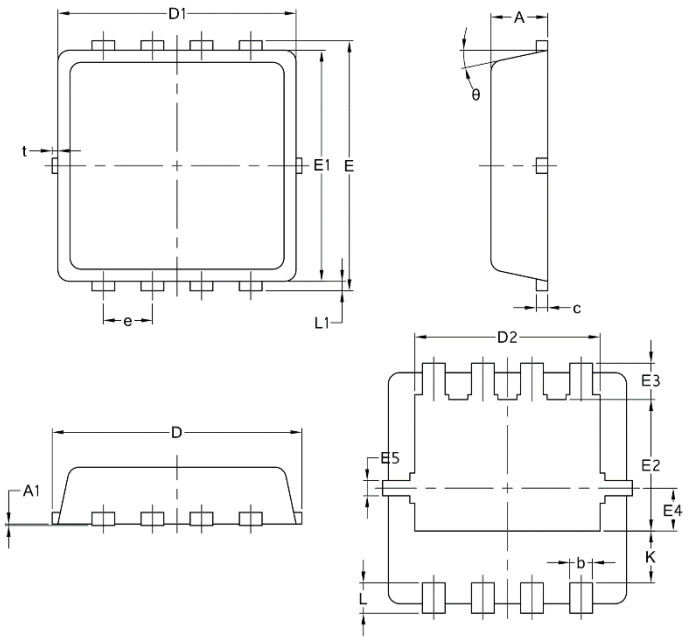


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

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20V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2019/3/31	Initial release