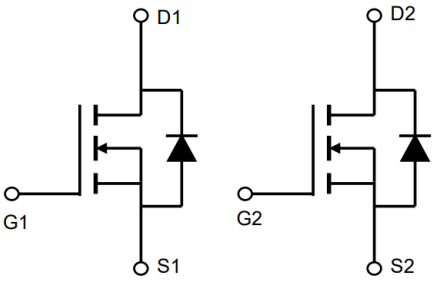
AP35H04NF

40V N+N-Channel Enhancement Mode MOSFET

Description

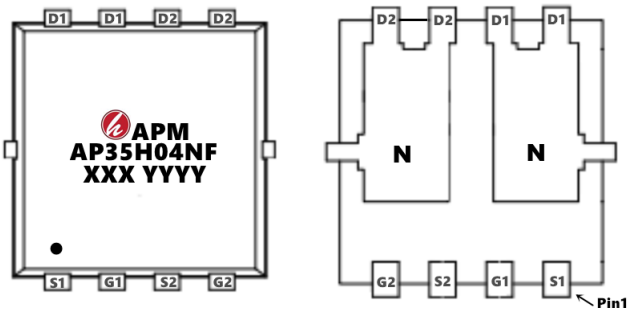
The AP35H04NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = 40V I_D =35A

$R_{DS(ON)}$ < 10mΩ @ V_{GS}=10V （**Type：8.6mΩ**）

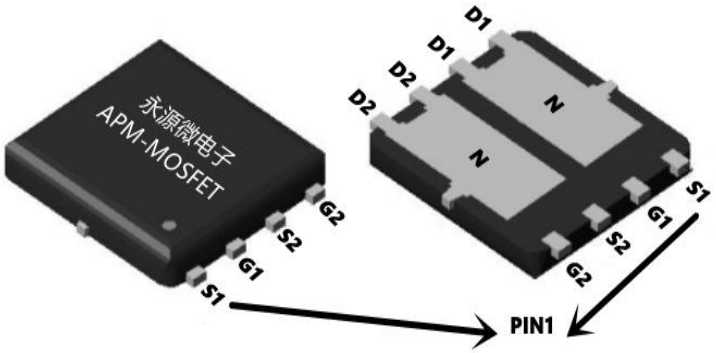


Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP35H04NF	PDFN5*6-8L	AP35H04NF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	35	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	23	A
I_{DM}	Pulsed Drain Current[2]	100	A
EAS	Single Pulse Avalanche Energy[3]	81	mJ
I_{AS}	Avalanche Current	16	A
P_D@T_C=25℃	Total Power Dissipation[4]	33.7	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	25	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	2.1	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	40	---	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.028	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance	V_{GS}=10V , I_D=30A	---	8.5	10	mΩ
		V_{GS}=4.5V , I_D=15A	---	10	16	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	1.6	2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-6.16	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=40V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=40V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=30A	---	22	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.7	3.4	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=10V , I_D=25A	---	37	---	nC
Q_{gs}	Gate-Source Charge		---	6	---	
Q_{gd}	Gate-Drain Charge		---	7	---	
Td(on)	Turn-On Delay Time	V_{DD}=30V , V_{GS}=10V , R_G=1Ω I_D=25A	---	12	---	ns
T_r	Rise Time		---	12	---	
Td(off)	Turn-Off Delay Time		---	38	---	
T_f	Fall Time		---	9	---	
C_{iss}	Input Capacitance	V_{DS}=20V , V_{GS}=0V , f=1MHz	---	2400	---	pF
Coss	Output Capacitance		---	192	---	
Crss	Reverse Transfer Capacitance		---	165	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	50	A
ISM	Pulsed Source Current[2,5]		---	---	200	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V
t_{rr}	Reverse Recovery Time	IF=30A , dI/dt=100A/μs ,T_J=25℃	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	11	---	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3、The EAS data shows Max. rating . The test condition is VDD=36V,VGS =10V,L=0.1mH,IAS =16A
4、The power dissipation is limited by 150℃ junction temperature
5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

Typical Characteristics

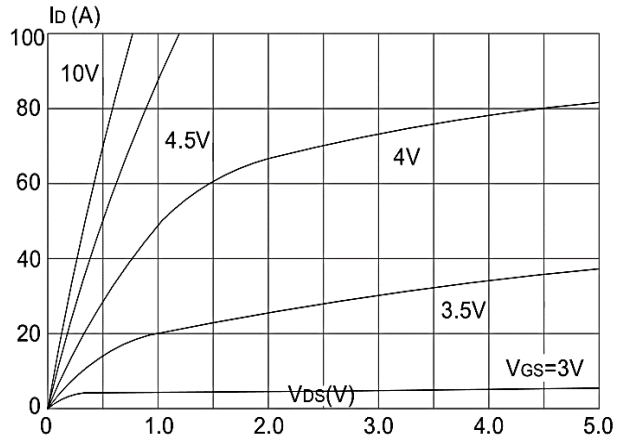


Figure1: Output Characteristics

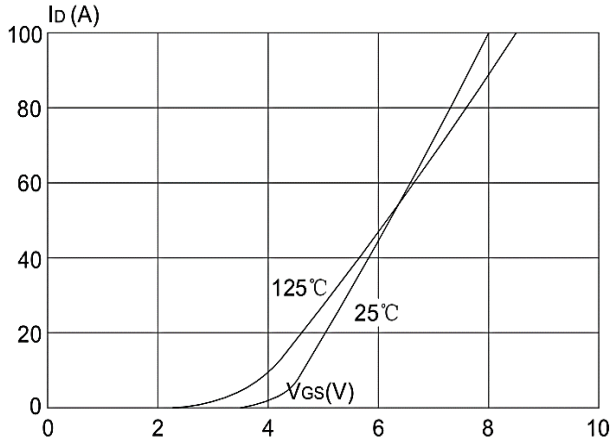


Figure 2: Typical Transfer Characteristics

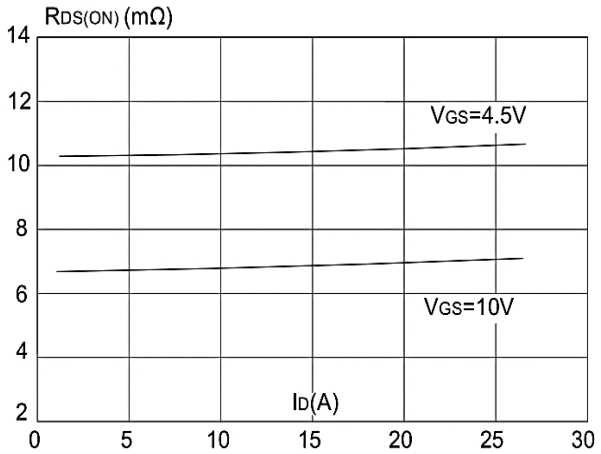


Figure 3:On-resistance vs. Drain Current

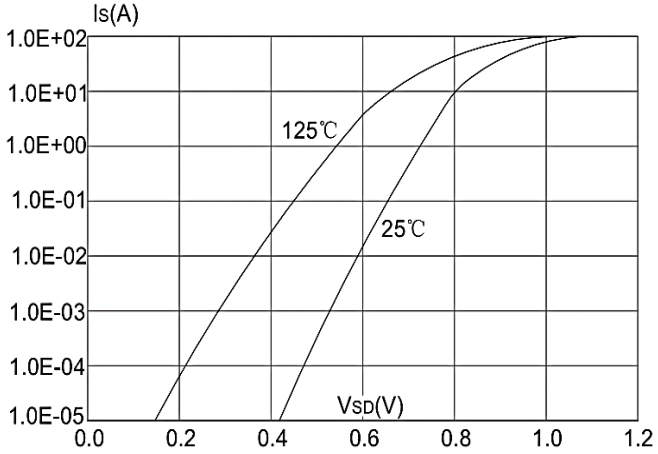


Figure 4: Body Diode Characteristics

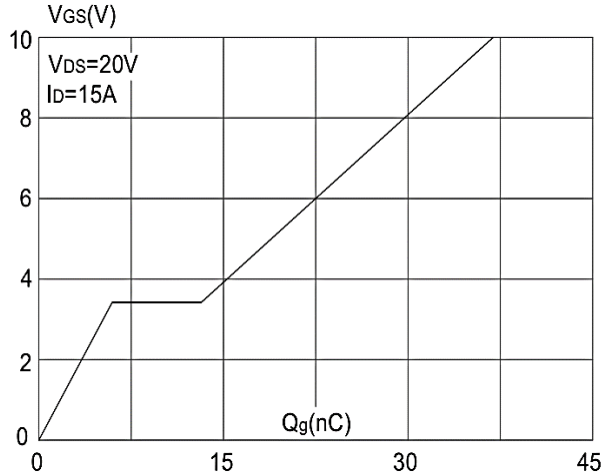


Figure 5: Gate Charge Characteristics

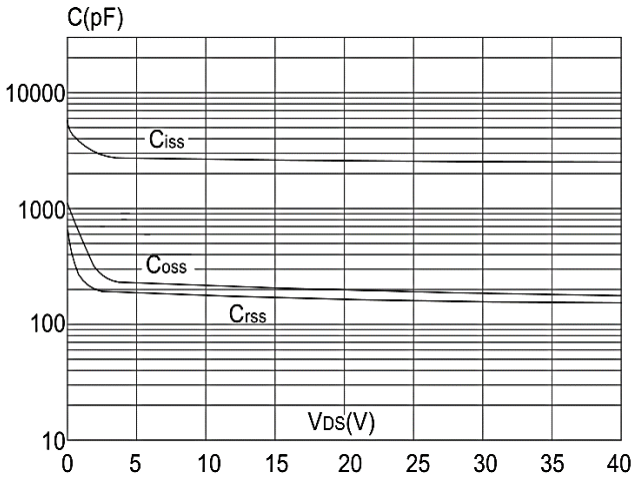


Figure 6: Capacitance Characteristics

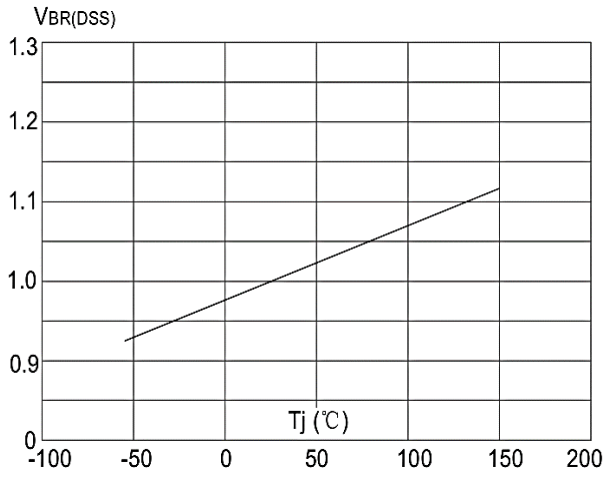


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

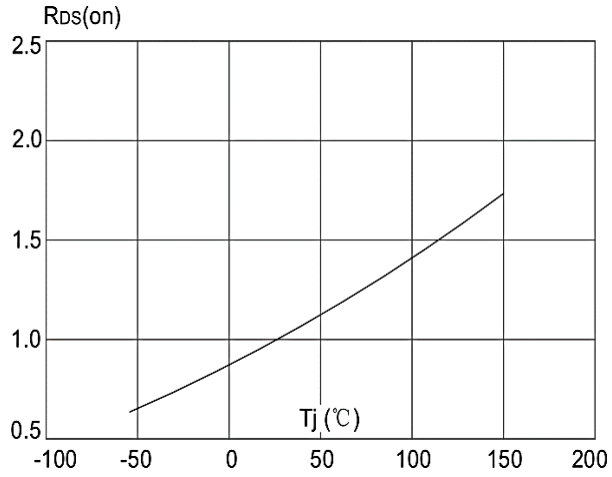


Figure 8: Normalized on Resistance vs Junction Temperature

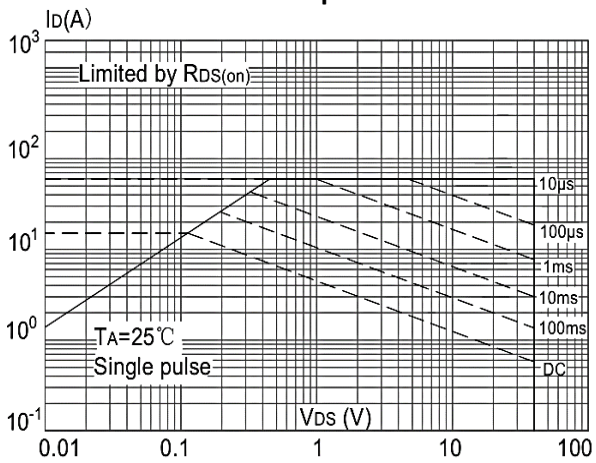


Figure 9: Maximum Safe Operating Area vs. Case Temperature

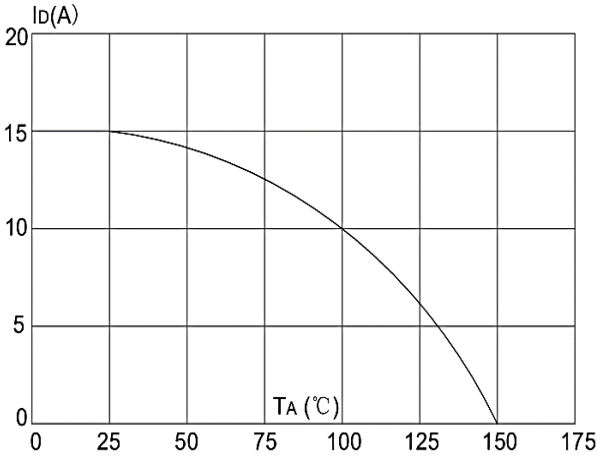


Figure 10: Maximum Continuous Drain Current

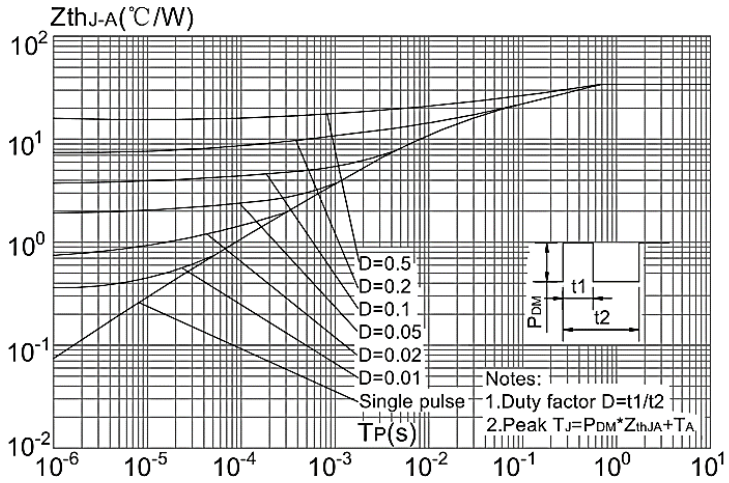
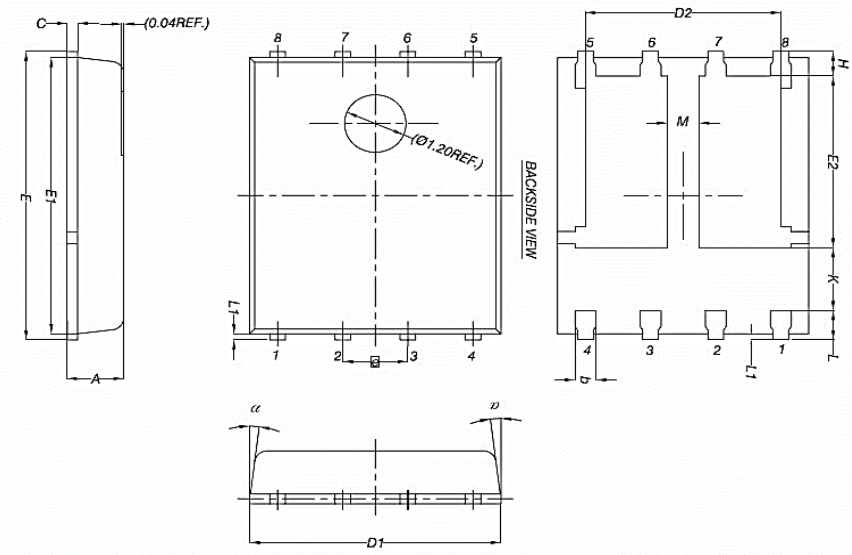


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-DFN5*6-8L-JQ Double



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	3.30	3.45
E2	3.38	3.05	3.20
e	1.27BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	--	--
a	0°	--	12°

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40V N+N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2020/8/1	Initial release