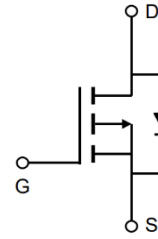


## 30V P-Channel Enhancement Mode MOSFET

### Description

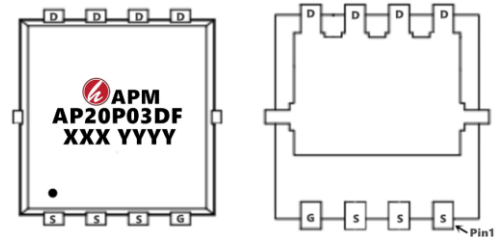
The AP20P03DF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = -30V$   $I_D = -20A$

$R_{DS(ON)} < 25m\Omega$  @  $V_{GS} = -10V$



### Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP20P03DF	PDFN3*3-8L	AP20P03DF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10V^1$	-20	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10V^1$	-13	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-80	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	16	mJ
$I_{AS}$	Avalanche Current	-17	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	16.6	W
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	1.67	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	7.53	$^\circ\text{C/W}$

## 30V P-Channel Enhancement Mode MOSFET

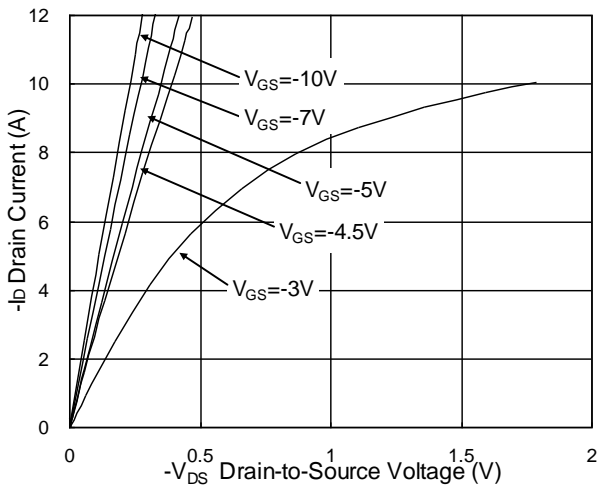
### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	32	---	V
ΔBVDSS/ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.022	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-10A	---	18.8	25	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A	---	30.5	40	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.2	-1.7	-2.5	V
ΔVGS(th)	V <sub>GS(th)</sub> Temperature Coefficient		---	4.6	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	-5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	8.9	---	Ω
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-15A	---	19	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	6.3	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	4.5	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-15A	---	6	---	ns
T <sub>r</sub>	Rise Time		---	5	---	
Td(off)	Turn-Off Delay Time		---	25	---	
T <sub>f</sub>	Fall Time		---	7	---	
Ciss	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	900	---	pF
Coss	Output Capacitance		---	140	---	
Crss	Reverse Transfer Capacitance		---	120	---	
IS	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-20	A
ISM	Pulsed Source Current		---	---	-80	A
VSD	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1.2	V
trr	Reverse Recovery Time	I <sub>F</sub> =-15A, dI/dt=100A/μs, T <sub>J</sub> =25°C	---	7	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	6.3	---	nC

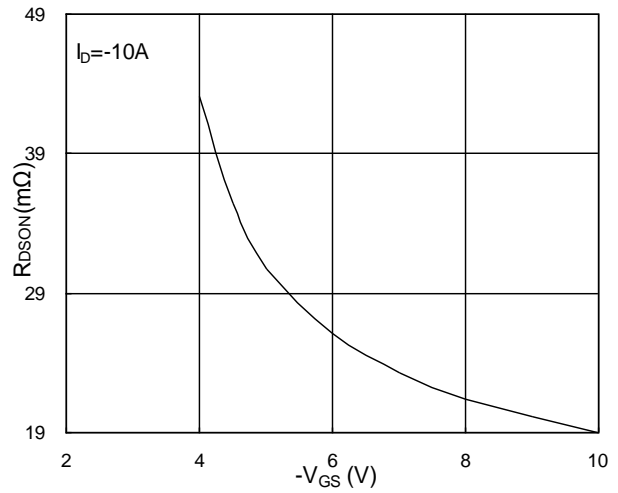
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-24V,V<sub>GS</sub>=-10V,L=0.1mH,I<sub>AS</sub>=-17A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

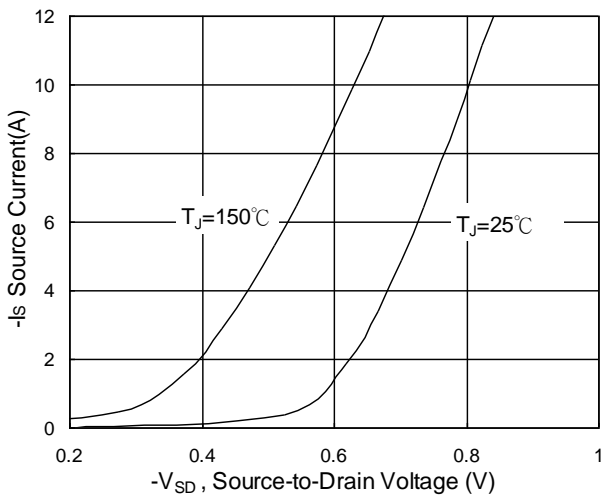
**Typical Characteristics**



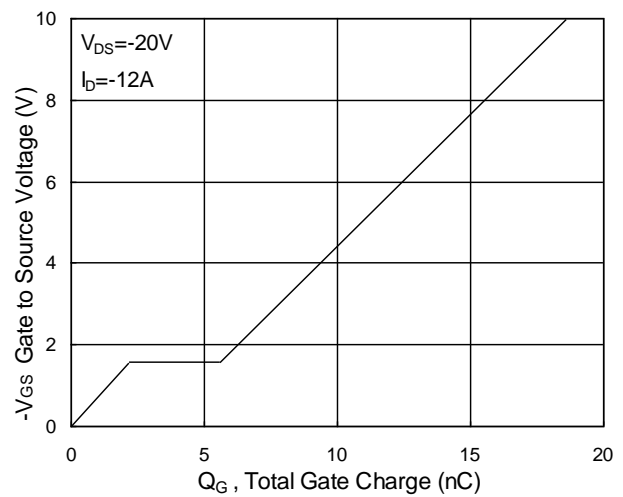
**Fig.1 Typical Output Characteristics**



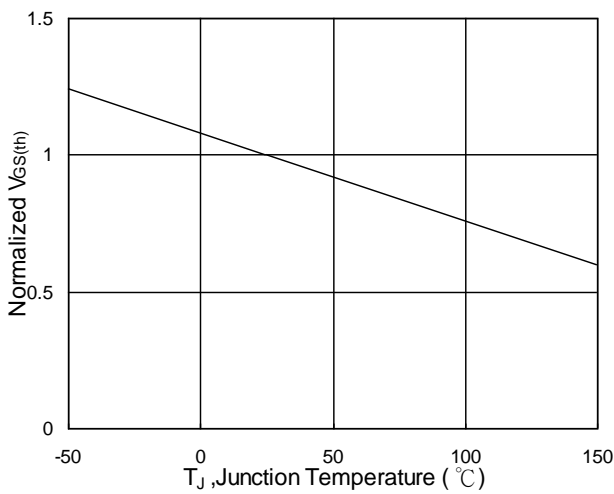
**Fig.2 On-Resistance v.s Gate-Source**



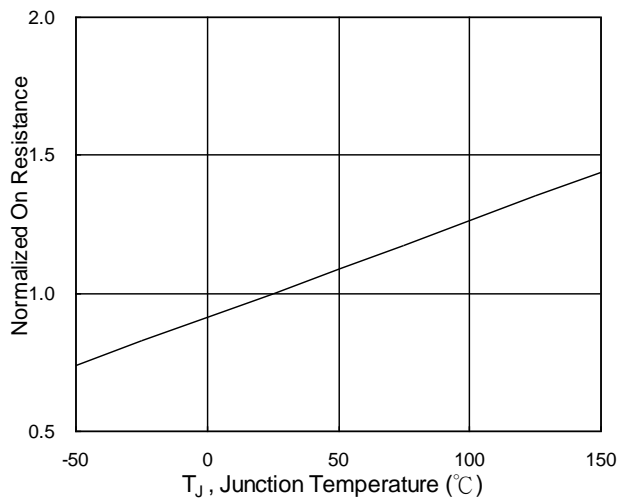
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



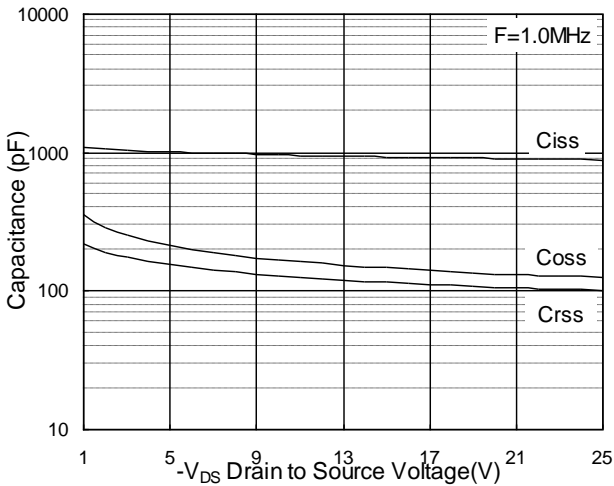
**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



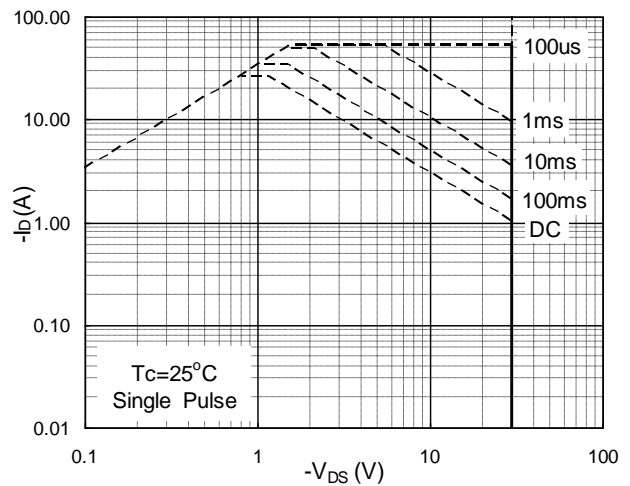
**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**



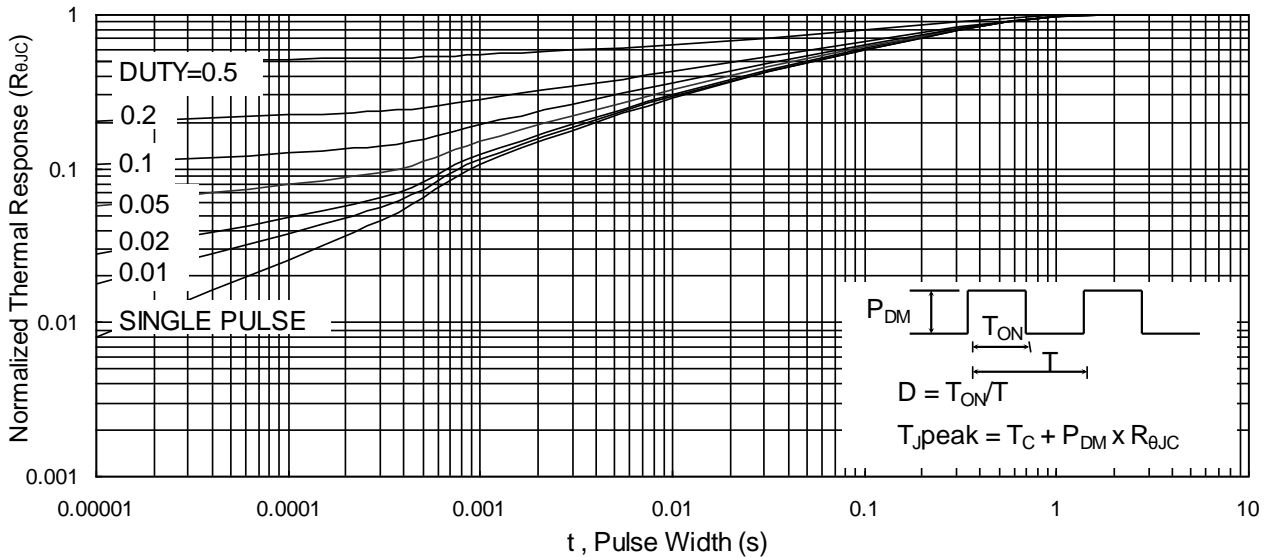
## 30V P-Channel Enhancement Mode MOSFET



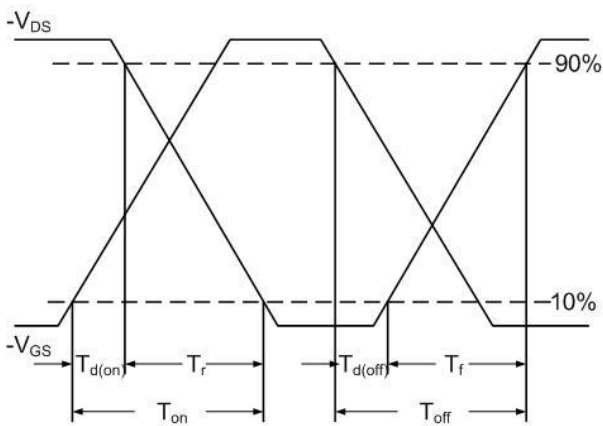
**Fig.7 Capacitance**



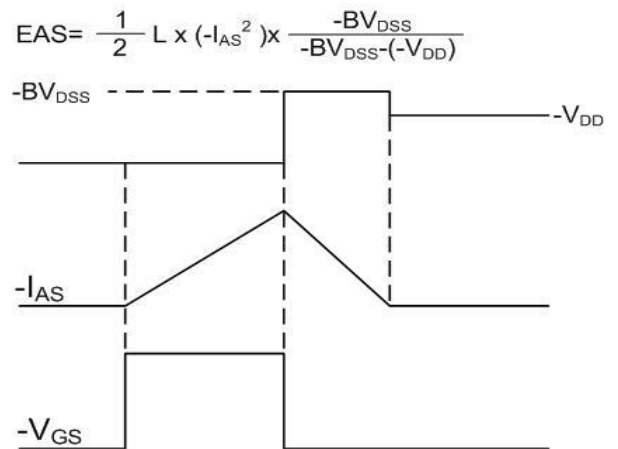
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



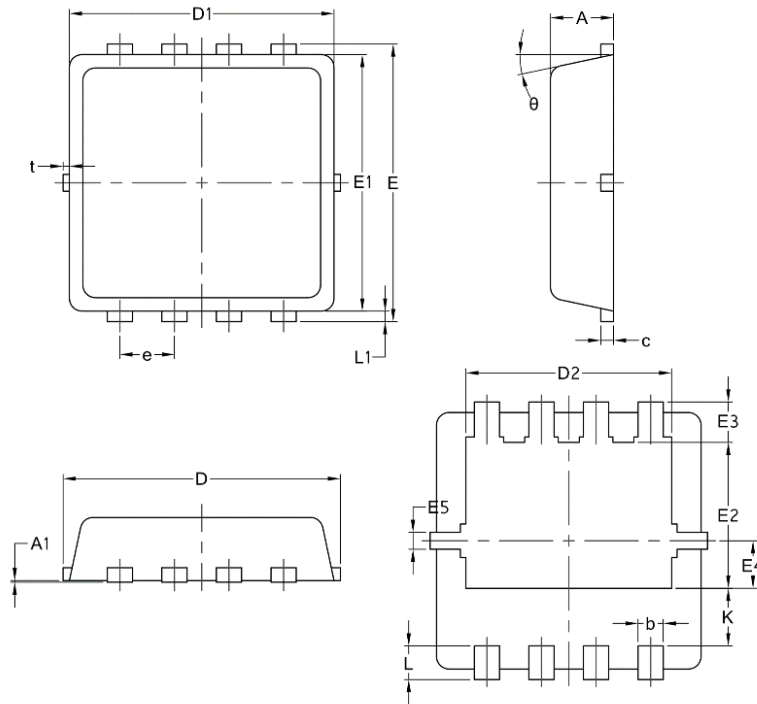
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**



### Package Mechanical Data-DFN3\*3-8L-JQ Single



Symbol	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

**30V P-Channel Enhancement Mode MOSFET****Attention**

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