

-40V P-Channel Enhancement Mode MOSFET

Description

The AP12P04S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -40V$ $I_D = -12A$

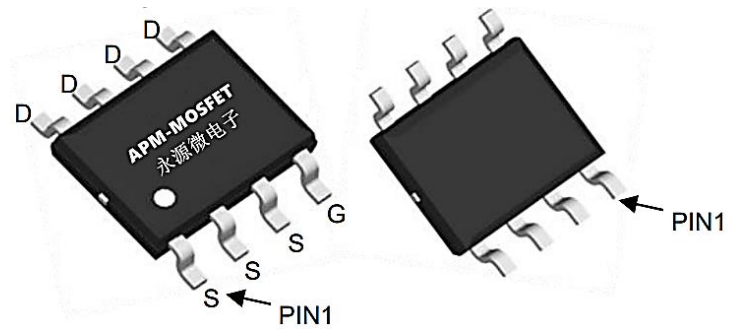
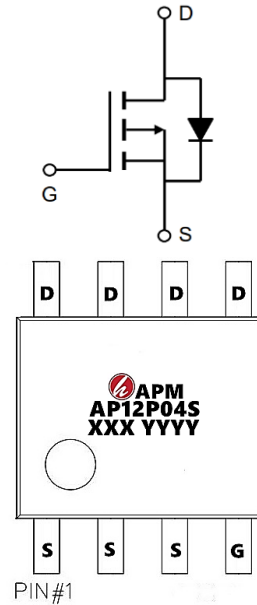
$R_{DS(ON)} < 18m\Omega$ @ $V_{GS} = -10V$ (Type: 14m Ω)

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP12P04S	SOP-8L	AP12P04S XXX YYYY	3000

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-12	A
$I_D @ T_C = 75^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-8.9	A
I_{DM}	Pulsed Drain Current ²	-36	A
EAS	Single Pulse Avalanche Energy ³	125	mJ
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	3.5	W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	1.9	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	5	$^\circ C/W$

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-40	-44	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.023	---	V/°C
R _{DS(on)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-30A	---	14	18	mΩ
		V _{GS} =-4.5V, I _D =-20A	---	18	25	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	-1.6	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.74	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-40V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-40V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-12A	---	25	---	nC
Q _{gs}	Gate-Source Charge		---	11	---	
Q _{gd}	Gate-Drain Charge		---	9.5	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15Ω I _D =-1A, V _{GEN} =-10V, R _G =6Ω	---	48	---	ns
T _r	Rise Time		---	24	---	
T _{d(off)}	Turn-Off Delay Time		---	88	---	
T _f	Fall Time		---	9.6	---	
C _{iss}	Input Capacitance	V _{DS} =-20V, V _{GS} =0V, f=1MHz	---	2760	---	pF
C _{oss}	Output Capacitance		---	260	---	
C _{rss}	Reverse Transfer Capacitance		---	85	---	
I _s	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-40	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-90	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.3	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

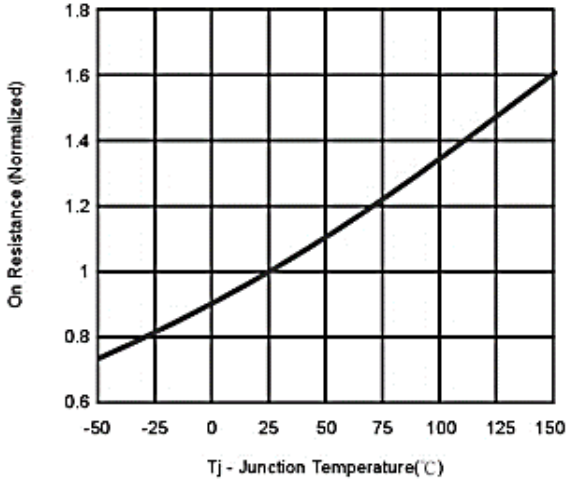


Fig.1 On Resistance Vs Junction Temperature

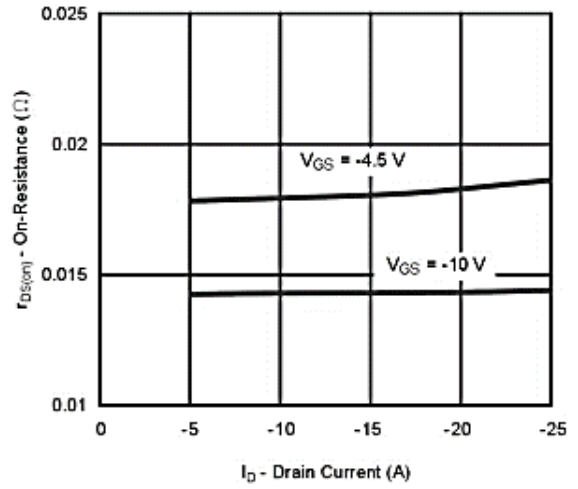


Fig.2 On-Resistance Vs. Drain Current

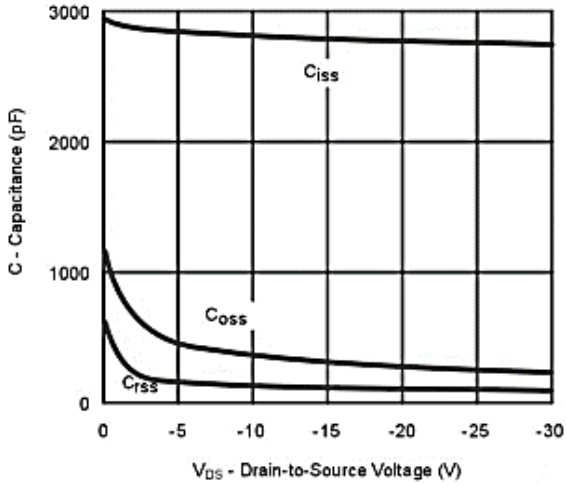


Fig.3 Capacitance

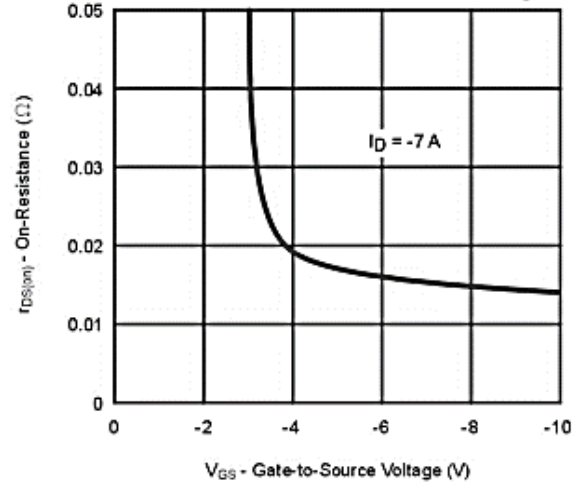


Fig.4 On-Resistance Vs. Gate-to-Source Voltage

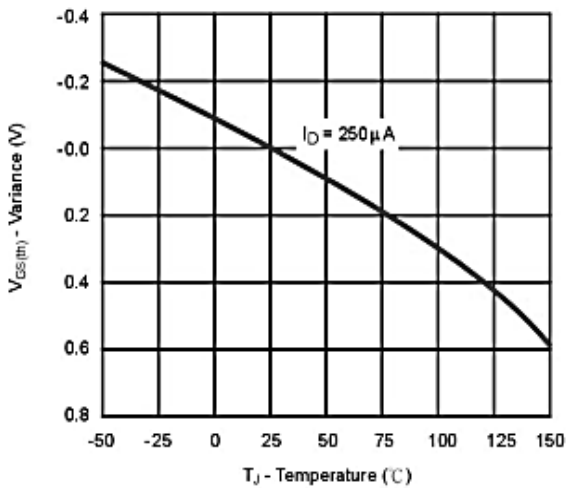


Fig.5 Threshold Voltage

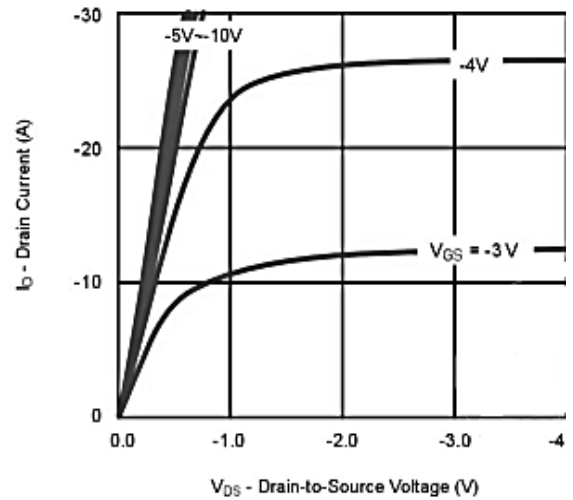


Fig.6 On-Region Characteristics



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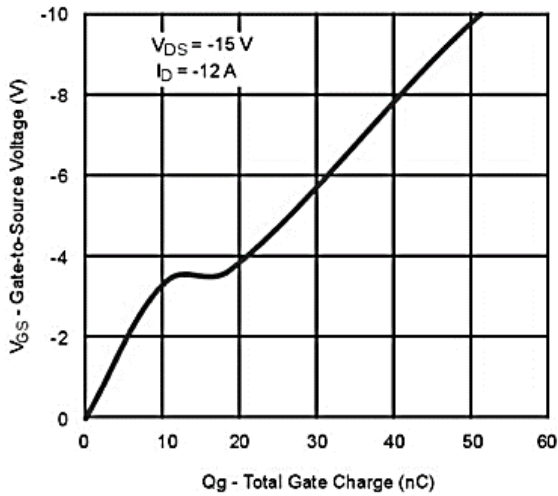


Fig.7 Gate Charge

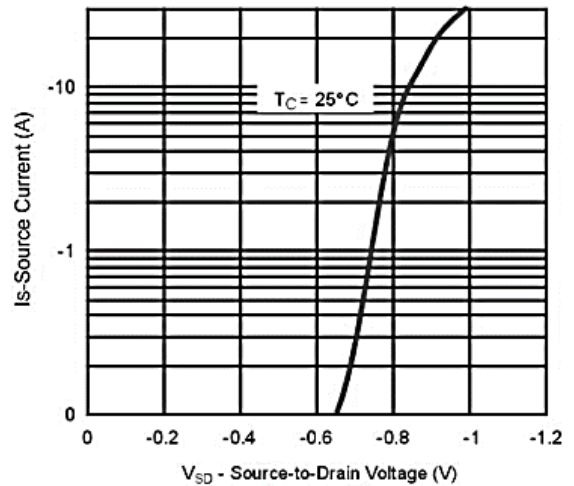


Fig.8 Body-diode Characteristic

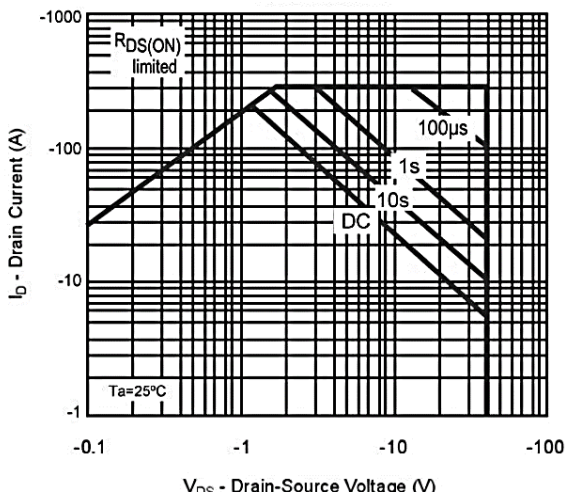


Fig.9 Safe Operating Area

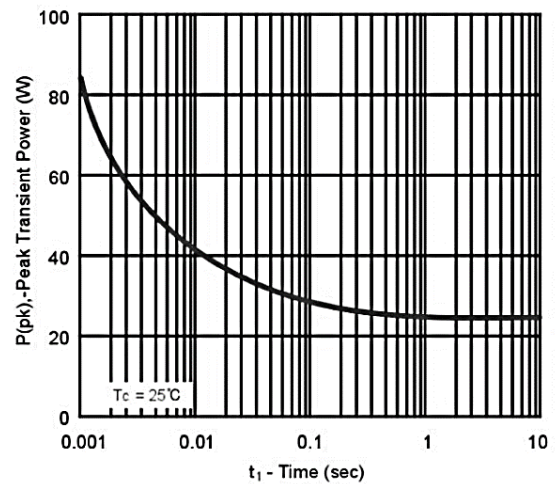


Fig.10 Single Pulse Maximum Power Dissipation

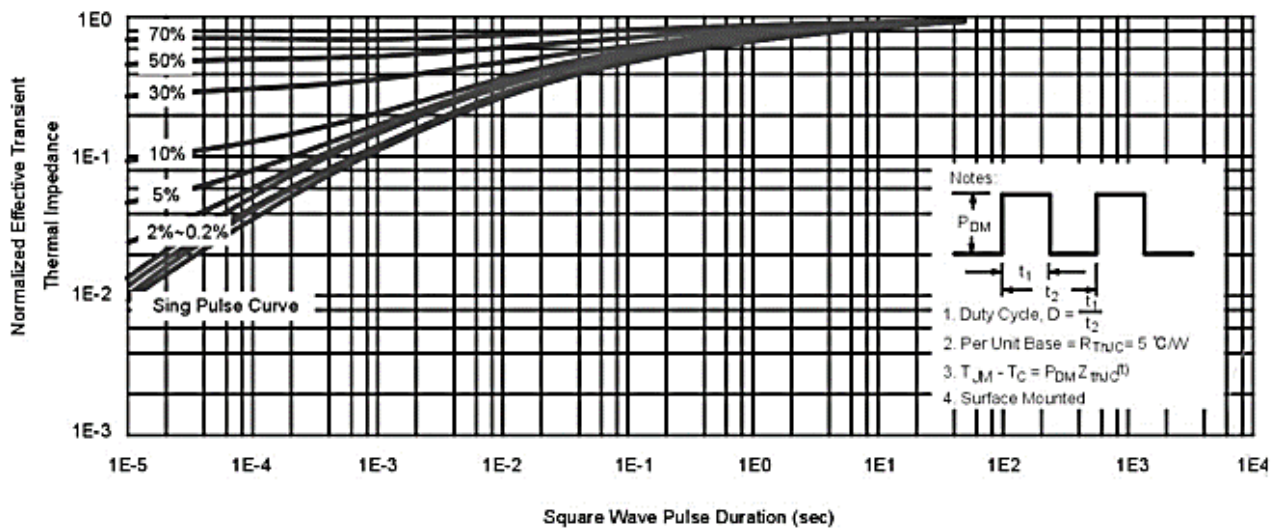
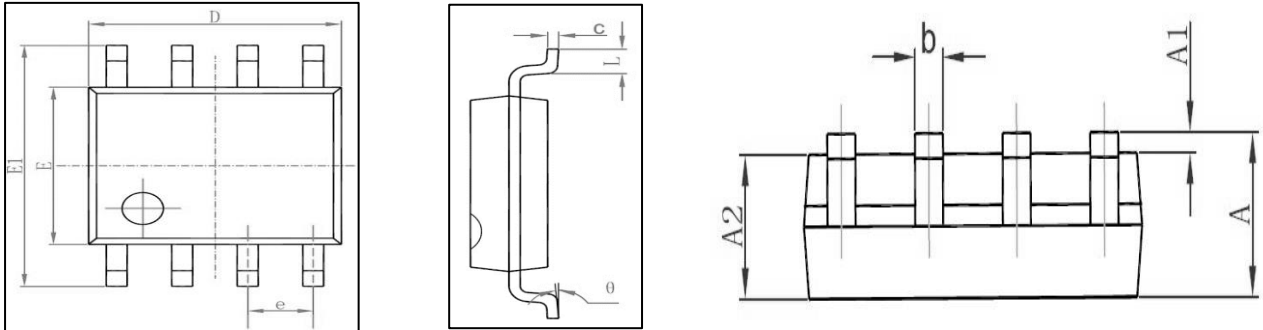
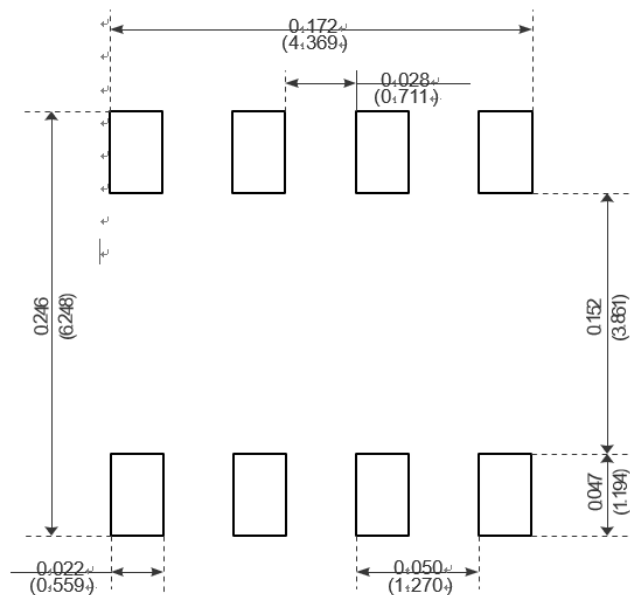


Fig.11 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-SOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

-40V P-Channel Enhancement Mode MOSFET**Attention**

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AP12P04S

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Edition	Date	Change
Rve1.0	2021/8/8	Initial release

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